ROLM® LAUNCH CONTROL CENTER COMPUTER (AN/UYK-19(V))

VOLUME 1

MODEL 1602B/D PROCESSOR

Contract No. N00019-76-C-0193

OPERATION AND MAINTENANCE MANUAL

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4900 Old Ironsides Drive
Santa Clara, California 95050

FEBRUARY 1981

SYSTEM CONFIGURATION

This manual has been specifically configured for the system whose serial number appears in the configuration tables at the end of Section I. These tables contain complete system configuration information, including equipment supplied, wiring lists, and system interconnection.

In addition to specific system configuration information, Section I includes a general description of the 1602B/D processor and associated system components. Sections II–VII deal exclusively with the CPU, core memory, control panel, and power supply. Appendix A contains a complete discussion of I/O operation and interfacing. Standard hardware options are described in Appendices B and C, and nonstandard modifications or additions are described in Appendix D.

AN INTRODUCTION TO THESE VOLUMES

The ROLM Ground Launched Cruise Missile (GLCM) launch control computer system consists of a Launch Control Center Computer (LCCC) and up to four satellite computer subsystems. The following figure provides an overall illustration of the system components and their relation to each other. This introduction briefly describes the overall system concept and individual unit functions.

Launch Control Center Computer

The Launch Control Center Computer consists of a ROLM 1666/D Computer, a 1648 Control Panel, and two 2166/D-(v) Computer Interface Units. The LCCC is the central data processing and command computer for up to four satellite sites. Detailed LCCC information is contained in this two-volume manual, which covers operation and maintenance of the Model 1666/D Computer and 2166/D-(v) Computer Interface Unit.

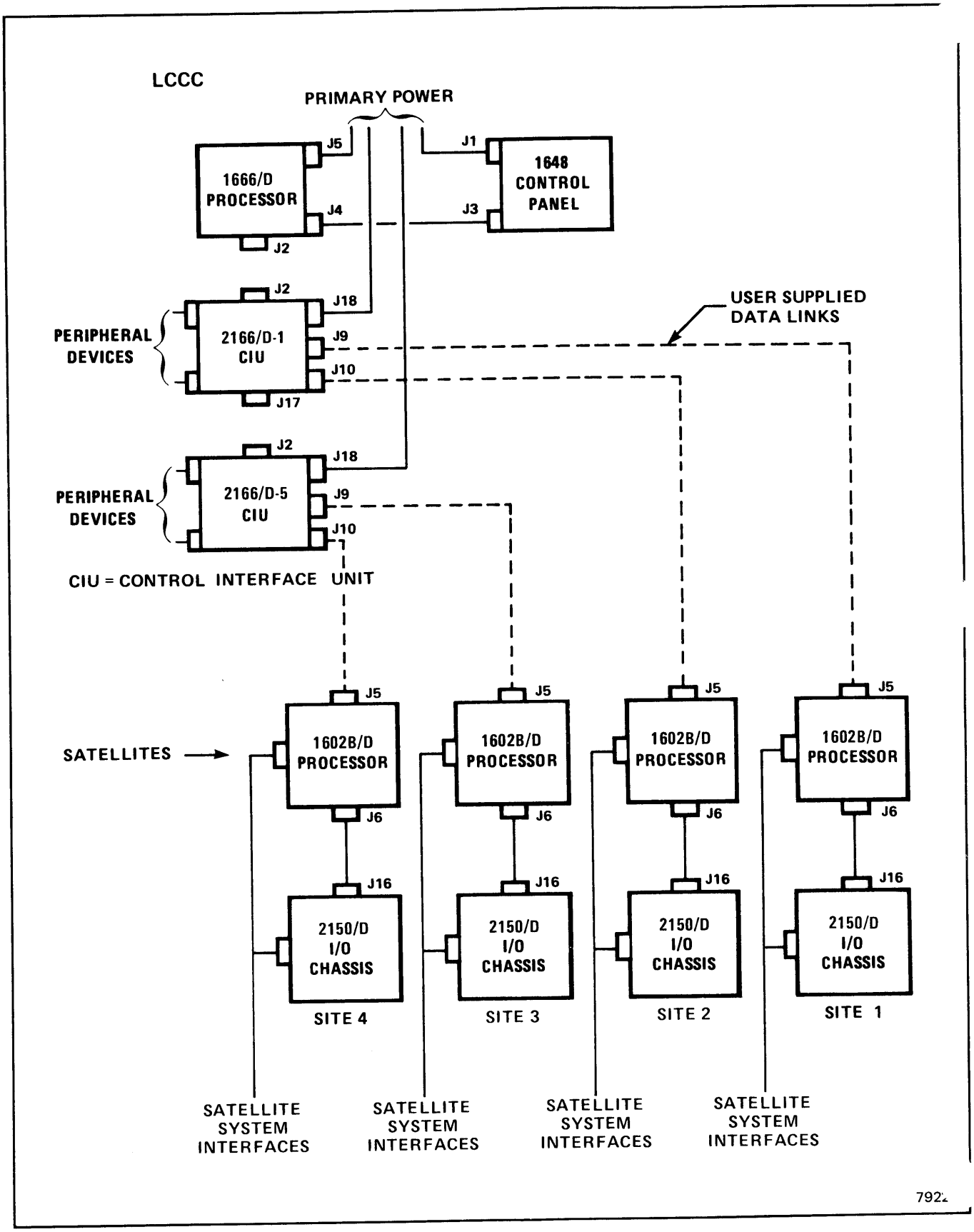
1666/D Digital Computer. The 1666/D Digital Computer contains the basic processor, Floating Point Processor (FPP), 64K words of core memory, and a Resource Management Unit (RMU). All calculations (except floating point arithmetic) are performed by the basic processor. The operating program and working memory are contained in core memory. All interface with external units is accomplished via a single Input/Output (I/O) bus. The RMU allows use of a large physical-address range by a smaller logical-address range. In addition, the 1666/D core memory capacity may be expanded by adding remote memory in the 2166/D-(v) Computer Interface Units if future requirements dictate.

2166/D-(v) Computer Interface Units. The 2166/D-(v) Computer Interface Units provide I/O bus interface slots for modules that enable the 1666/D Computer to communicate with external peripheral devices. The different-version computer interface units are equipped with special function interface modules, which communicate with particular peripherals, as dictated by system configuration. The 2166/D-(v) is described in the LCCC Operation and Maintenance Manual, Volume II. Detailed information on the individual interface modules installed in the 2166/D-(v)'s is provided in Appendix B inserts at the rear of Volume II.

The 2166/D-(v) also provides serial interface from the 1666/D I/O bus to the satellite computers. Actual interface connection between the LCCC and satellite computers is provided via customer-supplied devices using MIL-STD-1397 protocol and signal level/rates. In addition, each 2166/D-(v) computer interface unit may be equipped with up to 32K of remote memory, as future system requirements dictate.

Satellite Computer Systems

Up to four satellite computer systems may be associated with each LCCC. Each satellite computer system consists of a ROLM 1602B/D Processor and 2150 I/O Chassis.



GLCM Launch Control Computer System

1602B/D Processor

The ROLM 1602B/D is a basic processor unit equipped with a single board CPU, 16K words of memory, and accommodations for up to seven I/O bus modules. One of the I/O bus modules is dedicated to communications with the LCCC. The 1602B/D performs local processing tasks at the installed site and makes all data available to the LCCC through the dedicated data link. Detailed 1602B/D information is available in a separate operation and maintenance manual. (References in this manual to the 1602B apply to the 1602B/D).

2150/D I/O Chassis

The 2150/D I/O Chassis provides accommodations for up to 15 interface modules on the 1602B/D I/O bus. All modules in the 2150/D I/O Chassis regard the local 1602B/D as their host processor. Detailed 2150/D Chassis and I/O bus operation is provided in the 2150/D operation and maintenance manual. (References in this manual to the 2150 apply to the 2150/D).

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SECTION I
GENERAL DESCRIPTION

1.1 INTRODUCTION

The ROLM® Model 1602B (Figure 1-1) is one of an upward-compatible family of general-purpose digital processors based on the AN/UYK-19(V), designed for high reliability in hostile or severe environments. The 1602B has the same computing capability provided by the earlier Model 1602 and 1602A processors. It is packaged in a 19.56-inch ATR chassis that accommodates the CPU module, up to four 16K-word core memory modules (1 μs cycle time), seven Input/Output (I/O) slots, an optional ROM and an optional CPI board, a power supply, an EMI filter, I/O bus connections, and input power connections.

The CPU is a Model 5605 Processor Card Set, which is microprogrammed and executes 52-bit microinstructions in 150 to 250 ns cycle times. Use of the latest bipolar LSI technology allows the entire CPU to be packaged on a single folded-board circuit module. The 1602B instructions are the same as those for use with the Model 1602 and 1602A Processors.

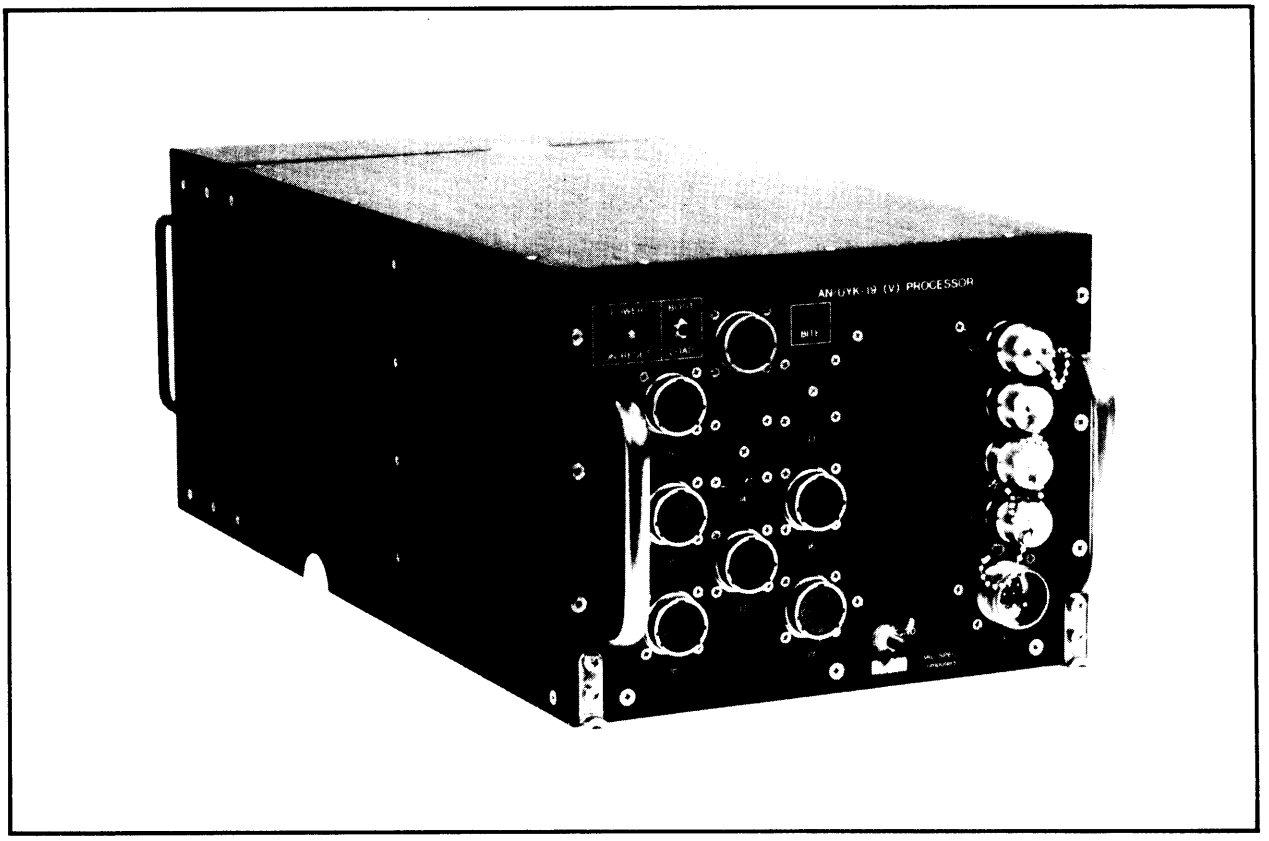


Figure 1-1. Model 1602B Processor

A variety of I/O options are available for 1602B systems, including parallel and serial digital interfaces, analog-to-digital and digital-to-analog converters, and serial communication interfaces. Controllers are available for a wide range of peripheral devices, including teletypewriter, paper tape equipment, line printers, magnetic tape, and disk. Standard I/O options are interchangeable with those of other ROLM processors.

The 1602B uses the same rugged packaging and conductive cooling techniques proved effective on other ROLM processors. The chassis is designed for ATR rack mounting; other mounting provisions are optional.

The Model 1635 or Model 1638 Control Panel for use with the Model 1602B processor provides for manual data entry, examination of stored data, and operational control. The control panel connects by cable to the processor, permitting remote mounting. It is of ATR cross section, and it has a self-contained power supply and LED displays.

The control panel is interfaced to the 1602B with a Model 1642 Control Panel Interface (CPI) module. In addition to control panel interface logic, the CPI module provides a real-time clock, terminal interface, and paper tape reader interface.

Basic specifications for the ROLM Model 1602B Processor are listed in Table 1-1. The processor has been designed to the environmental specifications of MIL-E-5400, MIL-E-4158, and MIL-E-16400 for aircraft, ground based, and shipborne electronic equipment, respectively. In addition, the processor is designed to electromagnetic interference and susceptibility requirements of MIL-STD-461.

Sections II through V of this manual describe the installation, operation, theory, and maintenance for the central processor unit (CPU), CPI board, power supply, control panel, and core memory. Applicable schematic drawings (excluding schematics for the CPU, I/O, and any special configuration) are included in Section VI. Parts lists and assembly drawings are included in Section VII. Optional assemblies, which may be purchased for use with the basic processor, are described in the appendices. A complete discussion of the I/O operation is contained in Appendix A, and a discussion of all standard I/O options ordered is given in Appendix B. Other optional items (such as the heat exchanger) are described in Appendix C. In some cases there are special modifications to the processor and I/O interfaces made at the request of the buyer. When such modifications are included, they are described in Appendix D.

1.2 GENERAL OPERATING PRINCIPLES

The ROLM Model 1602B Processor can be functionally operated in many varied applications. Generally the processor is configured with I/O options to directly interface with one or more devices that are external to the processor and are part of the overall system. The processor itself is then part of some larger system. The operation of the processor is controlled by a software program that is loaded into memory (or sometimes is located in a fixed read-only memory). Each instruction of the program "tells" the processor to perform a specified action. These instructions can move data to or from memory, move data to or from an I/O device, perform arithmetic and logic manipulations of data, and sense or control the status of external devices.

Table 1-1. ROLM Model 1602B Specifications

CPU

Architecture	Microprogrammed
Microinstruction Word	52 bits
Microcycle Time	150–250 ns
Microinstruction Capacity	1024 words
Number of Full-Length Registers	18

MAIN MEMORY

Word Length	16 bits
Maximum Size	65,536 words
Core Cycle Time	1.0 μs
Core Increment	16,384 words

I/O

Number of Addressable Devices	61
Interrupt Levels	16
DMA Word Rate (core memory)	666 kHz max

PHYSICAL

1602B standard chassis with CPU, CPI, ROM, seven I/O modules, four 16K memory modules and power supply

Size:	7.62 in. (19.35 cm) high x 10.12 in. (25.7 cm) wide x 19.56 in. (49.68 cm) deep
Weight:	74 ± 2 lb (33.5 ± 1 kg)

1635 or 1638 Control Panel

Installation:	Connects via cables to computer (Options 10, 11, 12)
Size:	7.75 in. (19.69 cm) x 10.25 in. (26.04 cm) x 5.35 in. (13.59 cm)
Weight:	9 lb

POWER

47–440 Hz, 115 (±15) Vac, single-phase. At 400 Hz, meets MIL-STD-704B.

OR

28 Vdc, per MIL-STD-704B.

Table 1-1. ROLM Model 1602B Specifications (Continued)

ENVIRONMENTAL

The 1602B Processor has been designed to meet the following environmental specifications, which meet or exceed those of MIL-E-5400 Class 2 and MIL-E-16400 Range 3:

Case Temperature	Standard:	0° to +65°C
	Wide:	−25°C to +75°C
	Extreme:	−55°C to +95°C
Model 3902 Heat Exchanger		
Inlet Air Temperature	Standard:	0° to +50°C
	Wide:	−25° to +60°C
	Extreme:	−55° to +71°C
Vibration	10g, 5-2000 Hz, with vibration isolators (MIL-E-5400, Curve IVa)	
	2g, 5-2000 Hz, hard-mounted (MIL-E-5400, Curve IIa)	

A simplified block diagram of the processor is given in Figure 1-2. This shows the basic interrelation between the processor assemblies. The CPU provides for all transfer and manipulation of data. Words (data and instructions) can be stored or fetched from memory. The processor performs a program by executing instructions retrieved from consecutive memory locations as counted by the program counter (PC). At the end of each instruction, PC is incremented by one so that the next instruction is normally taken from the next consecutive location. Sequential program flow is altered by changing the contents of PC, either by incrementing it an extra time in a test skip instruction or by replacing its contents with the value specified by a jump instruction. Other internal registers of importance to the programmer are four 16-bit accumulators, AC0 to AC3. Data can be moved in either direction between any memory location accumulator. Associated with the accumulators are two flags, Carry and Overflow. Carry indicates when a carry occurs out of bit 0 in an arithmetic instruction; Overflow occurs when an arithmetic operation results in an arithmetic overflow. Operands for arithmetic and logical operations may be located in the accumulators or, in some cases, in memory. Arithmetic instructions include add, subtract, complement, negate, multiple, divide, and arithmetic shift. Logical instructions include OR, AND, exclusive OR, and logical shifts. Memory reference instructions allow use of AC2 or AC3 as an index register, as well as multiple level indirect addressing. Double word memory reference instructions allow direct addressing of any location in memory.

Input/Output hardware allows the program to address up to 61 devices. A single instruction can transfer a word between an accumulator and a device interface and at the same time control the device operation. Included in the I/O system are facilities for program interrupts and high-speed data transfers. The interrupt system facilitates processor control of the peripheral equipment by allowing any device to interrupt the normal program flow on a priority basis. A high-speed device, such as magnetic tape or disk, can gain direct access to memory through a

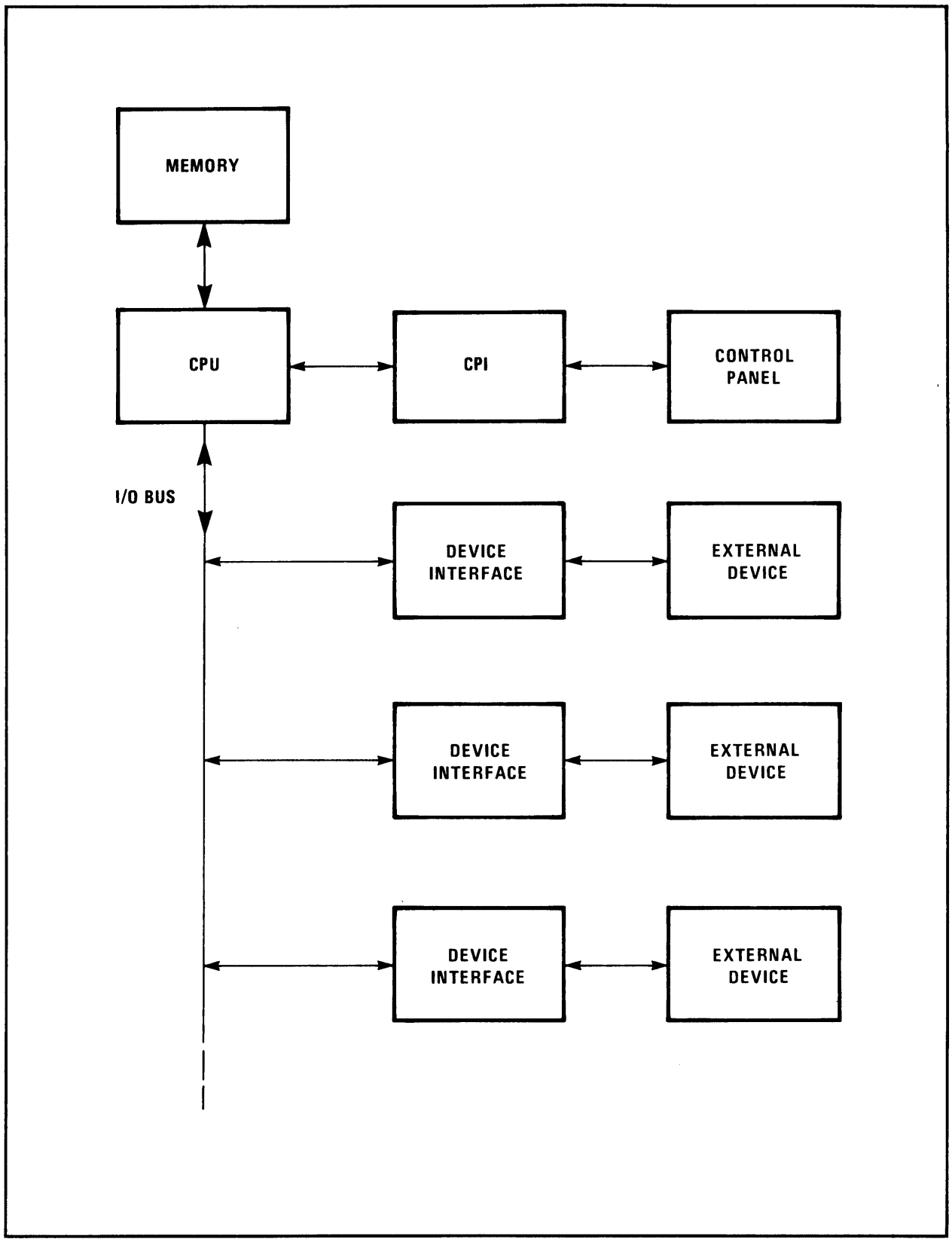


Figure 1-2. Simplified Block Diagram

data channel without requiring execution of any instructions. All communications with external devices are done via the I/O bus. This bus consists of 16 bidirectional data lines, 6 device selection lines, and 23 control lines. Since external devices operate with different control requirements and data transfer rates, a device interface is generally required to adapt the device to the I/O bus circuits and timing.

The control panel provides data entry switches and various control switches. It includes indicators to display content of a memory location or accumulator. The program counter and various status flags are also displayed.

1.3 SYSTEM CONFIGURATION

Tables 1-2 through 1-7 contain detailed information about the 1602B system for which this manual has been configured. The information includes equipment supplied, system configuration, wiring, and cabling. The tables accurately reflect the system as it was shipped from the factory. It is the user's responsibility to maintain records of field changes and system modifications if, or as, they occur.

Table 1-2, System Diagram, represents the proper physical arrangement and connection of all items supplied (as listed in Table 1-3) with the exception of accessories. Continuation sheets of Table 1-2 show the internal organization of each chassis, including front panel connector wiring references. For each location containing an I/O interface, the device code, interrupt and data channel priorities (IPC, DPC), and mask bit (if nonstandard) are given. The highest interrupt priority interface is 1, then 2, and so on. If an I/O slot does not contain a card, a Model 3566 Priority/Load Module (Paragraph 2.11) must be installed to maintain continuity of the priority chains. See Appendix A for a complete discussion of I/O operation.

Table 1-3, Equipment Supplied, lists all major system components, including peripheral devices, cables, and accessories. An item listed at assembly Level 1 is a catalog item, and an item listed in Level 2 is a modular subassembly of the nearest Level 1 item above it. If a Level 2 contains a model number, it may be ordered separately for spares purposes. The items listed in Table 1-3 are cross referenced by index number to Table 1-2, System Diagram. The reference designation indicates the chassis and, if applicable, the location of a module within the chassis (e.g., A1A4 indicates location A4 of chassis A1). Also indicated for each item is the ROLM part number, revision level, and serial number where applicable.

Table 1-4, Memory Configuration, summarizes the sizes and types of memory installed in the system, with logic (software) address segments referenced to the hardware modules containing the memory elements. For semiconductor memory modules, logical addressing is determined by jumpers on the module itself. Refer to the appropriate section of Appendix C for details of logical addressing for semiconductor memories.

Table 1-5 is reserved. Table 1-6 lists all software shipped with the system. The upper portion of the table lists model numbers of standard software and CPU diagnostics; the lower portion itemizes diagnostic software manuals and tapes related to various I/O and other units. Shiplists included with the software give detailed listings of tapes and manuals comprising a software model number.

Table 1-7 lists accessories shipped with the system. Following Table 1-7 are all wiring lists for panel connectors and, as appropriate, system cable drawings and intrachassis wiring lists.

APPLICATION		REVISIONS			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
FINAL	109209-03	A	RELEASE PER ER G/SLCM-02 [illegible]	2/20/81	[illegible]

ROLM P/N 109209-03

MDAC P/N 70P187402-2107

SYSTEM S/N _____

PREP _____ DATE _____

APP. _____ DATE _____

APP. _____ DATE _____

APP. _____ DATE _____

A	A	A	A	A	A	A	A	A	A																					
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33

RECORD OF REVISION STATUS OF EACH SHEET

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES

DECIMALS
2 PLACE ±
3 PLACE ±

ANGLES
±

MATERIAL

CONTR NO.

		DATE
DR	[signature]	2/6/81
CHK	M. Wolfe	2-9-81
APPD	J. Tye	2/20/81
APPD	[signature]	
ACCPD	[signature]	2/20/81

ROLM MIL-SPEC Computers

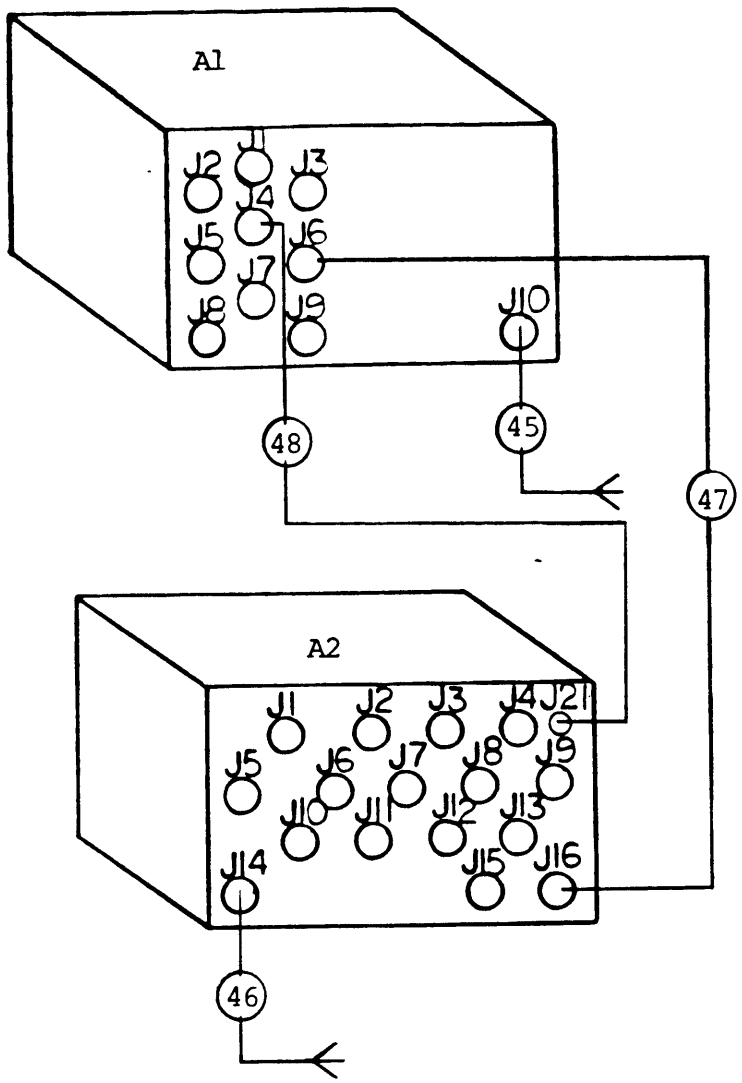
4900 OLD IRONSIDES DRIVE
SANTA CLARA, CA. 95050

CONFIGURATION CONTROL DRAWING
GLCM SATELLITE COMPUTER SYSTEM

SIZE	CODE IDENT NO.	DWG NO.
A	14345	03-110696

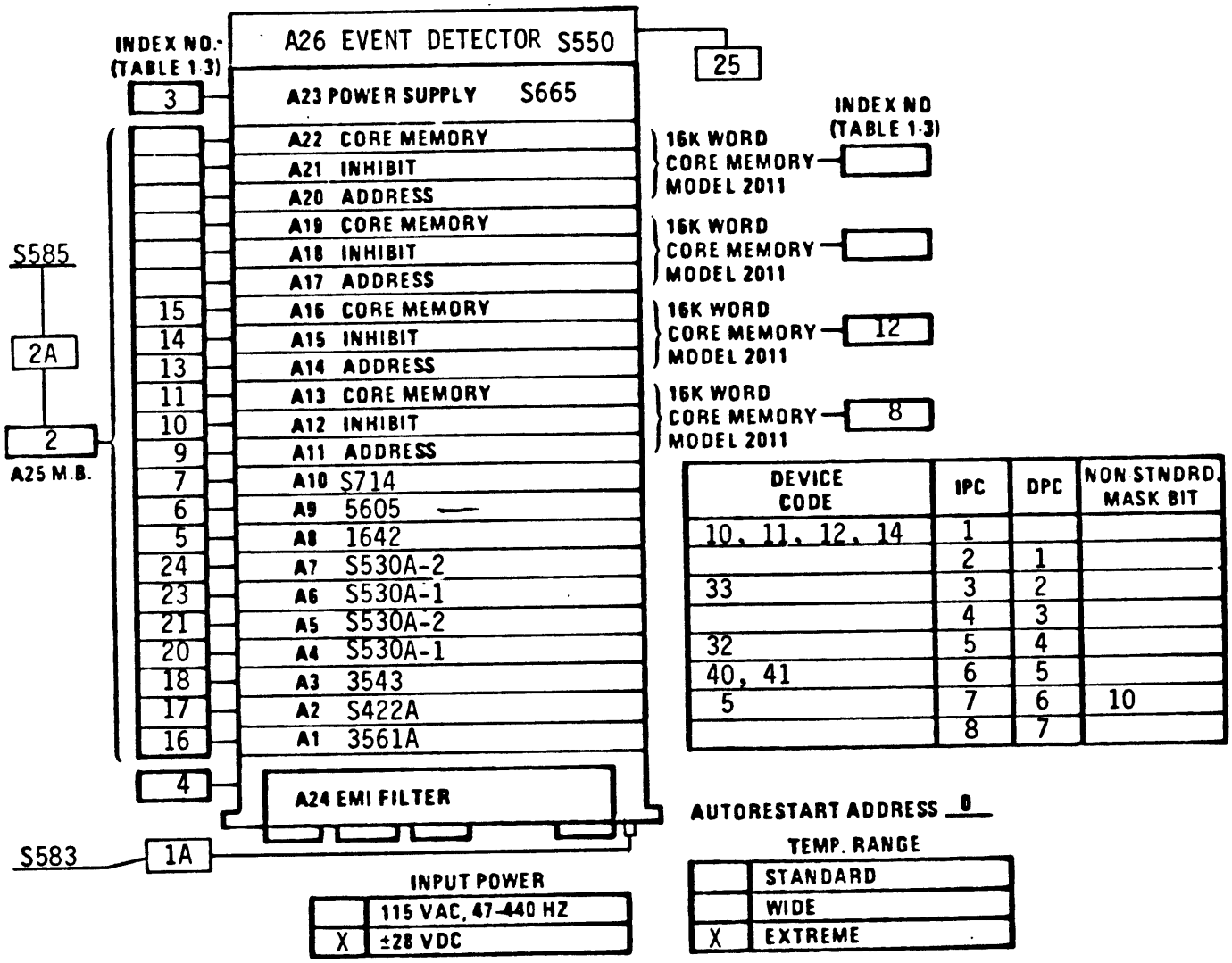
SHEET 1 OF 10

GLOM SATELLITE COMPUTER SYSTEM DIAGRAM



SIZE	CODE IDENT NO.	DWG NO.
A	14345	
	REV	SHEET

TABLE 1-2
GLCM SATELLITE COMPUTER SYSTEM
1602B/D PROCESSOR (A1)



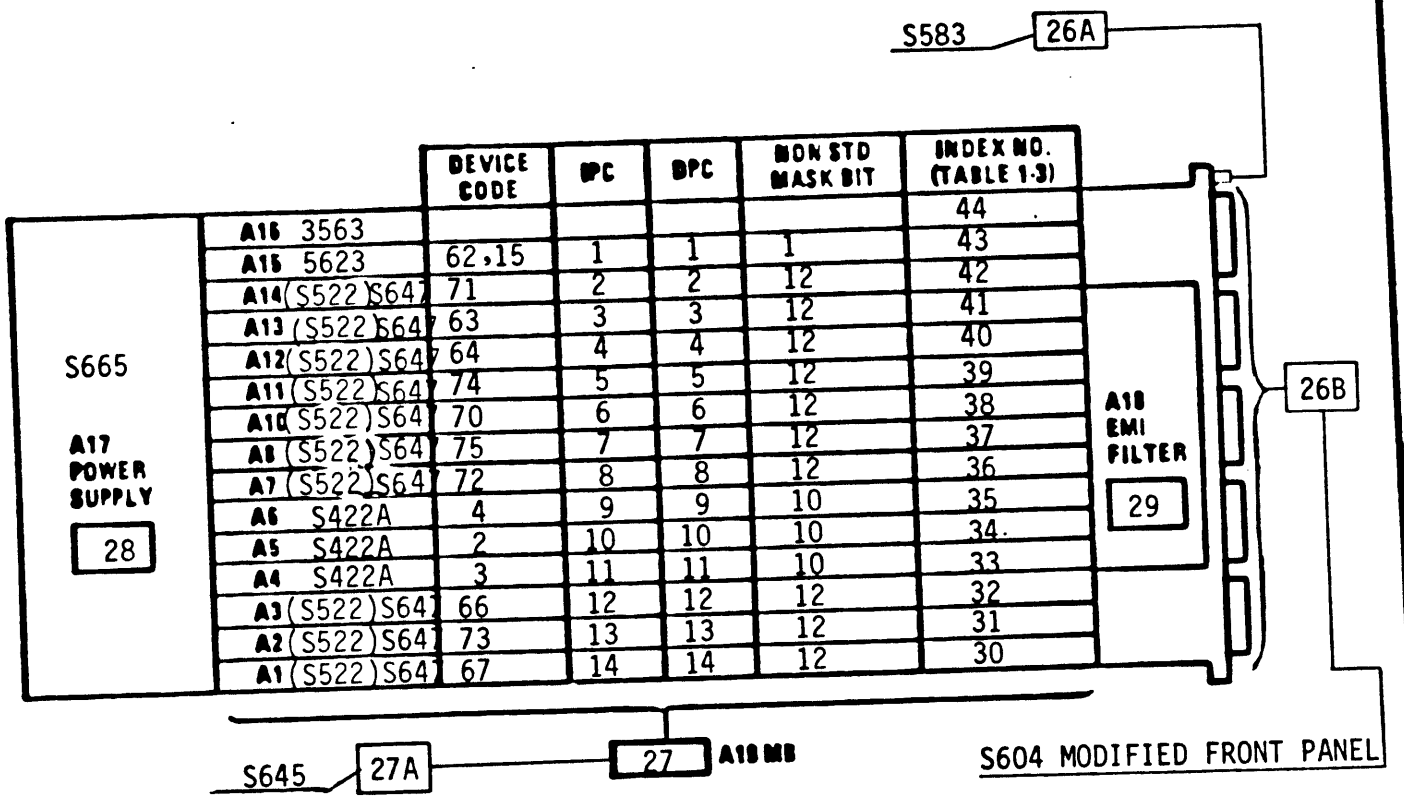
DEVICE CODE	IPC	DPC	NON STNDRD MASK BIT
10, 11, 12, 14	1		
	2	1	
33	3	2	
	4	3	
32	5	4	
40, 41	6	5	
5	7	6	10
	8	7	

FRONT PANEL CONNECTOR	DESTINATION	WIRING ASSEMBLY OR LIST	DRAWING NUMBER
J1	A8	Terminal/Paper Tape Reader 1642	WL-110531
J2	A3	I/O Buffer, Option 60 3543	WL-110531
J3			
J4	A26	S550 Nuclear Event Detector/S585 Harness	109786
J5	A4,A5	Serial DMA Interface S530 Set	WL-110531
J6	A1	Single I/O Bus Expander 3561A	WL-110531
J7	A2	S422A MK-82 Interface	WL-110531
J8	A6,A7	Serial DMA Interface S530 Set	WL-110531
J9	CONTROL PANEL	Control Panel	WL-110531
J10	POWER	S665 POWER SUPPLY	WL-110531

SIZE	CODE IDENT NO.	DWG NO.
A	14345	03-110696
	REV A	SHEET 2

TABLE 1-2

GLCM SATELLITE COMPUTER SYSTEM
2150/D I/O CHASSIS
(A2)



	DEVICE CODE	BPC	BPC	NON STD MASK BIT	INDEX NO. (TABLE 1-3)
A16 3563					44
A15 5623	62,15	1	1	1	43
A14 (S522) S647	71	2	2	12	42
A13 (S522) S647	63	3	3	12	41
A12 (S522) S647	64	4	4	12	40
A11 (S522) S647	74	5	5	12	39
A10 (S522) S647	70	6	6	12	38
A8 (S522) S647	75	7	7	12	37
A7 (S522) S647	72	8	8	12	36
A6 S422A	4	9	9	10	35
A5 S422A	2	10	10	10	34
A4 S422A	3	11	11	10	33
A3 (S522) S647	66	12	12	12	32
A2 (S522) S647	73	13	13	12	31
A1 (S522) S647	67	14	14	12	30

INPUT POWER

	115 VAC, 47-440 HZ
	±28 VDC

TEMP. RANGE

	STANDARD
	WIDE
	EXTREME

FRONT PANEL CONNECTOR	DESTINATION	WIRING ASSEMBLY OR LIST		DRAWING NUMBER
J1	A3	(S522) Relay I/O Interface	S647	WL-110557
J2	A5	S422A MK-82 Interface		WL-110557
J3	A10	(S522) Relay I/O Interface	S647	WL-110557
J4	A14	(S522) Relay I/O Interface	S647	WL-110557
J5	A1	(S522) Relay I/O Interface	S647	WL-110557
J6	A4	S422A MK82		WL-110557
J7	A7	(S522) Relay I/O Interface	S647	WL-110557
J8	A11	(S522) Relay I/O Interface	S647	WL-110557
J9	A15	S5623 I/O Tester		WL-110557
J10	A2	(S522) Relay I/O Interface	S647	WL-110557
J11	A6	S422A MK82 Interface		WL-110557
J12	A8	(S522) Relay I/O Interface	S647	WL-110557
J13	A13	(S522) Relay I/O Interface	S647	WL-110557
J14	POWER A17	S665 POWER SUPPLY		WL-110555
J15	A12	(S522) Relay I/O Interface	S647	WL-110557
J16	A16	3563 I/O Bus Repeater		WL-110557
J22	---	S645 Internal Harness		WL-110555

Note: Items in parenthesis are shipped in place of the items they are preceded by.

SIZE	CODE IDENT NO.	DWG NO.
A	14345	03-110696
	REV A	SHEET 3

TABLE 1-3

GLCM SATELLITE COMPUTER SYSTEM
EQUIPMENT SUPPLIED
(A1) CONT'D.

TABLE 1-2 INDEX NO.	MODEL NO.	ASSY LEVEL	DESCRIPTION	REF. DESIG.	PART NO.	REV	SERIAL NO.
1	1602B/D	2	PROCESSOR OPTION 3: EXTREME TEMP, RANGE OPTION 8: CUSTOM LOADER PROM (TBD) OPTION 15: BITE/FLOATING POINT OPTION 16: SINGLE CABLE I/O BUS WIRING OUT OPTION 21: DC POWER OPTION 60: ILS WIRING (CO-CP 3101)	A1	109211-03		
1A	S583	3	OPTO RESET SWITCH POWER ON/RESET		109746-01		
2	- - -	3	MOTHERBOARD ASSY	A1A25	110531-01		
2A	S585	3	INTERNAL HARNESS	A1A25	109786-01	N/A	N/A
3	S665	3	POWER SUPPLY OPT. 3 EXTREME TEMP. RANGE	A1A23	110486-01		
4	3882	3	EMI FILTER, DC	A1A24	107142-01	N/A	N/A
5	1642	3	CONTROL PANEL INTERFACE OPT. 6 RS-232C COMPATIBILITY OPT. 7 READER/TERMINAL WIRING OPT. 17 9600 BAUD CLOCK ON TERMINAL	A1A8	104502-02		
6	5605	3	PROCESSOR CARD OPTION 3: EXTREME TEMP. RANGE OPTION 15: BITE/FLOATING POINT	A1A9	102394-03		
7	S714	3	16K SPECIAL ROM	A1A10	112025-01	-	B/O
7A	S565	(3)	(16K SPECIAL ROM)	(A1A10)	(109574-01)	-	B/O
8	2011	3	CORE MEMORY SET OPTION 3: EXTREME TEMP. RANGE				

Note: Items in parenthesis are shipped in place of the items they are preceded by.

TABLE 1-3

GLCM SATELLITE COMPUTER SYSTEM EQUIPMENT SUPPLIED

(A1) (CONT'D)

TABLE 1-2 INDEX NO.	MODEL NO.	ASSY LEVEL	DESCRIPTION	REF. DESIG.	PART NO.	REV	SERIAL NO.
9		4	16K ADDRESS PWA	A1A11	101949		
10		4	16K INHIBIT PWA	A1A12	102261		
11		4	16K CORE STACK ASSY	A1A13	101818		
12	2011	3	CORE MEMORY SET OPTION 3: EXTREME TEMP. RANGE				
13		4	16K ADDRESS PWA	A1A14	101949		
14		4	16K INHIBIT PWA	A1A15	102261		
15		4	16K CORE STACK ASSY	A1A16	101818		

TABLE 1-3
GLCM SATELLITE COMPUTER SYSTEM
EQUIPMENT SUPPLIED
(A1) CONT'D.

TABLE 1-2 INDEX NO.	MODEL NO.	ASSY LEVEL	DESCRIPTION	REF. DESIG.	PART NO.	REV	SERIAL NO
16	3561A	3	I/O BUS EXPANDER WITH POWER FAIL	A1A1	106680-01		
17	S422A	3	MK 82 INTERFACE OPT. 5: ALT. MASK BIT (10) OPT. 9: EXTERNAL DVC. CODE	A1A2	109224-01		
18	3543	3	DIFFERENTIAL I/O BUFFER OPT. 6: OUTPUT CONFIGURATION-B OPT. 60: WIRING PER CO-CP-3100	A1A3	100928-01		
19	S530	3	SERIAL DMA CARD SET				
20	-	4	SERIAL DMA COMM INTL S530-A1 OPT. 9: EXTERNAL DEVICE CODE	A1A4	109286-01		
21	-	4	SERIAL DMA CONTROLLER S530-A2	A1A5	109290-01		
22	S530	3	SERIAL DMA CARD SET				
23	-	4	SERIAL DMA COMM INTF S530-A1 OPT. 9: EXTERNAL DEVICE CODE	A1A6	109286-01		
24	-	4	SERIAL DMA CONTROLLER S530-A2	A1A7	109290-01		
25	S550	3	NUCLEAR EVENT DETECTOR	A1A26	110423-01		

TABLE 1-3
GLCM SATELLITE COMPUTER SYSTEM
EQUIPMENT SUPPLIED
(A2) CONT'D

TABLE 1-2 INDEX NO.	MODEL NO.	ASSY LEVEL	DESCRIPTION	REF. DESIG.	PART NO.	REV	SERIAL NO.
26	2150/D	2	I/O INTERFACE UNIT OPT. 3: EXTREME TEMP. RANGE OPT.16: SINGLE CABLE I/O BUS WIRING OUT OPT.21: DC POWER OPT.60: ILS WIRING (CO-CP 3101)	A2	109206-03		
26A	S583	3	OPTO RESET SWITCH POWER ON/RESET		109746-01		
26B	S604	3	MODIFIED FRONT PANEL	A2	109790-01	N/A	N/A
27	----	3	MOTHERBOARD ASSY	A2A19	110557-01		
27A	S645	3	INTERNAL HARNESS	A2A19	109879-01	N/A	N/A
28	S665	3	POWER SUPPLY OPT. 3: EXTREME TEMP. RANGE	A2A17	110486-01		
29	3882	3	EMI FILTER, DC	A2A18	107142-01	N/A	N/A
30	S647	3	DISCREET I/O INTERFACE OPT. 5: ALT. MASK BIT (12) OPT. 9: EXTERNAL DEVICE CODE	A2A1	110598-01	-	B/O
(30A)	(S522)	(3)	RELAY I/O OPT. 5: ALT. MASK BIT (12) OPT. 9: EXTERNAL DEVICE CODE	(A2A1)	(109251-01)		
31	S647	3	DISCREET I/O INTERFACE OPT. 5: ALT. MASK BIT (12) OPT. 9: EXTERNAL DEVICE CODE	A2A2	110598-01	-	B/O
(31A)	(S522)	(3)	RELAY I/O OPT. 5: ALT. MASK BIT (12) OPT. 9: EXTERNAL DEVICE CODE	(A2A2)	(109251-01)		
32	S647	3	DISCREET I/O INTERFACE OPT. 5: ALT. MASK BIT (12) OPT. 9: EXTERNAL DEVICE CODE	A2A3	110598-01	-	B/O
(32A)	(S522)	(3)	RELAY I/O OPT. 5: ALT. MASK BIT (12) OPT. 9: EXTERNAL DEVICE CODE	(A2A3)	(109251-01)		

Note: Items in parenthesis are shipped in place of the items they are preceded by.

TABLE 1-3

GLCM SATELLITE COMPUTER SYSTEM EQUIPMENT SUPPLIED (A2) CONTINUED

TABLE 1-2 INDEX NO.	MODEL NO.	ASSY LEVEL	DESCRIPTION	REF. DESIG.	PART NO.	REV	SERIAL NO.
33	S422A	3	MK 82 INTERFACE OPTION 5: ALT. MASK BIT (10) OPTION 9: EXTERNAL DEVICE CODE	A2A4	109224-01		
34	S422A	3	MK 82 INTERFACE OPTION 5: ALT. MASK BIT (10) OPTION 9: EXTERNAL DEVICE CODE	A2A5	109224-01		
35	S422A	3	MK 82 INTERFACE OPTION 5: ALT. MASK BIT (10) OPTION 9: EXTERNAL DEVICE CODE	A2A6	109224-01		
36	S647	3	DISCRETE I/O INTERFACE OPTION 5: ALT. MASK BIT (12) OPTION 9: EXTERNAL DEVICE CODE	A2A7	110598-01	--	B/O
(36A)	(S522)	(3)	RELAY I/O INTERFACE OPTION 5: ALT. MASK BIT (12) OPTION 9: EXTERNAL DEVICE CODE	(A2A7)	(109251-01)		
37	S647	3	DISCRETE I/O INTERFACE OPTION 5: ALT. MASK BIT (12) OPTION 9: EXTERNAL DEVICE CODE	A2A8	110598-01	--	B/O
(37A)	(S522)	(3)	RELAY I/O INTERFACE OPTION 5: ALT. MASK BIT (12) OPTION 9: EXTERNAL DEVICE CODE	(A2A8)	(109251-01)		
38	S647	3	DISCRETE I/O INTERFACE OPTION 5: ALT. MASK BIT (12) OPTION 9: EXTERNAL DEVICE CODE	(A2A10)	110598-01	--	B/O
(38A)	(S522)	(3)	RELAY I/O INTERFACE OPTION 5: ALT. MASK BIT (12) OPTION 9: EXTERNAL DEVICE CODE	(A2A10)	(109251-01)		
39	S647	3	DISCRETE I/O INTERFACE OPTION 5: ALT. MASK BIT (12) OPTION 9: EXTERNAL DEVICE CODE	A2A11	110598-01	--	B/O
(39A)	(S522)	(3)	RELAY I/O INTERFACE OPTION 5: ALT. MASK BIT (12) OPTION 9: EXTERNAL DEVICE CODE	(A2A11)	(109251-01)		

Note: Items in parenthesis are shipped in place of the items they are preceded by.

TABLE 1-3

GLCM SATELLITE COMPUTER SYSTEM EQUIPMENT SUPPLIED (A2) CONTINUED

TABLE 1-2 INDEX NO.	MODEL NO	ASSY LEVEL	DESCRIPTION	REF. DESIG.	PART NO.	REV	SERIAL NO
40	S647	3	DISCRETE I/O INTERFACE OPTION 5: ALT. MASK BIT (12) OPTION 9: EXTERNAL DEVICE CODE	A2A12	110598-01	--	B/O
(40A)	(S522)	(3)	RELAY I/O INTERFACE OPTION 5: ALT. MASK BIT (12) OPTION 9: EXTERNAL DEVICE CODE	(A2A12)	(109251-01)		
41	S647	3	DISCRETE I/O INTERFACE OPTION 5: ALT. MASK BIT (12) OPTION 9: EXTERNAL DEVICE CODE	A2A13	110598-01	--	B/O
(41A)	(S522)	(3)	RELAY I/O INTERFACE OPTION 5: ALT. MASK BIT (12) OPTION 9: EXTERNAL DEVICE CODE	(A2A13)	(109251-01)		
42	S647	3	DISCRETE I/O INTERFACE OPTION 5: ALT. MASK BIT (12) OPTION 9: EXTERNAL DEVICE CODE	A2A14	110598-01	--	B/O
(42A)	(S522)	(3)	RELAY I/O INTERFACE OPTION 5: ALT. MASK BIT (12) OPTION 9: EXTERNAL DEVICE CODE	(A2A14)	(109251-01)		
43	5623	3	I/O TESTER MODULE	A2A15	100791-01		
44	3563	3	I/O BUS REPEATER	A2A16	100389-01		

Note: Items in parenthesis are shipped in place of the items they are preceded by.

TABLE 1-3
GLCM SATELLITE COMPUTER SYSTEM
EQUIPMENT SUPPLIED

TABLE 1-2 INDEX NO.	MODEL NO.	ASSY LEVEL	DESCRIPTION	REF. DESIG.	PART NO.	REV	SERIAL NO
			CABLE ASSEMBLIES				
45		2	POWER CABLE - DC 6'	W1	105792-02		
46		2	POWER CABLE - DC 6'	W2	105792-02		
47		2	SINGLE I/O BUS CABLE 6'	W3	106816-02		
48	S586	2	NUCLEAR EXT. CABLE	W4	109778-01		
49		2	ANCILLARY EQUIPMENT KIT	--	110930-01		

APPLICATION		REVISIONS			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
	1602B/D	A	RELEASE PER ER 1602B/D-03	3/9/81	
		A/R1	REVISED PER ECO 7337	5/20/81	

NOTES

1. TIE MOTHERBOARD PINS J1-1, 13, 34, 53 INDIVIDUALLY TO NEAREST MOTHERBOARD GROUND.
2. TWIST GROUND WIRE AROUND SIGNAL WIRES - 2 TWISTS PER INCH.
3. TIE WRAP WIRES 186-208 IN A SEPARATE BUNDLE FROM 209-258.
4. MORE THAN 1 WIRE USED IN THIS PIN.
5. TIE WRAP WIRES 259-281 IN A SEPARATE BUNDLE FROM 282-330.
6. TIE MOTHERBOARD PINS J1-15, 17, 19, 21 INDIVIDUALLY TO NEAREST MOTHERBOARD GROUND.
7. TIE THIS PIN INDIVIDUALLY TO NEAREST M/B GND.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33
A	A	A	A	A	A	A	A	A	A	A	A	A	A																			

RECORD OF REVISION STATUS OF EACH SHEET

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES

DECIMALS ANGLES
2 PLACE ± ±
3 PLACE ±

MATERIAL

CONTR NO.

DR	DATE
R. Post	
CHK	
APPD	
APPD	3-9-81
ACCPD	3-1-81

ROLM MIL-SPEC Computers

4900 OLD IRONSIDES DRIVE
SANTA CLARA, CA. 95050

WIRE LIST, 1602B/D PROCESSOR
MOTHER BOARD ASSEMBLY

SIZE	CODE IDENT NO.	DWG NO.
A	14345	WL-110531

SHEET 1 OF 14

NO.	FROM	TO	FUNCTION	COLOR	GA	LGTH	ITEM	REMARKS
1	A3J2-25	A4J2-25	-12V		26	AR	31	
2	A4J2-25	A5J2-25	-12V		26	AR	31	
3	A5J2-25	A6J2-25	-12V		26	AR	31	
4	A6J2-25	A7J1-25	-12V		26	AR	31.	
5	A7J2-25	A1E19	-12V		26	AR	31	
7	A3J2-27	A4J2-27	+12V		26	AR	31	
8	A4J2-27	A5J2-27	+12V		26	AR	31	
9	A5J2-27	A6J2-27	+12V		26	AR	31	
10	A6J2-27	A7J2-27	+12V		26	AR	31	
11	A7J2-27	A1E20	+12V		26	AR	31	
13	A1J2-4	A2J2-5	DCHPIN/OUT		26	AR	31	
14	A2J2-4	A3J2-5	DCHPIN/OUT		26	AR	31	
15	A3J2-4	A4J2-5	DCHPIN/OUT		26	AR	31	
16	A4J2-4	A5J2-5	DCHPIN/OUT		26	AR	31	
17	A5J2-4	A6J2-5	DCHPIN/OUT		26	AR	31	
18	A6J2-4	A7J1-5	DCHPIN/OUT		26	AR	31	
19	A7J2-4	A7J2-3	DCHPIN/GND		26	AR	31	
20	A1E25	A1J2-5	DCHPOUT		26	AR	31	
22	A1J2-48	A2J2-42	INTPIN/OUT		26	AR	31	
23	A2J2-48	A3J2-42	INTPIN/OUT		26	AR	31	
24	A3J2-48	A4J2-42	INTPIN/OUT		26	AR	31	
25	A4J2-48	A5J2-42	INTPIN/OUT		26	AR	31	
26	A5J2-48	A6J2-42	INTPIN/OUT		26	AR	31	
27	A6J2-48	A7J2-42	INTPIN/OUT		26	AR	31	
28	A7J2-48	A8J2-55	INTPIN/OUT		26	AR	31	
29	A8J2-60	A8J2-3	INTPIN/GND		26	AR	31	
30	A1E24	A1J2-42	INTPOUT		26	AR	31	

NOTES:

SIZE	CODE IDENT NO.	DWG NO.
A	14345	WL-110531
SCALE	REV A	SHEET 2 OF

NO.	FROM	TO	FUNCTION	COLOR	GA	LGTH	ITEM	REMARKS
38	J1-1	A8J2-70	+5V	BLK	26	A/R	31	
39	J1-2	A8J2-43	RDR RUN	ORN	26	A/R	31	
40	J1-3	A8J1-58	TT IN	WHT/GRA	26	A/R	31	
41	J1-4	A8J2-59	-12V	WHT	26	A/R	31	
42	J1-5		SPARE		26	A/R	31	
43	J1-6	A8J2-69	TT OUT	WHT	26	A/R	31	
44	J1-7	A8J2-67	+V	VIO	26	A/R	31	
45	J1-8	A8J2-47	$\overline{\text{STOP 2 ENABLE}}$	VIO	26	A/R	31	
46	J1-9	A8J2-63	GND	ORN	26	A/R	31	
47	J1-10	CHASSIS	CHASSIS GND	BLK	24	3	30,25	
48	J1-41	CHASSIS	CHASSIS GND	BLK	24	3	30,25	
49	J1-42	A8J1-8	GND	GRA	26	A/R	31	
50	J1-43	A8J1-2	CONTROL	RED	26	A/R	31	
51	J1-44	A8J1-4	STOP	YEL	26	A/R	31	
52	J1-45	A8J1-3	$\overline{\text{RDR RDY}}$	ORN	26	A/R	31	
53	J1-46	A8J1-5	FWD	GRN	26	A/R	31	
54	J1-47	A8J1-1	SPKT	BRN	26	A/R	31	
55	J1-48	A8J1-6	RDR 0	BLU	26	A/R	31	
56	J1-49	A8J1-7	RDR 1	VIO	26	A/R	31	
57	J1-50	A8J1-9	RDR 2	WHT	26	A/R	31	
58	J1-51	A8J1-10	RDR 3	WHT/BLK	26	A/R	31	
59	J1-52	A8J1-12	RDR 4	WHT/RED	26	A/R	31	
60	J1-53	A8J1-14	RDR 5	WHT/YEL	26	A/R	31	
61	J1-54	A8J1-16	RDR 6	WHT/BLU	26	A/R	31	
62	J1-55	A8J1-18	RDR 7	WHT/GRA	26	A/R	31	
63	J1-16	A9J2-38	$\overline{\text{P BOOT}}$	WHT	26	A/R	31	
64	J1-17	A9J2-39	$\overline{\text{P BOOT RET}}$	WHT	26	A/R	31	
65	J1-18	A9J2-69	$\overline{\text{BITE}}$	WHT	26	A/R	31	
66	J1-19	A9J2-67	$\overline{\text{BITE RET}}$	WHT	26	A/R	31	

NOTES:
WIRING FOR 1642

SIZE	CODE IDENT NO.	DWG NO.
A	14345	WL-110531
SCALE	REV A	SHEET 3 OF

ABR143

NO.	FROM	TO	FUNCTION	COLOR	GA	LGTH	ITEM	REMARKS
75	J2-1	A3J1-1		BRN	26	AR	31	[1]
76	J2-2	A3J1-2		RED	26			
77	J2-3	A3J1-3		ORN	26			
78	J2-4	A3J1-4		YEL	26			
79	J2-5	A3J1-5		GRN	26			
80	J2-6	A3J1-6		BLU	26			
81	J2-7	A3J1-7		VIO	26			
82	J2-8	A3J1-8		GRA	26			
83	J2-9	A3J1-9		WHT	26			
84	J2-10	A3J1-10		BLK	26			
85	J2-11	A3J1-11		WHT/BRN	26			
86	J2-12	A3J1-12		WHT/RED	26			
87	J2-13	A3J1-13		WHT/ORN	26			[1]
88	J2-14	A3J1-14		WHT/YEL	26			
89	J2-15	A3J1-15		WHT/GRN	26			
90	J2-16	A3J1-16		WHT/BLU	26			
91	J2-17	A3J1-17		WHT/VIO	26			
92	J2-18	A3J1-18		WHT/GRA	26			
93	J2-19	A3J1-19		WHT	26			
94	J2-20	A3J1-20		BLK	26			
95	J2-21	A3J1-21		BRN	26			
96	J2-22	A3J1-22		RED	26			
97	J2-23	A3J1-23		ORN	26			
98	J2-24	A3J1-24		YEL	26			
99	J2-25	A3J1-25		GRN	26			
100	J2-26	A3J1-26		BLU	26			
101	J2-27	A3J1-27		VIO	26			
102	J2-28	A3J1-28		GRA	26			
103	J2-29	A3J1-29		WHT	26			
104	J2-30	A3J1-30		BLK	26			
105	J2-31	A3J1-31		WHT/BRN	26			
106	J2-32	A3J1-32		WHT/RED	26			
107	J2-33	A3J1-33		WHT/ORN	26			
108	J2-34	A3J1-34		WHT/YEL	26			[1]
109	J2-35	A3J1-35		WHT/GRN	26			
110	J2-36	A3J1-36		WHT/BLU	26			
111	J2-37	A3J1-37		WHT/VIO	26	AR	31	

NOTES:

SIZE	CODE IDENT NO.	DWG NO.
A	14345	WL-110531
SCALE	REV A	SHEET 4 OF

ABR143

NO.	FROM	TO	FUNCTION	COLOR	GA	LGTH	ITEM	REMARKS
112	J2-38	A3J1-38		WHT/GRA	26	AR	31	
113	J2-39	A3J1-39		WHT	26			
114	J2-40	A3J1-40		BLK	26			
115	J2-41	A3J1-41		BRN	26			
116	J2-42	A3J1-42		RED	26			
117	J2-43	A3J1-43		ORN	26			
118	J2-44	A3J1-44		YEL	26			
119	J2-45	A3J1-45		GRN	26			
120	J2-46	A3J1-46		BLU	26			
121	J2-47	A3J1-47		VIO	26			
122	J2-48	A3J1-48		GRA	26			
123	J2-49	A3J1-49		WHT	26			
124	J2-50	A3J1-50		BLK	26			
125	J2-51	A3J1-51		WHT/BRN	26			
126	J2-52	A3J1-52		WHT/RED	26			
127	J2-53	A3J1-53		WHT/ORN	26			1
128	J2-54	A3J1-54		WHT/YEL	26	AR	31	
129	J2-55	CHASSIS	CHASSIS GND	BLK	24	3"	30,25	

NOTES:

SIZE	CODE IDENT NO.	DWG NO.
A	14345	WL-110531
SCALE	REV A	SHEET 5 OF

NO.	FROM	TO	FUNCTION	COLOR	GA	LGTH	ITEM	REMARKS
149	J5-A	A4J1-25	DATA+			AR	33	
150	SHIELD	A4J1-32	DATA-					
151	J5-B	A5J1-25	DATA+			AR	33	
152	SHIELD	A5J1-32	DATA-					
153	J5-E	A4J1-8	SRIN+			AR	33	
154	SHIELD	A4J1-10	SRIN-					
155	J5-D	A4J1-36	SROUT+			AR	33	
156	SHIELD	A4J1-40	SROUT-					
157	A5J1-1	[1]	GND	WHT	26	AR	31	
158	A5J1-13	[1]	GND	WHT	26	AR	31	
159	A5J1-34	[1]	GND	WHT	26	AR	31	
160	A5J1-53	[1]	GND	WHT	26	AR	31	
161	A4J1-1	[1]	GND	WHT	26	AR	31	
162	A4J1-13	[1]	GND	WHT	26	AR	31	
163	A4J1-34	[1]	GND	WHT	26	AR	31	
164	A4J1-53	[1]	GND	WHT	26	AR	31	
165	J5-F	A4J1-53	REF GND		20	AR	39,40,41	
166	A4J1-12	A6J1-12	$\overline{\text{PBUS}}$		26	AR	31	
167	A4J1-14	A6J1-14	SBUS		26	AR	31	
168	A4J1-3	A4J1-4	$\overline{\text{SL1}}$		26	AR	31	
169	A4J1-5		$\overline{\text{SL2}}$		26	AR	31	S530 A1
170	A4J1-15	A4J1-16	$\overline{\text{SL4}}$		26	AR	31	D.C. 32

NOTES:

SIZE	CODE IDENT NO.	DWG NO.
A	14345	WL-110531
SCALE	REV A	SHEET 6 OF

NO.	FROM	TO	FUNCTION	COLOR	GA	LGTH	ITEM	REMARKS
186	J6-1	A1J1-33	$\overline{\text{BDATA2}}$	WHT/ORN	26	AR	31	
187	J6-2	A1J1-37	$\overline{\text{BDATA1}}$	WHT/VIO	26	AR	31	
188	J6-5	A1J1-23	$\overline{\text{BDATA7}}$	ORN	26	AR	31	
189	J6-6	A1J1-29	$\overline{\text{BDATA6}}$	WHT	26	AR	31	
190	J6-12 [4]	A1J1-21	GND	BLK	30	AR	32	[6] [2]
192	J6-12 [4]	A1J1-21	GND	BLK	30	AR	32	[6] [2]
193	J6-4	A1J1-34	$\overline{\text{BDATA8}}$	WHT/YEL	26	AR	31	
194	J6-10	A1J1-32	$\overline{\text{BDATA13}}$	WHT/RED	26	AR	31	
195	J6-11	A1J1-26	$\overline{\text{BDATA12}}$	BLU	26	AR	31	
196	J6-20	A1J1-24	$\overline{\text{BDATA15}}$	YEL	26	AR	31	
198	J6-3	A1J1-35	$\overline{\text{BDATA0}}$	WHT/GRN	26	AR	31	
199	J6-9	A1J1-27	$\overline{\text{BDATA3}}$	VIO	26	AR	31	
200	J6-15	A1J1-36	$\overline{\text{BDATA10}}$	WHT/BLU	26	AR	31	
201	J6-16	A1J1-30	$\overline{\text{BDATA9}}$	BLK	26	AR	31	
202	J6-14 [4]	A1J1-21	GND	BLK	30	AR	32	[6] [2]
204	J6-14 [4]	A1J1-21	GND	BLK	30	AR	32	[6] [2]
205	J6-7	A1J1-25	$\overline{\text{BDATA5}}$	GRN	26	AR	31	
206	J6-8	A1J1-31	$\overline{\text{BDATA4}}$	WHT/BRN	26	AR	31	
207	J6-13	A1J1-38	$\overline{\text{BDATA11}}$	WHT/GRA	26	AR	31	
208	J6-21	A1J1-28	$\overline{\text{BDATA14}}$	GRA	26	AR	31	
	********** BUNDLE DIVISION ********** [3] **********							
209	J6-40	A1J1-42	BDCH0	RED	26	AR	31	
210	J6-33 [4]	A1J1-19	GND	BLK	30	AR	32	[6]
212	J6-33 [4]	A1J1-19	GND	BLK	30	AR	32	[6] [2]
213	J6-18	A1J1-43	$\overline{\text{BDS3}}$	ORN	26	AR	31	
214	J6-19	A1J1-41	$\overline{\text{BDS4}}$	BRN	26	AR	31	
215	J6-27	A1J1-45	$\overline{\text{BDS1}}$	GRN	26	AR	31	
216	J6-28	A1J1-6	$\overline{\text{BDCHPOUT}}$	BLU	26	AR	31	
217	J6-41	A1J1-8	$\overline{\text{BINTR}}$	GRA	26	AR	31	
218	J6-47	A1J1-44	$\overline{\text{BRQENB}}$	YEL	26	AR	31	
219	J6-48	A1J1-16	$\overline{\text{BDCHMI}}$	WHT/BLU	26	AR	31	
220	J6-35	A1J1-4	$\overline{\text{BINTPIN}}$	YEL	26	AR	31	

NOTES:

SIZE	CODE IDENT NO.	DWG NO.
A	14345	WL-110531
SCALE	REV A	SHEET 7 OF

NO.	FROM	TO	FUNCTION	COLOR	GA	LGTH	ITEM	REMARKS
222	J6-25	A1J1-10	$\overline{\text{BSELD}}$	BLK	26	AR	31	
223	J6-26	A1J1-52	BDATOA	WHT/RED	26	AR	31	
224	J6-32	A1J1-20	BDATOC	BLK	26	AR	31	
225	J6-34	A1J1-53	BDATOB	WHT/ORN	26	AR	31.	
226	J6-33 [4]	A1J1-19	GND	BLK	26	AR	32	[6] [2]
228	J6-36	A1J1-11	BDCHPIN	WHT/BRN	26	AR	31	
229	J6-30	A1J1-1	BDATIA	BRN	26	AR	31	
230	J6-31	A1J1-3	BDATIC	ORN	26	AR	31	
231	J6-37	A1J1-5	BDATIB	GRN	26	AR	31	
232	J6-39	A1J1-12	$\overline{\text{BSELB}}$	WHT/RED	26	AR	31	
233	J6-38 [4]	A1J1-17	GND	BLK	30	AR	32	[6] [2]
235	J6-38 [4]	A1J1-17	GND	BLK	30	AR	32	[6] [2]
236	J6-22	A1J1-51	$\overline{\text{BDS5}}$	WHT/BRN	26	AR	31	
237	J6-23	A1J1-47	$\overline{\text{BDS2}}$	VIO	26	AR	31	
238	J6-24	A1J1-13	$\overline{\text{BINTPOUT}}$	WHT/ORN	26	AR	31	
239	J6-29	A1J1-49	$\overline{\text{BDSØ}}$	WHT	26	AR	31	
240	J6-45	A1J1-18	$\overline{\text{BDCHR}}$	WHT/GRA	26	AR	31	
241	J6-46	A1J1-9	$\overline{\text{DDCHA}}$	WHT	26	AR	31	
242	J6-51	A1J1-14	$\overline{\text{BDCHMØ}}$	WHT/YEL	26	AR	31	
244	J6-38 [4]	A1J1-15	GND	BLK	30	AR	32	[6]
245	J6-52	A1J1-7	$\overline{\text{BDCHI}}$	VIO	26	AR	31	
247	J6-42	A1J1-40	BIOPLS	BLK	26	AR	31	
248	J6-49	A1J1-39	BSTRT	WHT	26	AR	31	
249	J6-50	A1J1-48	BCLR	GRA	26	AR	31	
250	J6-54	A1J1-22	BOVFLO	RED	26	AR	31	
251	J6-43 [4]	A1J1-15	GND	BLK	30	AR	32	[6] [2]
253	J6-43 [4]	A1J1-15	GND	BLK	30	AR	32	[6] [2]
254	J6-44	A1J1-50	$\overline{\text{BIORST}}$	BLK	26	AR	31	
255	J6-53	A1J1-46	$\overline{\text{BMSKO}}$	BLU	26	AR	31	
256	J6-55	A1J1-54	BINTA	WHT/YEL	26	AR	31	
257	J6-17	CHASSIS	CHASSIS GND	BLK	24	3"	30,25	

NOTES:

SIZE	CODE IDENT NO.	DWG NO.
A	14345	WL-110531
SCALE	REV A	SHEET 8 OF

NO.	FROM	TO	FUNCTION	COLOR	GA	LGTH	ITEM	REMARKS
259								
260								
261								
262								
263								
265								
266								
267								
268								
269								
271								
272								
273								
274								
275								
277								
278								
279								
280								
281								
282								
283								
285								
286								
287								
288								
289								
290								
291								
292								
293								

NOTES:

SIZE	CODE IDENT NO.	DWG NO.
A	14345	WL-110531
SCALE	REV A	SHEET 9 OF

NO.	FROM	TO	FUNCTION	COLOR	GA	LGTH	ITEM	REMARKS
295								
296								
297								
298								
299								
301								
302								
303								
304								
305								
306								
308								
309								
310								
311								
312								
313								
314								
315								
317								
318								
320								
321								
322								
323								
324								
326								
327								
328								
329								
330								

NOTES:

SIZE	CODE IDENT NO.	DWG NO.
A	14345	WL-110531
SCALE	REV A	SHEET 10 OF

A8R143

NO.	FROM	TO	FUNCTION	COLOR	GA	LGTH	ITEM	REMARKS
332	J8-A	A6J1-25	DATA+			AR	33	
333	SHIELD	A6J1-32	DATA-			AR		
334	J8-B	A7J1-25	DATA+			AR	33	
335	SHIELD	A7J1-32	DATA-			AR		
336	J8-E	A6J1-8	SRIN+			AR	33	
337	SHIELD	A6J1-10	SRIN-			AR		
338	J8-D	A6J1-36	SROUT+			AR	33	
339	SHIELD	A6J1-40	SROUT-			AR		
340	A6J1-1	[1]	GND	WHT	26	AR	31	
341	A6J1-13	[1]	GND	WHT	26	AR	31	
342	A6J1-34	[1]	GND	WHT	26	AR	31	
343	A6J1-53	[1]	GND	WHT	26	AR	31	
344	A7J1-1	[1]	GND	WHT	26	AR	31	
345	A7J1-13	[1]	GND	WHT	26	AR	31	
346	A7J1-34	[1]	GND	WHT	26	AR	31	
347	A7J1-53	[1]	GND	WHT	26	AR	31	
348	J8-F	A6J1-53	REF GND		20	AR	39,40,41	
349	A6J1-3	A6J1-4	$\overline{SL1}$	WHT	26	AR	31	
350	A6J1-5		$\overline{SL2}$	WHT	26	AR	31	S530 A1
351	A6J1-15	A6J1-16	$\overline{SL4}$	WHT	26	AR	31	DC 33
352	A6J1-17	A6J1-18	$\overline{SL5}$	WHT	26	AR	31	

NOTES:

SIZE	CODE IDENT NO.	DWG NO.
A	14345	WL-110531
SCALE	REV A	SHEET 11 OF

ABR143

NO.	FROM	TO	FUNCTION	COLOR	GA	LGTH	ITEM	REMARKS
369	J9-1	E29-2A	PBØ	BROWN	26	18"	31	
370	J9-6	E29-2B	PBØ RET	RED				
371	J9-2	E29-2C	PB1	ORANGE				
372	J9-7	E29-2D	PB1 RET	YELLOW				
373	J9-3	E29-3A	PB2	BROWN				
374	J9-8	E29-3B	PB2 RET	RED				
375	J9-4	E29-3C	PB3	ORANGE				
376	J9-5	E29-3D	PB3 RET	YELLOW				
377	J9-9	E29-4A	PB4	BROWN				
378	J9-16	E29-4B	PB4 RET	RED				
379	J9-10	E29-4C	PB5	ORANGE				
380	J9-11	E29-4D	PB5 RET	YELLOW				
381	J9-12	E29-5A	PB6	BROWN				
382	J9-13	E29-5B	PB6 RET	RED				
383	J9-14	E29-5C	PB7	ORANGE				
384	J9-15	E29-5D	PB7 RET	YELLOW				
385	J9-17	E29-6A	PB8	BROWN				
386	J9-18	E29-6B	PB8 RET	RED				
387	J9-19	E19-6C	PB9	ORANGE				
388	J9-20	E19-6D	PB9 RET	YELLOW				
389	J9-21	E29-7A	PB1Ø	BROWN				
390	J9-22	E29-7B	PB1Ø RET	RED				
391	J9-23	E29-7C	PB11	ORANGE				
392	J9-24	E29-7D	PB11 RET	YELLOW				
393	J9-25	E29-8A	PB12	BROWN				
394	J9-32	E29-8B	PB12 RET	RED				
395	J9-26	E29-8C	PB13	ORANGE				
396	J9-27	E29-8D	PB13 RET	YELLOW				
397	J9-28	E29-9A	PB14	BROWN				
398	J9-29	E29-9B	PB14 RET	RED				
399	J9-30	E29-9C	PB15	ORANGE				
400	J9-31	E29-9D	PB15 RET	YELLOW				
401	J9-33	E29-1A	PRST	BROWN				
402	J9-34	E29-1B	PRST RET	RED				
403	J9-35	E29-1C	PSTP	ORANGE				
404	J9-36	E29-1D	PSTP RET	YELLOW				
405	J9-37	E29-13A	PRQ	BROWN	26	18"	31	TWIST WITH WIRE NO. 406

NOTES:

SIZE	CODE IDENT NO.	DWG NO.
A	14345	WL-110531
SCALE	REV A	SHEET 12 OF

NO.	FROM	TO	FUNCTION	COLOR	GA	LGTH	ITEM	REMARKS
406	J9-38	E29-13B	PRQ RET	RED	26	18"	31	TWIST WITH WIRE N0405
407	J9-40	E29-10A	PMST	BROWN				
408	J9-41	E29-10B	PMST RET	RED				
409	J9-42	E29-10C	PDST	ORANGE				
410	J9-43	E29-10D	PDST RET	YELLOW				
411	J9-44	E29-12A	PCLR	BROWN				
412	J9-45	E29-12B	PCLR RET	RED				
413	J9-46	E29-12C	PRUN	ORANGE				
414	J9-47	E29-11C	PSELØ	ORANGE				
415	J9-48	E29-11D	PSELØ RET	YELLOW				
416	J9-49	E29-11A	PSEL1	BROWN				
417	J9-53	E29-11B	PSEL1 RET	RED				
418	J9-50	E29-13C	PINT	ORANGE				
419	J9-54	E29-13D	PINT RET	YELLOW				
420	J9-51	E29-14A	PDMA	BROWN				
421	J9-55	E29-14B	PDMA RET	RED				
422	J9-52	E29-14C	PANF	ORANGE	26	18"	31	
423	J9-39	CHASSIS	CHASSIS GND	BLACK	24	3"	30,25	

NOTES:

SIZE	CODE IDENT NO.	DWG NO.
A	14345	WL-110531
SCALE	REV A	SHEET 13 OF

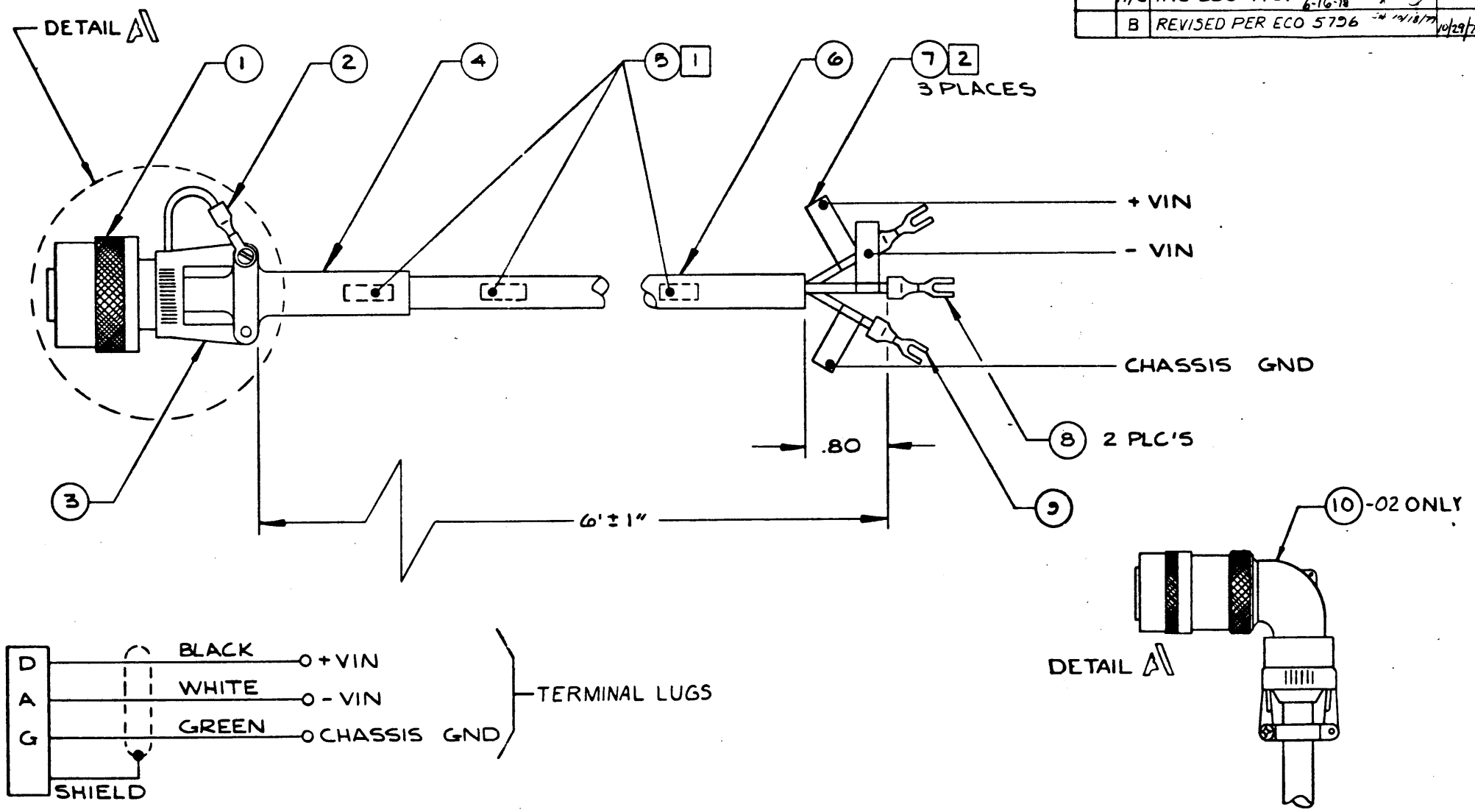
NO.	FROM	TO	FUNCTION	COLOR	GA	LGTH	ITEM	REMARKS
443	A9J2-69	A10J2-6	$\overline{FF7}$	WHT	26	AR	31	S565
444	A9J1-5	A10J1-4	+50K	WHT	26	AR	31	
445	A10J1-2	J21-1	GND					
446	A10J1-54	J2-11	GND					
447	A10J2-4	J21-12	+12V					
448	A10J2-50	J21-13	$\overline{DETF}$					
449	A9J1-5	J21-14	$\overline{NRST}$					
450	A10J2-10	J21-15	EFRST					
451	A10J2-4	J21-21	+12V					S585
452	A8J2-33	J21-9	-12V					
453	A10J1-40	J21-2	HAR +5V					
454		J21-10	HAR +5V					
455	J4-54	7	M/B GND					
456	J4-55	CHASSIS	CHASSIS GND					
457	A2J1-43	A2J1-44	SEL 0	WHT	26	AR	31	
458	A2J1-45	A2J1-46	SEL 2	WHT	26	AR	31	S422A
459	A2J1-49	A2J1-50	SEL 4	WHT	26	AR	31	DC-5
460	J7-1	A2J1-1	GND 7	BRN	26	AR	31	
461	J7-2	A2J1-2	UP DATA	RED	26	AR	31	
462	J7-3	A2J1-3	$\overline{UP\ DATA}$	ORN	26	AR	31	
463	J7-6	A2J1-6	ENB	BLU	26	AR	31	
464	J7-7	A2J1-7	$\overline{ENB}$	VIO	26	AR	31	
465	J7-10	A2J1-10	UP CLK	BLK	26	AR	31	
466	J7-11	A2J1-11	$\overline{UP\ CLK}$	WHT/BRN	26	AR	31	S422A
467	J7-13	A2J1-13	GND 7	WHT/ORN	26	AR	31	
468	J7-15	A2J1-15	DN DATA	WHT/GRN	26	AR	31	
469	J7-16	A2J1-16	$\overline{DN\ DATA}$	WHT/BLU	26	AR	31	
470	J7-34	A2J1-34	GND 7	WHT/YEL	26	AR	31	
471	J7-53	A2J1-53	GND 7	WHT/ORN	26	AR	31	
472	J7-55	CHASSIS	CHASSIS GND	BLK	24	AR	30	
473	J7-40	J4-7	GND LINK	WHT	26	AR	31	MIU WIRING
474								
475								
476								
477								
478								
479								

NOTES:

SIZE	CODE IDENT NO.	DWG NO.
A	14345	WL-110531
SCALE	REV A	SHEET 14 OF

10-105792

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	INITIAL ISSUE	10-6-77	
	R/C	INC ECO 4907 PJT 6-16-78	6-22-78	
	B	REVISED PER ECO 5756	10/29/79	



NOTES:

1. LABEL PER MP-000367 USING ITEM 5.
2. MARK WIRE FUNCTIONS AS SHOWN, USING ITEM 7.

SEE SEPARATE PARTS LIST

QTY REQ'D	KEY	CODE IDENT	PART OR IDENTIFYING NO.		NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.

PARTS LIST

-01, -02 SHOWN

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES

ANGLES ±
DECIMALS
2 PLACE ± .20
3 PLACE ±

SURFACES √ MICRO-INCHES

MATERIAL

	DR	DATE
	Tim Weekes	3 OCT 77
CHK	M. Tam	10/11/77
APPD	[illegible]	12-9-77
ACCPD		

ROLM CORPORATION ■ SANTA CLARA, CALIFORNIA

DC POWER CABLE ASSEMBLY

SIZE	CODE IDENT		REV
C	14345	10-105792	B

SCALE NONE SHEET 1 OF 1

NEXT ASSY	USED ON
	3879

APPLICATION

ROLM CORPORATION ■ VALLCO PARK CUPERTINO, CALIFORNIA

PL 105792-02		B
CODE IDENT **14345**	SHEET 1 OF 2	REV

CONTR NO	PREP L. CANGIAMILLA DATE 10/23/79	DC POWER CABLE ASSEMBLY
PROJECT NUMBER	CHK W J Franks 10/23/79	
	APPD	
	ACCPD	

SYM	REVISION DESCRIPTION	DATE	APPROVED
B	INC ECO 5796 SH 10-17-79	10/29/79	INIS G. VANREMOORTEL

SYM	REVISION DESCRIPTION	DATE	APPROVED
	NOTES: 1. -01 Standard -02 Option 80		

B	B																																									
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42

RECORD OF REVISION STATUS OF EACH SHEET

MODEL 3879

PL 105792-02

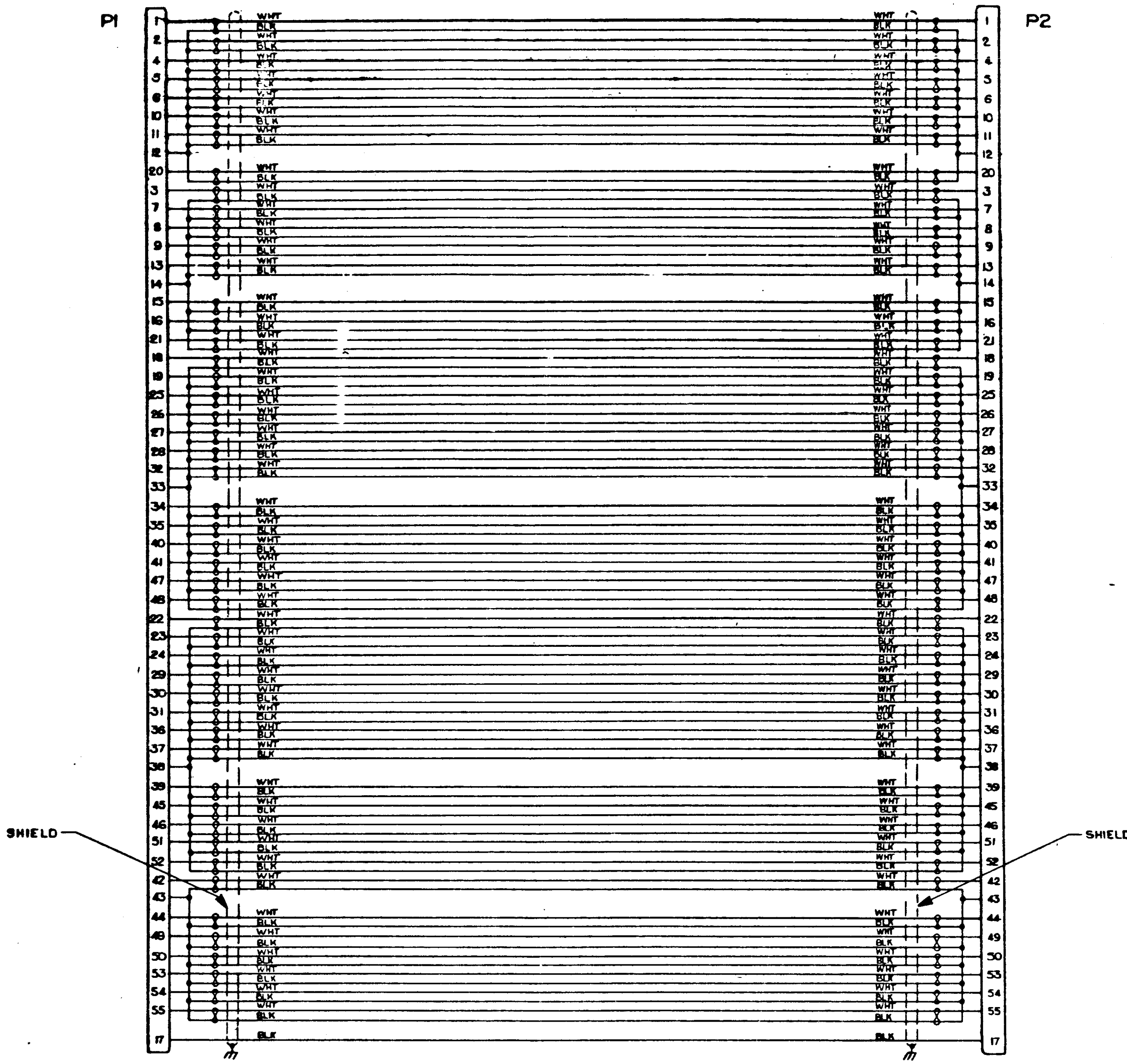
QTY	UM	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	ITEM NO
REF		14345	10-105792	DC POWER CABLE ASSY DWG		0
1		06324	MS3456L18-9S	CONNECTOR	P1	1
1		96906	MS25036-148	TERMINAL LUG, #4, RING, INSULATED, RED		2
1		02660	9779-513-8	RUBBER BUSHING		4
3		59730	WSLM35	LABEL		5
AR		14345	106065-01	CABLE, 12 GA, 3 COND, BLK, WHT, GRN		6
3		59730	WC-WHID	LABEL		7
2		00779	52430	TERMINAL LUG, #6, SPADE, INSULATED, YELLOW		8
1		00779	52420	TERMINAL LUG, #6, SPADE, INSULATED, BLUE		9
1		06324	G5602-185M	BACKSHELL, 90 DEG. LIGHTWEIGHT ELBOW ASSEMBLY		10
AR		29005	EXE16-19/29	WIRE, 16 AWG, TYPE-E-PER-MIL-W-16878D/4		11

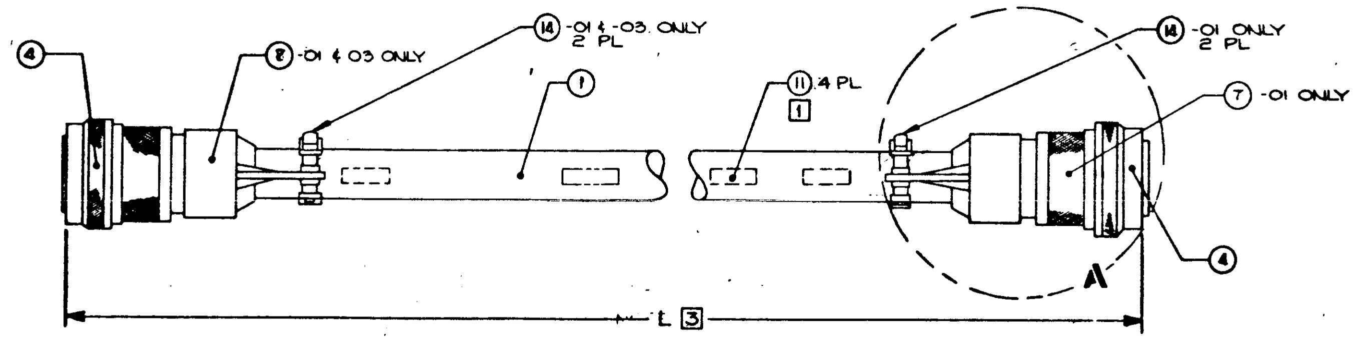
		PL 105792-02	B
		CODE IDENT 14345 SHEET 2 of 2	REV

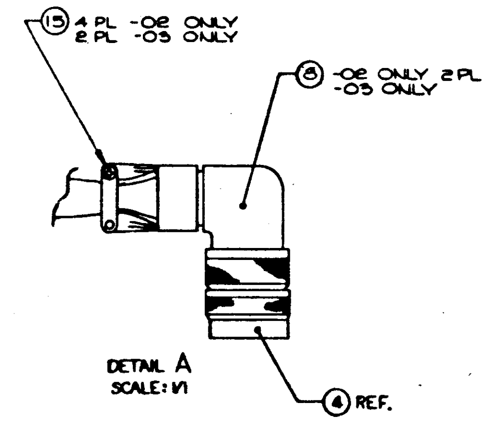
10-106816

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	INITIAL ISSUE	3-20-78	
	A/A	REVISED PER ECO 5981		







DETAIL A
SCALE: 1/1

NOTES:

1. [1] CABLE TO BE IDENTIFIED PER MP-000567 USING ITEM 11.
2.
3. [3] LENGTH WILL APPEAR ON PRODUCTION RELEASE.
4.
5.
6. WHERE 3 OR MORE WIRES TERMINATE AT A SINGLE PIN, USE ITEM 16 TO GROUP WIRES.

PARTS LIST

-01, -02, -03 SHOWN & NOTED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES: DECIMALS 2 PLACE ± .50

GEN'L USAGE

ROLM CORPORATION — SANTA CLARA, CALIFORNIA

SINGLE CABLE I/O BUS CABLE ASSEMBLY

SIZE E | CODE IDENT 14345 | 10-106816 | REV A

SCALE NONE

ROLM CORPORATION ■ VALLCO PARK CUPERTINO, CALIFORNIA

PL 106816-02	A/R3
CODE IDENT 14345	SHEET 1 OF 2	REV

CONTR NO	PREP K. MOSTAD DATE 2/16/78	SINGLE CABLE I/O BUS ASSEMBLY (MIL-C-38999)
PROJECT NUMBER	CHK 2-21-78	
	APPD Dick Cheung 3/15/78	
	ACCPD	

SYM	REVISION DESCRIPTION	DATE	APPROVED
A	INITIAL ISSUE	3-20-78	Hardridge
R/C	INC ECO 4278 P.J. 4-17-78 5/2/78	5-2-78	
A/R2	REVISED PER ECO 5981 PC 12/20/79	1/25/80	
A/R3	REVISED PER ECO 6593 PC 8/19/8	8-22-80	

SYM	REVISION DESCRIPTION	DATE	APPROVED
	NOTES: 1. -01 STRAIGHT -02 2 EA. 90° -03 1 EA. STRAIGHT 1 EA. 90°		

A	A																																								
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42

RECORD OF REVISION STATUS OF EACH SHEET

NEXT ASSY: TOP ASSY

MODEL GEN USAGE

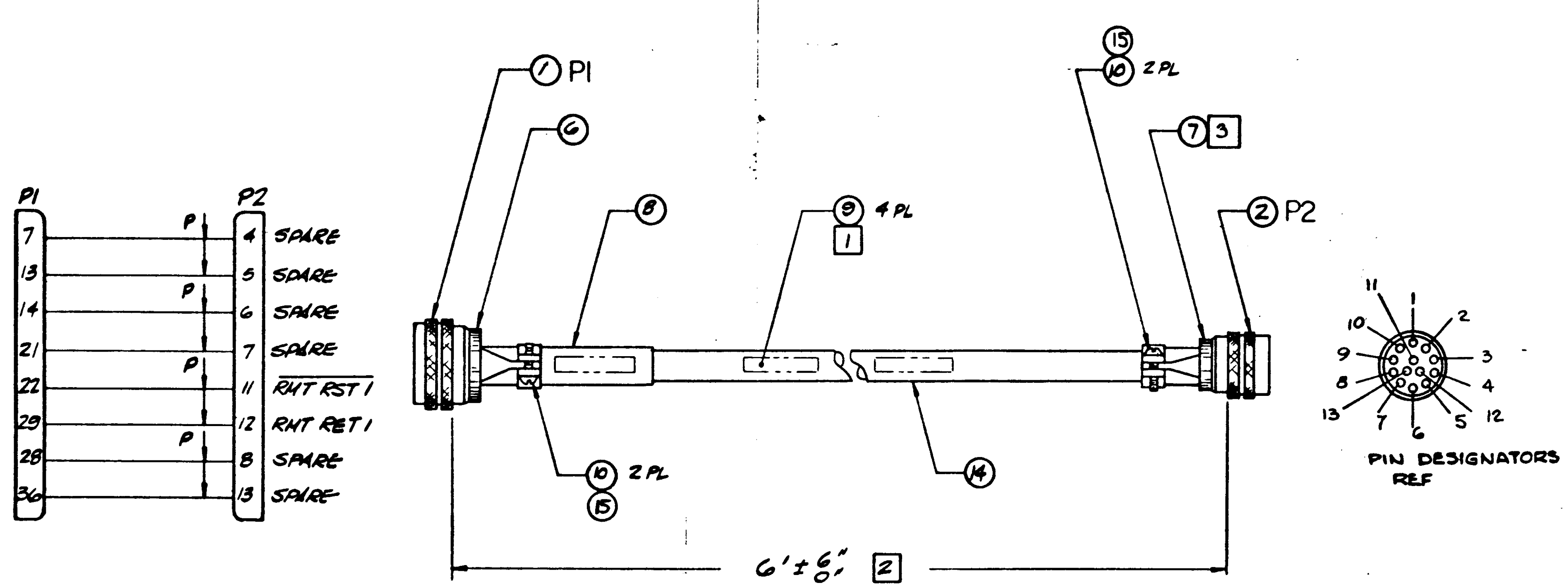
PL 106816-02

QTY	UM	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	ITEM NO
REF		14345	10-106816	SINGLE CABLE I/O BUS CABLE ASSEMBLY DRAWING		0
AR		14345	10320S-01	CABLE, 57 TWISTED PAIRS		1
2		96906	MS27473T16F35P	CONNECTOR, 55 CONTACTS		4
2		07418	SE57F1512ASE-12R	BACKSHELL, RIGHT ANGLE, ENTRY 12		8
4		59730	WSLM35	LABEL		11
4		96906	MS51957-47	SCREW, PAN HEAD, 8-32 X .750		15
10		C6090	D144-01	SOLDER SLEEVE, .20 DIA		16
AR		29005	EXE24-19/36	WIRE, 24 AWG, TYPE-E-PER-MIL-W-16878D/4		17

		PL 106816-02	A/R3
		CODE IDENT 14345 SHEET 2 of 2	REV

10-109778

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASE PER ER-5586-01		
	A/R	REVISED PER ECO 7196		



NOTES:

1. LABEL PER MP-000367 USING ITEM 9.
2. STANDARD LENGTH AS SHOWN; ADD 1 FT. OF CABLE FOR EACH OPTION 13 ON CUSTOMER ORDER.
3. REMOVE INTEGRAL BOOT
4. PIN LOCATIONS OF 13 PIN CONNECTOR 2 PL

SEE SEPARATE PARTS LIST

QTY REQ'D	KEY	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.

PARTS LIST

-01 SHOWN

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ± — DECIMALS — 2 PLACE ± — 3 PLACE ± —
SURFACES: √ MICRO-INCHES
MATERIAL: —

DR P. M. Ekert — 6 May 80
CHK Y. Usuki — 23 May 80
APPD W. Davis — 3 Jun 80
DEV ENGIN — 19 Jun 80
ACCPD — 15 Jul 80

ROLM MIL-SPEC Computers SANTA CLARA, CA

OPTO RESET CABLE ASSEMBLY

SIZE D | CODE IDENT 14345 | 10-109778 | REV A

SCALE None | SHEET 1 OF 1

NEXT ASSY	USED ON
	5586

APPLICATION

ROLM CORPORATION ■ VALLCO PARK CUPERTINO, CALIFORNIA

PL 109778-01 | CODE IDENT **14345** | SHEET 1 OF 2 | REV A

CONTR NO

PROJECT NUMBER

		DATE
PREP	L. CANGIAMILLA	5/13/80
CHK	Y USUKI	23 MAY 80
APPD	Wm Davis	3 JUNE 80
ACCPD	[illegible]	19 June 80

OPTO RESET
CABLE ASSEMBLY

SYM	REVISION DESCRIPTION	DATE	APPROVED
A	RELEASE PER ER S586-01 WD	7-2[illegible]	[illegible]
A/R1	REVISED PER ECO 7196 [illegible] 3/12/81	4/22/81	G. VANHIMMELER LT.

SYM	REVISION DESCRIPTION	DATE	APPROVED
	-01 SHOWN		

RECORD OF REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
A	A																																								

MODEL S586

PL 109778-01

QTY	KEY	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	ITEM NO.
REF		14345	10-109778	OPTO/RESET CABLE ASSEMBLY DWG		0
1		96906	MS27473T16F35P	CONNECTOR, 55 CONTACTS	P1	1
1		96906	MS27473T10F35P	CONNECTOR, 13 CONTACTS, PLUG	P2	2
1		96906	MS27506F16-2	CABLE CLAMP		6
1		96906	MS27506F10-2	CABLE CLAMP		7
1		02660	9779-513-6	RUBBER BUSHING		8
4		59730	WSLM33	LABEL		9
4		96906	MS51957-29	SCREW, PAN HEAD, 6-32 X .438		10
AR		14345	109725-01	CABLE, 8 TWISTED PAIRS, SHIELDED		14
AR		05972	LOCTITE 222	LIQUID SCREW SEALANT, MILD STRENGTH		15

PL 109778-01 REV A

CODE IDENT 14345 SHEET 2 of 2

APPLICATION		REVISIONS			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
109209-03	GLCM 2107	A	RELEASED PER ER G/SLCM-02		
		A/R1	REVISED PER ECO 7092	2/2/81	

A	A	A																													
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33

RECORD OF REVISION STATUS OF EACH SHEET

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES

DECIMALS
2 PLACE ±
3 PLACE ±

ANGLES ±

MATERIAL

CONTR NO.		
DR		DATE 1/13/81
CHK		
APPD		
APPD		1/9/81
ACCPD		

ROLM MIL-SPEC Computers

4900 OLD IRONSIDES DRIVE
SANTA CLARA, CA. 95050

ANCILLARY EQUIPMENT KIT
(GLCM 2107)

SIZE	CODE IDENT NO.	DWG NO.
A	14345	14-110930

SHEET 1 OF 3

127 – 9.79

1.0 GENERAL

1.1 The items listed on Sheet 3 of this document are to be shipped with each GLCM Satellite Computer System (ROLM P/N 109209-03).

1.2 Each item listed shall be bagged, tagged and marked with Class III markings in accordance with Paragraph 4.7 of Marking Specification 15-109180.

1.3 After all items are individually bagged, bag them all together in a single bag and mark with the following information.

ANCILLARY EQUIPMENT KIT
(GLCM 2107)

ROLM P/N 110930-01 REV. A
QTY: 1 (FSCM 14345)

QTY	KEY	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	ITEM NO.
20		96906	MS27473T16F35P	CONNECTOR, 55 CONTACTS		1
2		96906	MS27506F16-2	CABLE CLAMP		2
2		96906	MS27473T16F6P	CONNECTOR, 6 CONTACTS, PLUG		3
8		77820	21-33122-546	COAXIAL CONTACT, SIZE 12, PLUG	A B D E	4
1		16345	100068-01	EXTENDER CARD PRINTED WIRING ASSY		5
1		16345	102085-01	70 PIN EXTENDER CARD PRINTED WIRING ASSY		6
1		16345	106658-01	CARD EXTRACTOR		7
6		96906	MS27693-12	CONNECTOR, NO.12, PLUG	C F	8
6		77820	10-407479-1F	CRIMP SLEEVE	F	9

		PL 14-110930	A
		CODE IDENT 14345	SHEET 3	REV

SECTION II
INSTALLATION

2.1 INTRODUCTION

There are three basic ways to install the 1602B processor in equipment racks; with Option 31, the processor can be directly installed in ATR racks; with Option 33 (processor with heat exchanger on a Rack Mount), it can be installed directly into a 19 in. RETMA rack; or with Option 32 (Hardmount) it is attached to a tray suitable for deck or bulkhead mounting. There are no basic limitations to special mounting configurations since the processor is insensitive to physical orientation.

The processor system is fully tested prior to shipping. It is packed for shipment with all circuit modules installed in appropriate locations. Unless there is obvious physical damage from shipment, it can be installed and operated without any internal inspection. Physical installation, electrical connections, cooling, and checkout procedures for the basic processor are described in this section. Similar information for optional equipment such as expansion chassis, peripheral devices, etc., is contained in the appropriate sections of Appendices B and C.

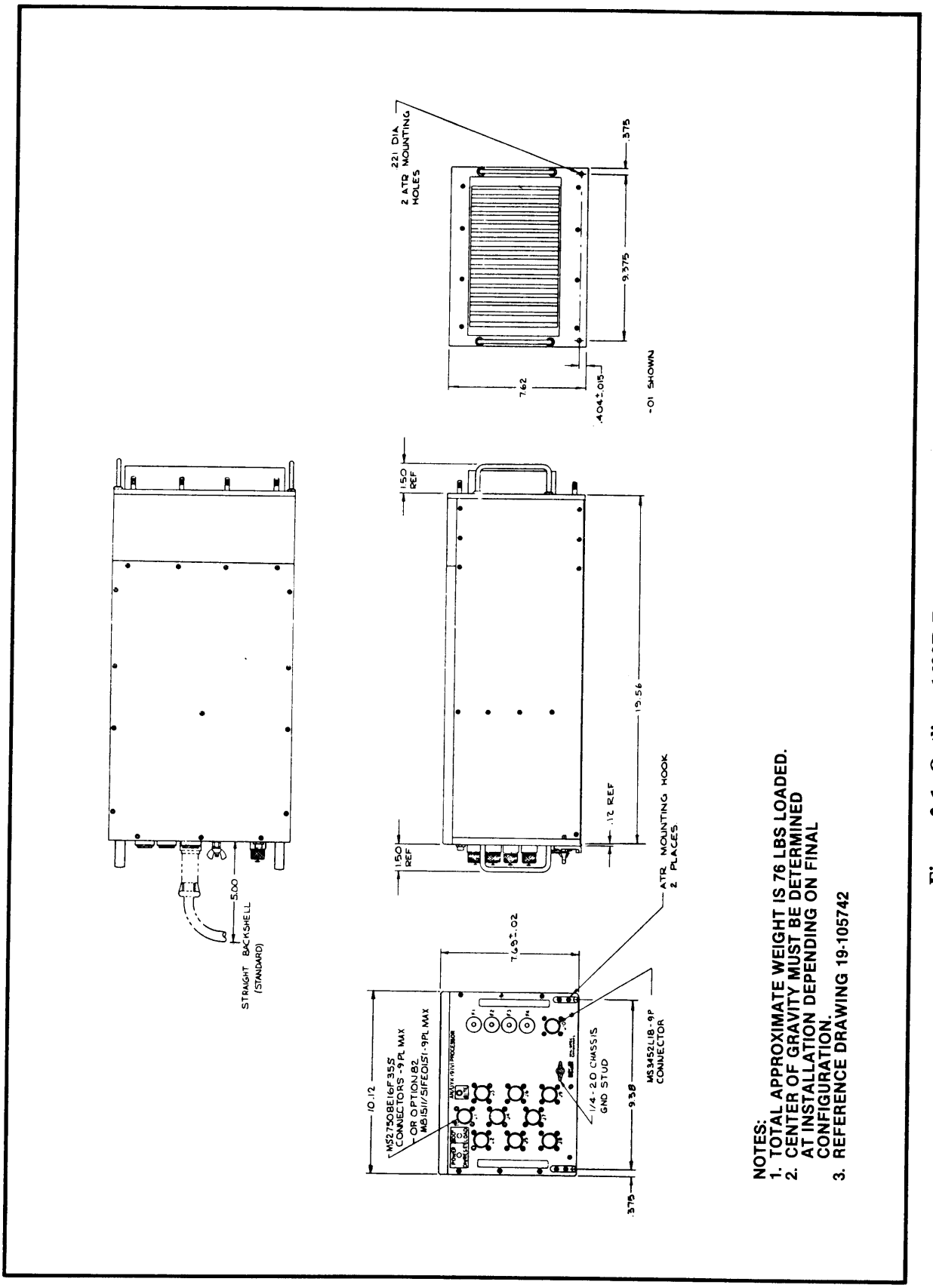
2.2 MECHANICAL INSTALLATION

Figures 2-1 and 2-2 show outline dimensions for the 1602B processor and control panel. Figures 2-3 through 2-5 show installation dimensions for the three basic mounting techniques as described in the following sections. Figure 2-6 shows mounting dimensions for the control panel when it is ordered with a rack mount, Option 30.

2.3 ATR Mounting

The processor mounts directly in a standard size ATR tray. Two holes at the lower rear corners of the chassis pick up the ATR guide pins, and the chassis is secured by two holddown clips at the lower front corners. A ground strap to system chassis or frame ground should be installed to satisfy any system grounding requirements and also to provide for personal safety. The control panel should be installed remotely as called for in the overall system installation plan.

To simplify installation, ROLM offers an ATR mounting tray, 1602B Option 31. When shipped with a system, this tray has guide pins already set for the processor. The tray installs directly to any firm shelf and contains vibration isolators. Figure 2-3 shows outline dimensions of the tray.



NOTES:
1. TOTAL APPROXIMATE WEIGHT IS 76 LBS LOADED.
2. CENTER OF GRAVITY MUST BE DETERMINED AT INSTALLATION DEPENDING ON FINAL CONFIGURATION.
3. REFERENCE DRAWING 19-105742

Figure 2-1. Outline, 1602B Processor Chassis

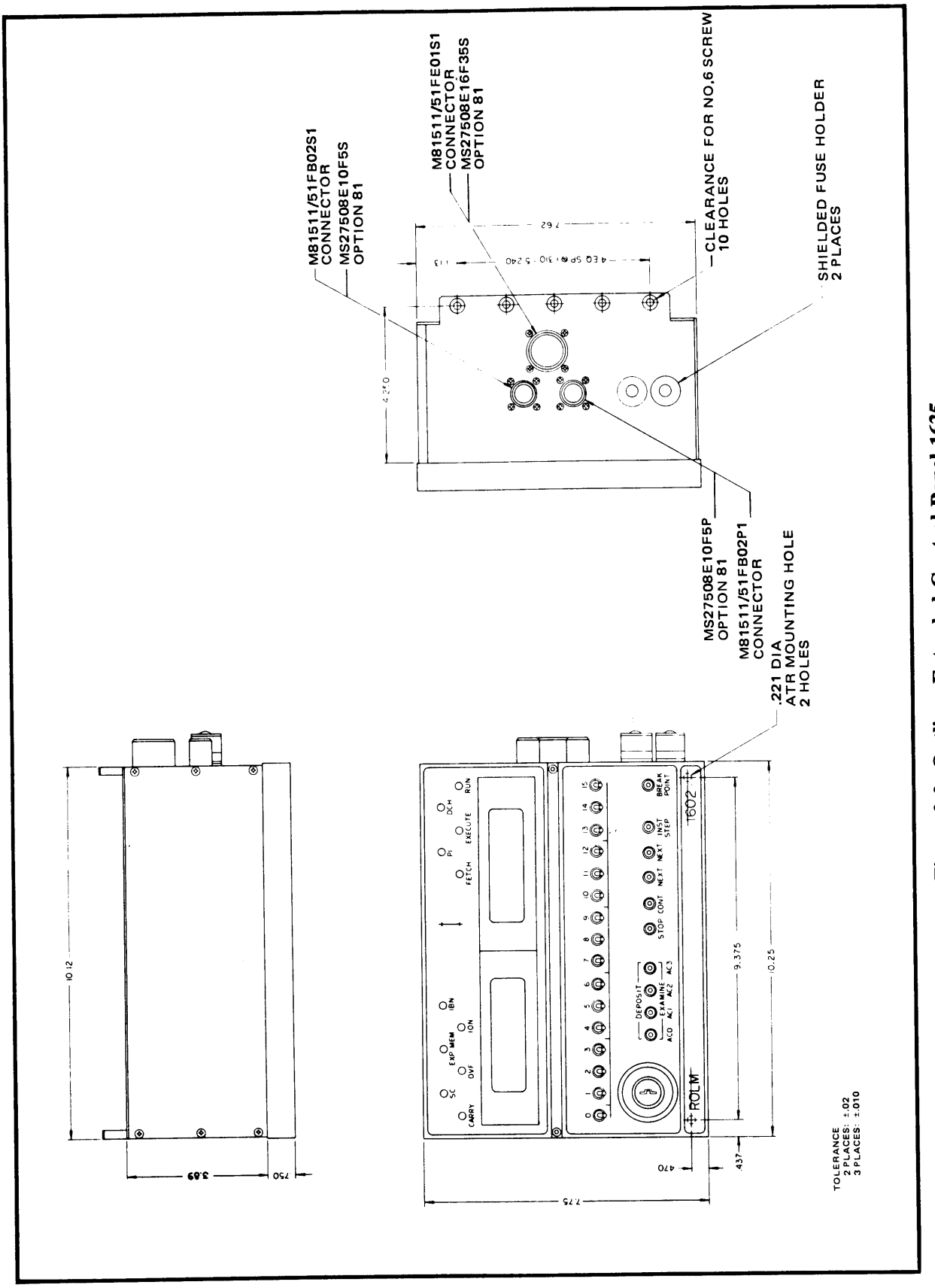


Figure 2-2. Outline, Extended Control Panel 1635

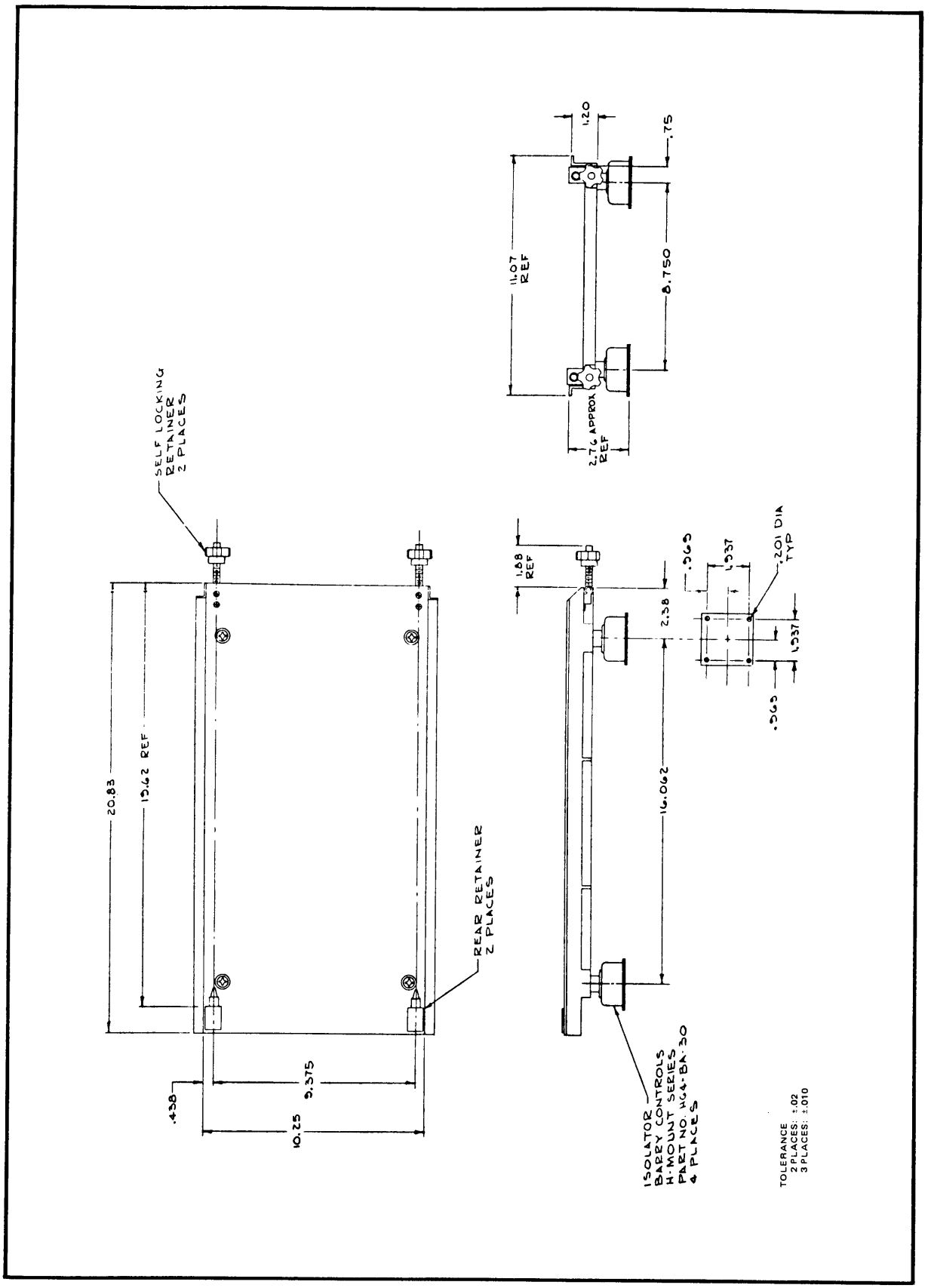
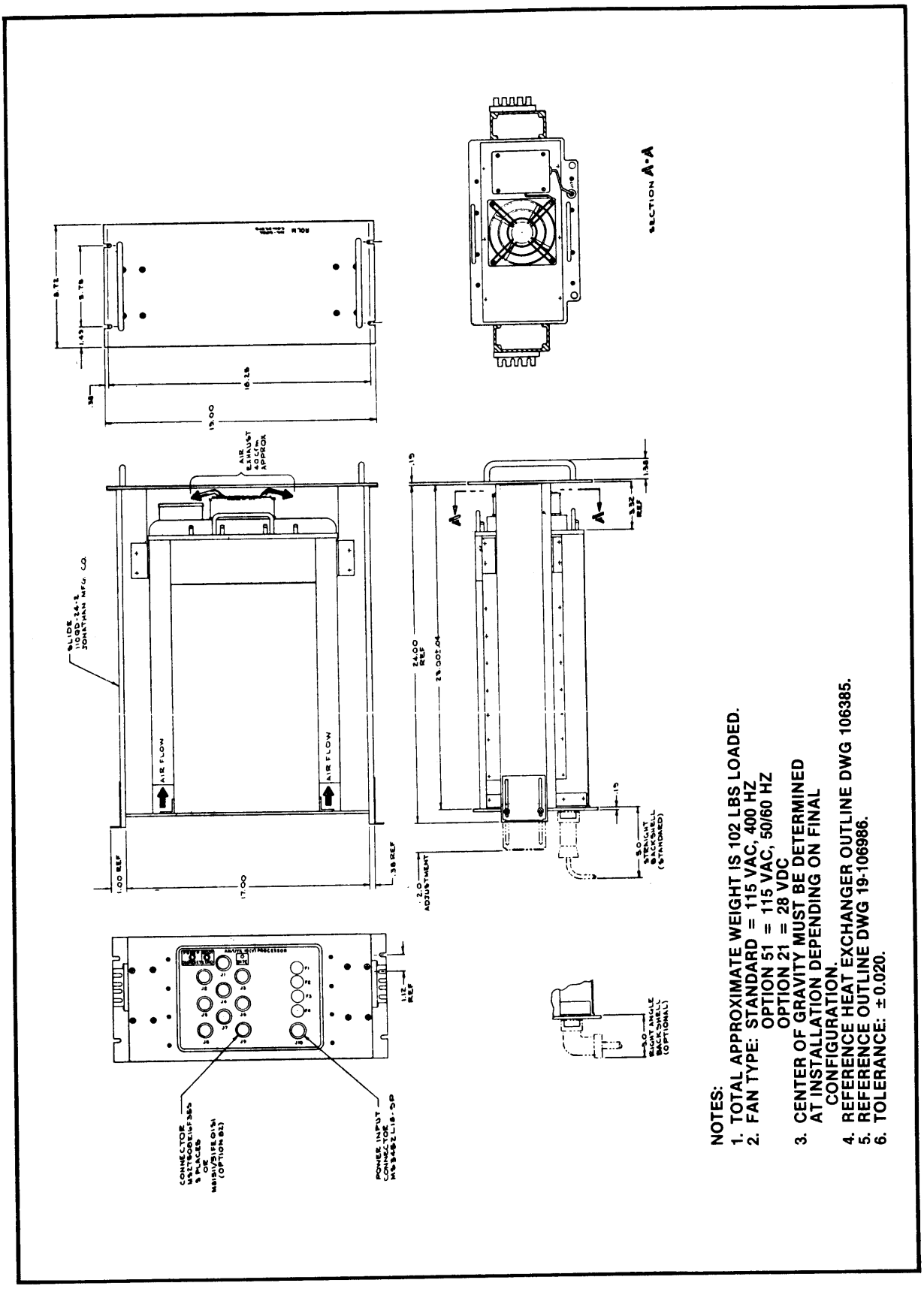


Figure 2-3. ATR Tray



NOTES:
1. TOTAL APPROXIMATE WEIGHT IS 102 LBS LOADED.
2. FAN TYPE: STANDARD = 115 VAC, 400 HZ
   OPTION 51 = 115 VAC, 50/60 HZ
   OPTION 21 = 28 VDC
3. CENTER OF GRAVITY MUST BE DETERMINED AT INSTALLATION DEPENDING ON FINAL CONFIGURATION.
4. REFERENCE HEAT EXCHANGER OUTLINE DWG 106385.
5. REFERENCE OUTLINE DWG 19-106986.
6. TOLERANCE: ±0.020.

Figure 2-4. RETMA Rack Installation

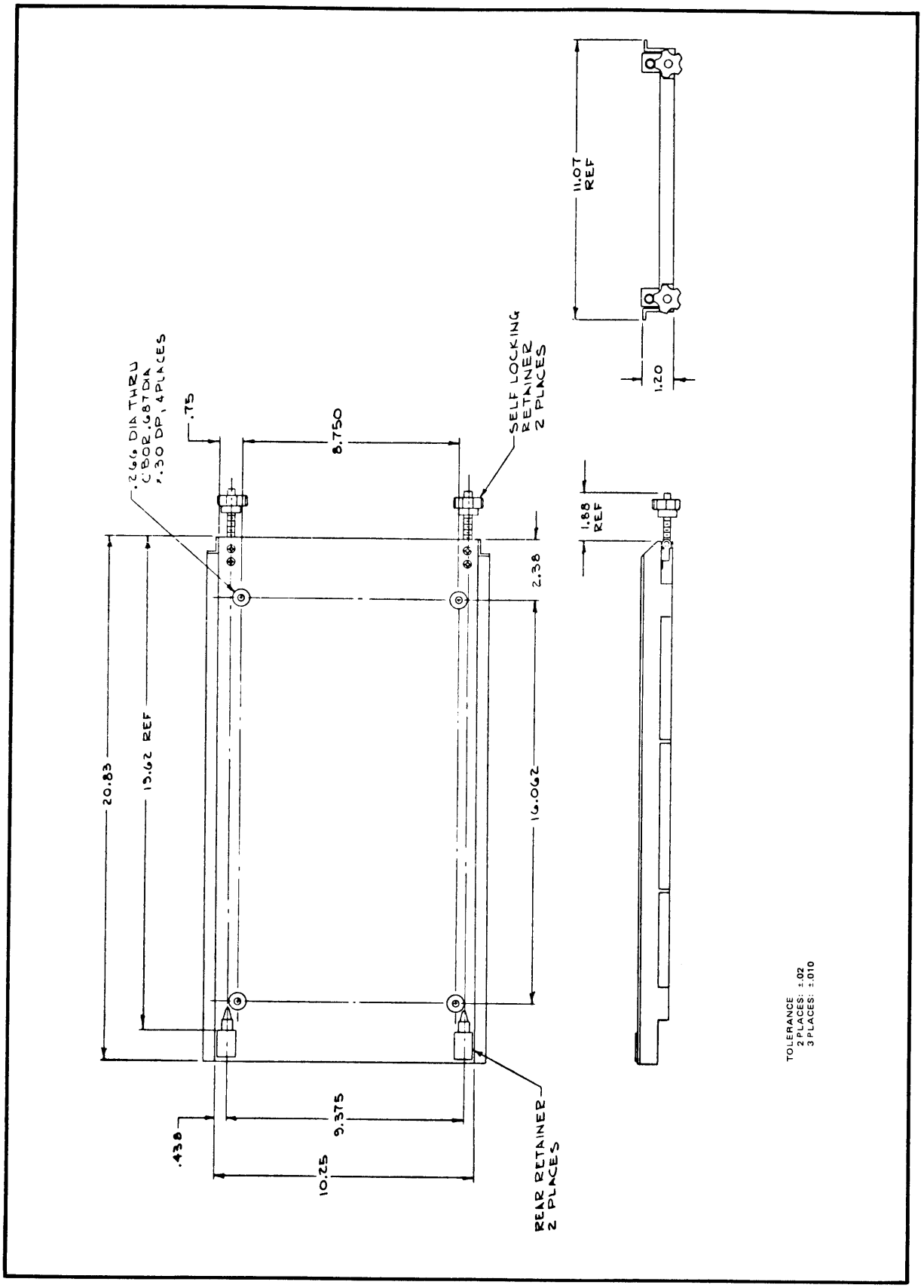
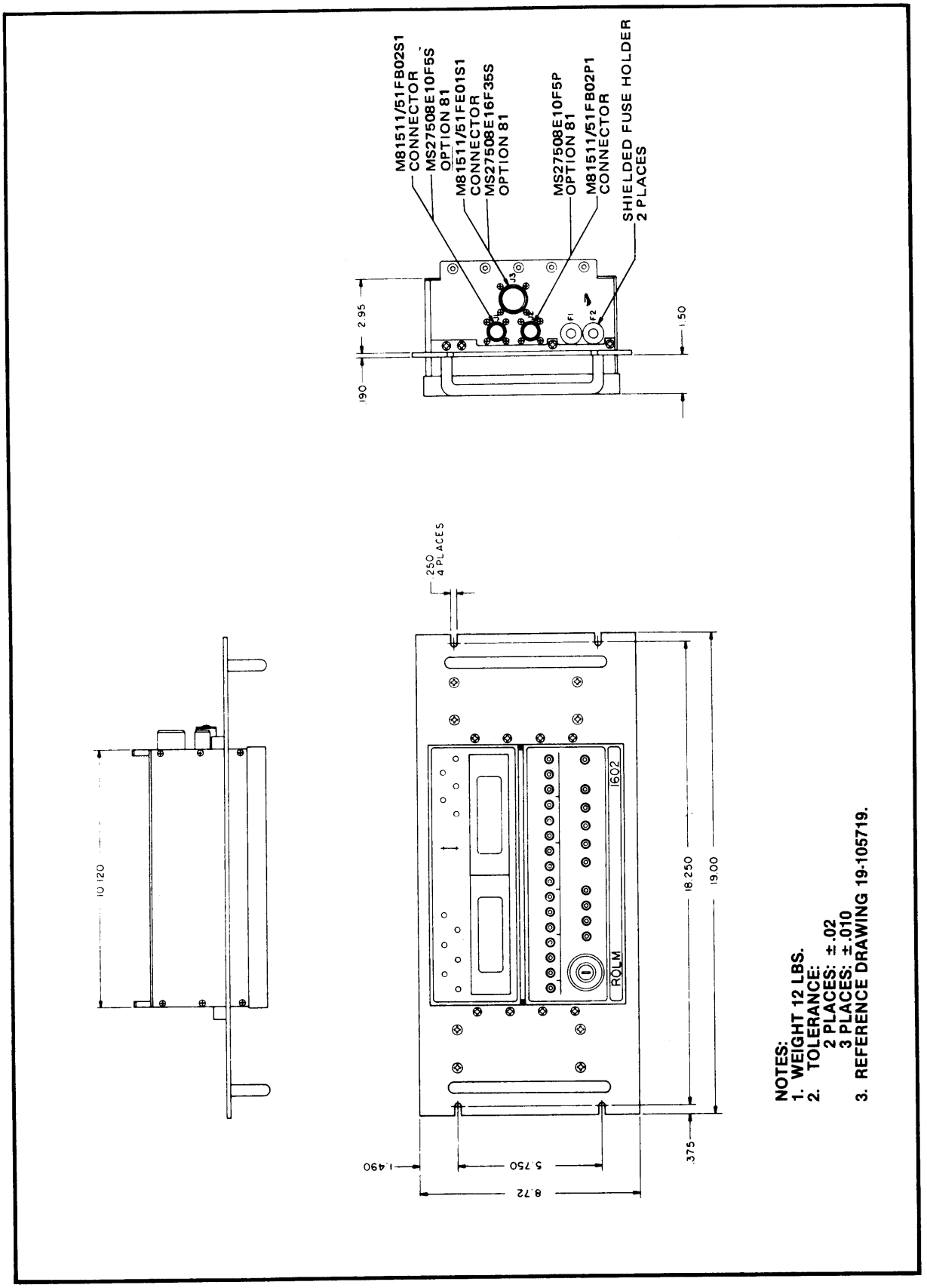


Figure 2-5. Hardmount Installation



NOTES:
1. WEIGHT 12 LBS.
2. TOLERANCE:
   2 PLACES: ±.02
   3 PLACES: ±.010
3. REFERENCE DRAWING 19-105719.

Figure 2-6. Control Panel, RETMA Rack Installation

2.4 RETMA Rack Mounting

When the 1602B processor is ordered with Option 33, appropriate hardware is attached to the chassis to allow direct mounting in a 19 in. standard RETMA rack, requiring 8¾ in. of panel height. Figure 2-4 shows the mounting dimensions. Universal slides allow ready access to the computer from the front of the rack. Installation consists of attaching the slides and front panel to the rack with 10-32 hardware using the standard hole patterns provided.

This rack mount equipment includes a built-in heat exchanger to facilitate heat removal from the power supply and side plates of the processor. The heat exchanger incorporates a low speed, high-reliability fan conforming to MIL-B-23071. Air flow is approximately 40 cfm. The fan operates from the internal power supply.

2.5 Hardmount Tray

When the processor is ordered with Option 32, it is delivered attached to a hardmount tray suitable for easy attachment to floor, deck, or bulkhead. Mounting dimensions are shown in Figure 2-5. Use ¼ in. bolts for attachment.

2.6 COOLING

The Model 1602B is conductively cooled; that is, all internal heat-dissipating elements are cooled by conduction to the chassis; no internal forced air or coolant is required. Processor temperature specifications are considered with respect to the case or chassis temperature. Provision must be made in installation of the computer for removing sufficient heat to keep the chassis within the required temperature range.

2.7 ELECTRICAL CONNECTIONS

All electrical connections to the processor are made at the front panel, including input power, control panel, and I/O connections. Connector locations are shown in Figure 2-7. Figure 2-8 shows control panel connectors.

2.8 Input Power

Power to the processor enters at connector J10, the pin assignments of which are:

Pin No.	Function	Recommended AWG
A	−DC	12
D	+DC	12
G	Chassis Ground	16
E	AC Line	16
B	AC Neutral	16
C	NC	
F	NC	

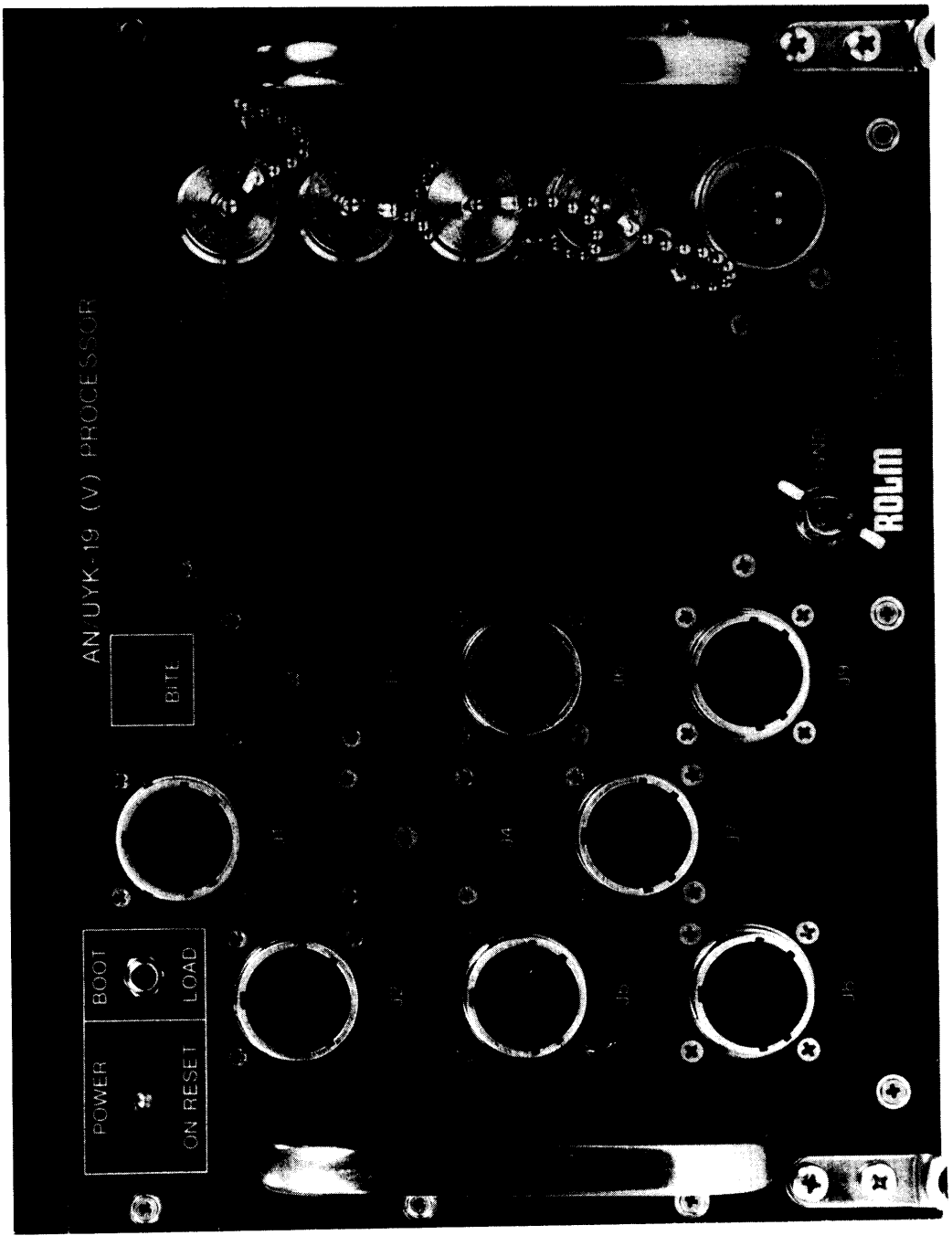


Figure 2-7. Model 1602B Processor, Front View

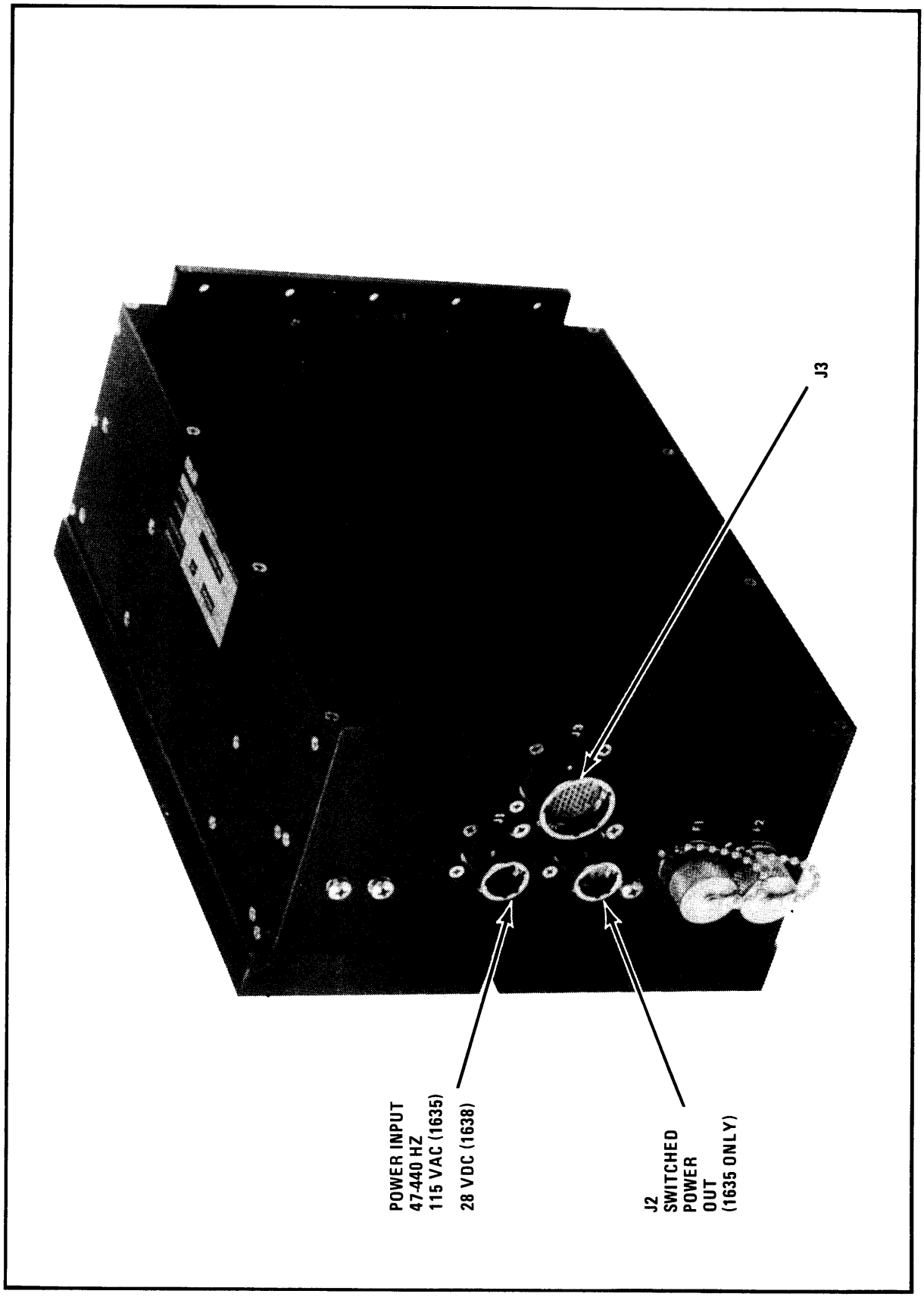


Figure 2-8. Control Panel Connectors

Power to the control panel enters at connection J1. The Model 1638 Control Panel accepts only 28 Vdc (nominal) per MIL-STD-704B. Power connector pin assignments are:

Model 1638, J1

Pin Number		Function
MIL-C-38999	MIL-C-81511	
A	1	+ VDC
B	2	– VDC
C	3	Chassis Gnd
D	4	—
E	5	—

2.9 Grounding

The processor is shipped with signal (digital) ground isolated from the chassis. When a common ground is required, it is recommended that signal ground be connected to earth ground (chassis) at a single point in the system. Preferably, this connection should be made by a jumper wire between J11-1 and J11-2 (see Section V for connector location).

2.10 Connectors

Connector identification is given in Table 2-1. Connector pin assignments are given in Section V.

2.11 SLOT/MOTHERBOARD WIRING

Slots A8–A22 are dedicated as shown in Figure 5-1. Slots A1–A7 are reserved for I/O, and they are wired as shown in the configuration tables referenced in Paragraph 1.3. Any of the seven slots not otherwise filled must contain a Model 3566 Priority/Load Module to provide continuity of the interrupt and data channel priority chains and to present a nominal load to the power supply.

2.12 SPECIAL I/O WIRING

If the processor is wired for Option 60, connector J1 in each I/O slot A3–A7 is grounded at pins 1, 13, 34, and 53. The remaining 50 pins in each of these connectors are wired pin-for-pin to the associated front panel connector (Table 2-1). Pin 55 of each associated front panel connector carries the cable shield to chassis ground. When Option 60 is specified for the processor, Option 60 must also be specified for any I/O modules not otherwise compatible with Option 60 wiring for I/O slots A3–A7.

Table 2-1. Front Panel Connectors, Model 1602B/D Processor

REF Designation	Chassis Slot	Function	Connector Part No.	Mating Connector
J1	A8	CPI[1]	MS27508E16F35S	MS27473E16F35P
J2	A3	I/O	MS27508E16F35S	MS27473E16F35P
J3	A4	I/O	Blank	Not Applicable
J4	A5	I/O	Blank	Not Applicable
J5	A6	I/O	MS27508E16F6S	MS27473T16F6P
J6	A1	I/O	MS27508E16F35S	MS27473E16F35P
J7	A2	I/O	MS27508E16F35S	MS27473E16F35P
J8	A7	I/O	MS27508E16F6S	MS27473T16F6P
J9	—	CP[2]	MS27508E16F35S	MS27473E16F35P
J10	—	PWR[3]	MS3452L18-9P	MS3456L18-9S

[1]Control Panel Interface [2]Control Panel [3]Power Input

Option 60 wiring also defines the types of modules that may be used for specified I/O slots. Type 2 wiring, used in slots A1 and A2, is designed for the Model 3561 or 3561A Expander or a customer-designed module with expander-type pinouts. Type 1 wiring, used in slots A3-A7, is designed for any option 60 I/O module.

Slots A8–A22 which are not affected by Option 60, are dedicated as shown in Figure 5-1.

Option 60 does not affect motherboard wiring for connector J2 in each I/O slot, the wiring of which remains as listed in Table 5-1.

2.13 CHECKOUT

A typical installation with remote panel might appear as depicted in Figure 2-9, where the processor operates with a terminal, paper tape reader, and other external devices. When the devices are ordered through ROLM Corporation, interconnecting cables are provided. The following steps are involved in connecting the system for operation:

1. Connect *power* cables to all units in the system, ensuring male-female relationships on connectors. Each processor, expansion chassis, and peripheral should be connected to its required power source. *DO NOT* connect signal cables between chassis at this time.

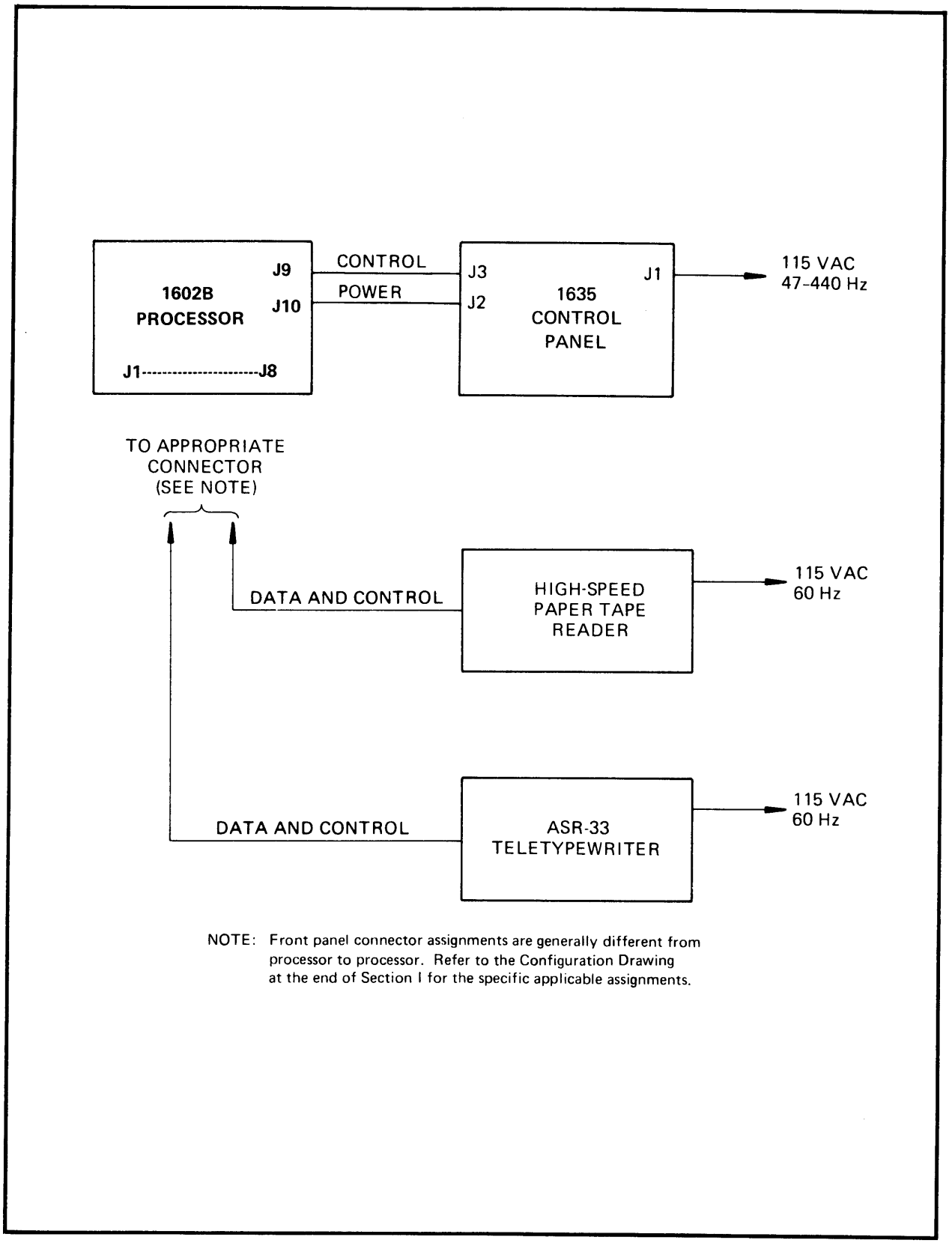
2. Verify that no potential difference will exist between chassis when power is applied by checking that each chassis measures zero ohms to earth ground.

3. Turn on all power sources. With a voltmeter measure potential differences between all chassis in the system. Use a low voltage scale (e.g., 2.5 volts) and measure ac and dc.

4. Correct any voltage differences. There should be zero volts between all chassis.

5. On each chassis, verify that signal ground is shorted or isolated from the chassis as required by the overall system grounding plan. Correct any discrepancies.

6. Connect all system signal cables. Refer to the configuration information in Section I for appropriate connections.



NOTE: Front panel connector assignments are generally different from processor to processor. Refer to the Configuration Drawing at the end of Section I for the specific applicable assignments.

Figure 2-9. Typical System Connection

7. Refer to device operating manuals for instructions in their operation.

To check the basic operation of the processor, a number of manual checks (using the control panel) can be made. Also, the Instruction Test diagnostic program can be loaded and executed to provide a thorough test of CPU operation. The processor, control panel, and a peripheral device for loading paper tape are connected as described above. Either a terminal paper tape reader or a high-speed reader can be used for loading programs, and it is assumed that one is available with a compatible interface module in the processor.

If the user is unfamiliar with 1602B processor operation, it is suggested that Section III (Operation) be read thoroughly before proceeding further. The following checks will verify basic operation prior to loading the Instruction Test Program:

1. Turn power on.
2. Enter all 0's in DATA switches; deposit and examine 0's in memory location 0.
3. Deposit and examine all 1's in memory location 0.
4. Deposit and examine all 0's in AC (accumulators) 0–3.
5. Deposit and examine all 1's in AC (accumulators) 0–3.
6. Deposit 000017 in AC0.
7. Deposit 000360 in AC1.
8. Deposit 007400 in AC2.
9. Deposit 170000 in AC3.
10. Examine all accumulators and verify that the data has not been changed.
11. Deposit all 0's in memory location 0. Keep all 0's in DATA switches.
12. Raise START switch. Verify that the RUN indicator is ON.
13. Press STOP switch to halt the computer. Verify that the RUN indicator is OFF.
14. If the diagnostics were supplied on paper tape, manually load and run the Memory Address Test. See Section III for listing.
15. If the diagnostics were supplied on an Integrated Diagnostic Management System (IDMS) media, boot the media. IDMS will perform a memory address check and output an error message if faulty memory is detected.

Once the manual tests have been performed, a more thorough check should be made with the 1602/1650 Instruction Test program. With the 1602/1650 Instruction Test program (Binary Tape No. 495-150362) loaded into core memory, refer to the corresponding listing (Document No. 497-150362) for a detailed description of the test. Follow the steps listed below to execute the program:

1. Set the control panel data switches to 000060. Press RESET and then START. The program should execute a HALT instruction and stop running.

2. Examine the contents of Accumulator 3. It should ocntain the octal number 60.

3. Press the CONTINUE switch. The program should run continuously without halting.

The proper running of the Instruction Test program is a good indication that the basic processor is operating satisfactorily. For a more complete checkout, run the various diagnostic programs as described in Section V and perform the checkout procedures given in Appendices B and C for the various I/O and other options installed in the system.

SECTION III
OPERATION

3.1 INTRODUCTION

There are two basic modes in which the 1602B processor is generally operated. These might be called the operator-oriented mode and the system mode. The operator-oriented mode includes such activities as program editing and assembly, diagnostic testing, paper tape preparation and duplication, program debugging, system debugging, and preparation for systems operation. In this mode the control panel is connected to the processor, and generally a program input/output device, such as a teletypewriter, is also attached. When in the system mode, the processor is simply executing a systems program, usually without an operator required. In this mode the control panel and the program loading devices need not be attached.

This section of the manual describes in detail the operator-oriented operation of the processor. In addition it contains a description of the instruction set and coding formats.

3.2 CONTROL PANEL OPERATION

The control panel provides a means for manually entering data, examining contents of memory or CPU registers, and controlling the operation of the processor. The control panel uses light-emitting diodes for display purposes, and the address and data are displayed in octal form. A photograph of the control panel is shown in Figure 3-1.

The control panel contains four basic groups of displays. At the upper right are five lights that indicate what is occurring with the processor. The six lights at the upper left display the contents of certain processor status flags. Below these are a pair of six-digit octal displays, one for address information, and one for data.

Below the octal displays is a register of toggle switches through which the operator can supply address and data to the processor (the up position of a switch represents a binary 1). This switch register can be used in conjunction with some of the operating switches, and its contents can be transferred under program control to an accumulator.

In the bottom row of the panel are the operating switches. Each switch lever is actually two momentary-contact logical switches with a common off position in the center. Lifting the lever up turns on the switch whose name is printed above it; pressing down on it turns on the switch whose name is written below.

At the lower left is a three-position key-operated rotary switch that controls power and locks the console. Turning it to ON simply turns on power. Turning it to LOCK keeps power on and disables the operating switches so that no one can interfere with the operation of the processor (the operator can still use the data switches to supply information to the program). Turning the power switch to LOCK also enables the Autorestart feature in the event primary power is interrupted and restored.

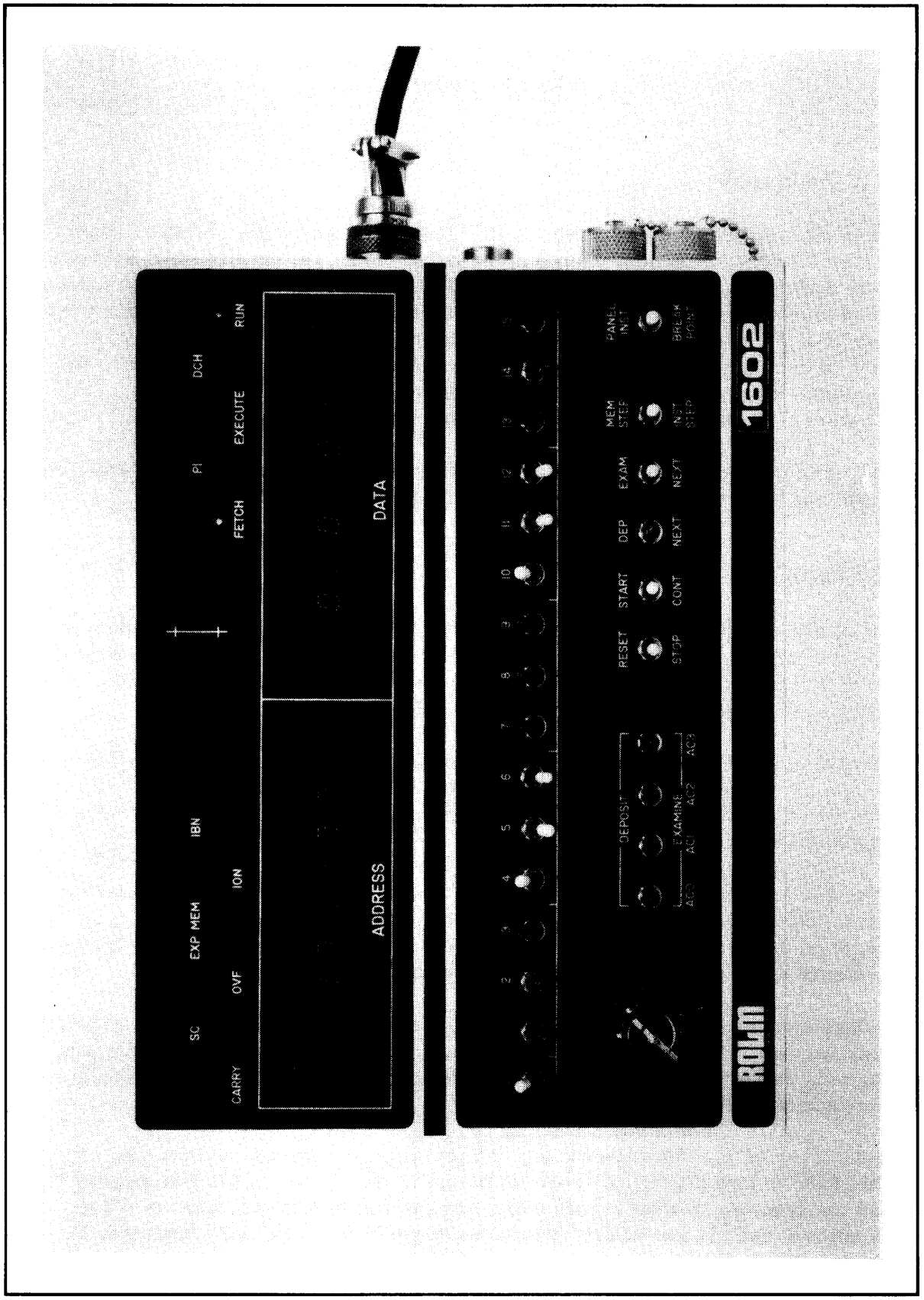


Figure 3-1. Control Panel, Front View

3.3 Indicators

When any control panel indicator is lit, the associated flip-flop is in the one state or the associated function is true. A few indicators display useful information while the processor is running, but most change too frequently and are therefore discussed in terms of the information they display when the processor has stopped.

The ADDRESS lights display the next memory address that will be accessed. The DATA lights display the last word transferred to or from memory. The various control or status light functions are described below for the case where the light is on.

RUN	The processor is in normal operation with one instruction following another. When the light goes off, the computer has stopped.
FETCH	The next memory operation will be to fetch an instruction. FETCH normally indicates that the quantity displayed in the ADDRESS lights is PC, although this may not be true immediately after a RESET operation.
EXECUTE	Normally will not be lit when the CPU is halted. When the CPU is running, it indicates nonfetch memory cycles are occurring.
DCH	Some in-out device is requesting a direct memory access cycle. This light is equivalent to the DCHR line in the I/O bus.
PI	Some in-out device is requesting a program interrupt. This light is equivalent to the INTR line in the I/O bus.
ION	The program interrupt is enabled (this is the Interrupt On flag).
CARRY	This light displays the state of the CARRY flag.
OVF	This light displays the state of the signed-overflow flag, OVF.
IBN	This light is on when the computer is in the interrupt branch-and-nest mode.
EXP MEM	This light is on when the computer is in the expanded-memory mode (i.e., can address 65K of memory).
SC	This light is on when the last memory location accessed was in semiconductor memory.

3.4 Operating Switches

All of the switches in the bottom row except STOP and RESET are interlocked so that they have no effect if RUN is lit. The four pairs of switches at the left are for depositing data in the accumulators and examining their contents. Lifting a switch lever up loads the contents of the DATA switches into the specified accumulator; pressing it down displays the contents of the accumulator in the DATA lights.

The 12 switches at the right perform the following functions when turned on:

EXAMINE	Load the address contained in the DATA switches into PC (which is displayed in the ADDRESS lights) and display the contents of the address location in the DATA lights.
DEPOSIT	Deposit the contents of the DATA switches in the memory location specified by the ADDRESS lights. At completion the DATA lights display the word deposited.
EXAMINE NEXT	Add 1 to the PC address displayed in the ADDRESS lights and display the contents of the location specified by the incremented address in the DATA lights.
DEPOSIT NEXT	Add 1 to the PC address displayed in the ADDRESS lights and deposit the contents of the DATA switches in the memory location specified by the incremented address. At completion the DATA lights display the word deposited.
START	Load the address contained in the DATA switches into PC, light RUN, and begin normal operation by executing the instruction at the location specified by PC.
STOP	Stop with FETCH on before beginning the next instruction. Thus the processor finishes the current instruction and then stops unless a device is waiting for data channel access or a program interrupt, in which case it performs all such operations before stopping. The ADDRESS lights point to the next instruction.

CAUTION

If the current instruction contains an infinitely long indirect addressing chain or there are continuous data channel requests, pressing STOP will stop the processor (see RESET, below).

CONTINUE	Turn on RUN and begin normal operation in the state indicated by the lights.
INST STEP	Begin operation in the state indicated by the lights but then stop as though STOP had been pressed at the same time. If the stop occurs at the end of an instruction, the data displayed by the DATA lights is the next instruction.
MEMORY STEP	Same as for INST STEP.

PANEL INST — Execute the instruction contained in the data switches and then stop. This instruction will normally be a single-word, nonmemory-reference instruction. Pressing PANEL INST causes PC to be decremented by 1, the contents of the DATA switches to be supplied as the (first word of the) instruction, and the STOP signal to be simulated. Thus an instruction that would skip will cause PC to be incremented by 1.

BREAKPOINT — Begin operation of the processor as with CONTINUE, but enable breakpoint sensing. When breakpoint sensing is enabled, the instruction addresses are continually compared with the DATA switches. If the instruction address ever matches the DATA switches, the processor will halt at the end of the matching instruction. The instruction at the breakpoint location will be completed; if the instruction is a jump-type instruction, the value of PC displayed in the ADDRESS lights when the processor halts may bear no obvious relationship to the breakpoint address. Holding the MEMORY STEP switch up while breakpoint sensing is enabled will cause all memory addresses to be monitored, i.e., addresses of data as well as instructions.

RESET — Stop at the end of the current memory cycle. An I/O Reset Pulse (IORST) is sent out to clear the flags in all I/O devices. The ION, IBN, and EXP MEM flags are cleared. Light the FETCH light.

EXAMINE can be used to load PC for beginning any single-step procedure. To use the various EXAMINE and DEPOSIT switches between instruction steps, simply remember what PC is and restore it before continuing.

3.5 Functional Summary

The following list briefly indicates which switches are used to perform certain basic functions at the control panel.

To stop an executing program:	Press STOP. If this fails, press RESET.
To clear the input/output devices and reset the CPU to a standard state:	Press RESET.
To start the CPU executing a stored program:	Put the starting address of the program in the DATA switches, and press START.
To continue the execution of a program from a stopping point:	Press CONTINUE.
To run a program until a specific instruction is reached:	If necessary use EXAMINE to get the program starting address into the ADDRESS lights. Put the breakpoint address into the DATA switches, and press BREAKPOINT.

To examine the contents of an accumulator:	Press the appropriate EXAMINE-AC switch. The contents will be displayed in the DATA lights.
To deposit data into an accumulator:	Place the data in the DATA switches. Press the appropriate DEPOSIT-AC switch.
To examine the contents of a memory location:	Press the memory address in the DATA switches. Press EXAMINE. The address will be displayed in the ADDRESS lights and the contents of the memory location will be displayed in the DATA lights.
To deposit data in an alterable memory location:	Place the memory address in the DATA switches, and press EXAMINE. (If the appropriate address already appears in the ADDRESS lights, the above steps may be omitted.) Place the information to be deposited in the DATA switches and press DEPOSIT.
To examine a block of memory:	Place the starting address of the block in the DATA switches and press EXAMINE. The address of the first word of the block will appear in the ADDRESS lights and its contents in the DATA lights. Then repeatedly press EXAMINE-NEXT to increment the address. At all times the contents of the word addressed by the address by the ADDRESS lights will be displayed in the DATA lights.
To deposit data into a block of memory:	Place the starting address of the block in the DATA switches and press EXAMINE. Place the first data word in the DATA switches and press DEPOSIT. For subsequent data words, place them in the DATA switches and press DEPOSIT-NEXT.
To cause the CPU to execute on program instruction from memory:	If necessary, use EXAMINE to get the address of the instruction into the ADDRESS lights. Then press INST-STEP.
To cause the CPU to execute an instruction from the DATA switches:	Place the (single-word) instruction in the DATA switches. Press PANEL INST.
To supply power to the computer:	Turn the power switch to ON.

To cut off power to the computer:	Turn the power switch to OFF.
To disable the STOP and RESET switches:	Turn the power switch to LOCK.

3.6 LOADING PROGRAMS

Before the 1602B can execute a program, the instructions comprising the program must be loaded into the 1602B memory from an external source. The procedure for loading a program depends upon the exact system configuration or, in particular, upon the I/O devices available. The BOOT LOAD switch on the front panel of the processor can simplify this procedure, as described in the following section.

3.7 Using the BOOT LOAD Switch

When the BOOT LOAD switch on the front panel of the processor is depressed, the program listed in Table 3-1 is loaded from a ROM (Read-Only Memory) into the top 127 locations in read/write memory and then executed. The program reads control panel DATA switches 10 through 15 and proceeds according to the following.

Data Switches 10–15	Operation
10_8	Load a program from paper tape by means of a Teletype® reader.
20_8	Do a bootstrap load of a program from fixed-head disk.
22_8	Do a bootstrap load of a program from magnetic tape.
33_8	Do a bootstrap load of a program from moving-head disk (DP0 only).
77_8	Execute a simple memory address test which writes the address of each available memory location into itself and then checks each location. Display the pass count in the DATA display. If an error is detected, the program halts with the error address in Accumulator 2 and the error word read from that address in Accumulator 3.
Any other setting	Load a program from paper tape by means of a high-speed reader.

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If the selected device does not exist in the system, the program remains in a wait loop until it is stopped by the STOP or RESET switch on the control panel.

Table 3-1. Boot Load Program

```
07601   004401          JSR .+1
07602   076601          SBFNW 3
07603   000002          2
07604   054573          STA 3, TOP          ;TOP OF MEMORY
07605   060477          READS 0
07606   024541          LDA 1, C77
07607   123400          AND 1,0
07610   106415          SUB# 0,1,SNR        ;MEM TEST?
07611   000551          JMP MTST            ;YES
07612   024544          LDA 1,STDEV
07613   107000          ADD 0,1
07614   044542          STA 1,STDEV
07615   030531          LDA 2, C20          ;DEV 20
07616   112415          SUB# 0,2,SNR
07617   000536          JMP BOOT            ;FH DISK
07620   064002          ADPI 2              ;DEV 22
07621   112415          SUB# 0,2,SNR
07622   000533          JMP BOOT            ;MAG TAPE
07623   064011          ADPI 11             ;DEV 33
07624   112415          SUB# 0,2,SNR
07625   000524          JMP MHDBT           ;MH DISK
07626   064355          ADNI 55             ;DEV 10
07627   112414          SUB# 0,2,SZR        ;TTY?
07630   102620          SUBZR 0,0           ;NO, ASSUME PTR

07631   040514  PTRTY:  STA 0,SAVE          ;STANDARD BLOCK LOADER
07632   060110          NIOS TTI
07633   060112          NIOS PTR
07634   004471  BLOCK:  JSR GTCHR
07635   171305          MOVS 3,2,SNR
07636   000776          JMP BLOCK
07637   004466          JSR GTCHR
07640   173300          ADDS 3,2
07641   141000          MOV 2,0
07642   145000          MOV 2,1
07643   004453          JSR BUILD
07644   050500          STA 2,ADDRS
07645   004451          JSR BUILD
07646   125113          MOVL# 1,1,SNC
07647   000430          JMP TEST
07650   044473          STA 1,COUNT
07651   024473          LDA 1,ADDRS
07652   062301          DSPD
07653   024470          LDA 1,COUNT

07654   030466          LDA 2,TEMP2
07655   064312          ADNI 12
07656   034466          LDA 3,ADDRS
```

Table 3-1. Boot Load Program (Continued)

```
07657   136400          SUB 1,3
07660   172023          ADCZ 3,2,SNC
07661   000414          JMP CHKER
07662   030464          LDA 2,C20
07663   147033          ADDZ# 2,1,SNC
07664   010457          ISZ COUNT
07665   147022          ADDZ 2,1,SZC

07666   125113  STORE:  MOVL# 1,1,SNC
07667   004427          JSR BUILD
07670   052454          STA 2,@ADDRS
07671   010453          ISZ ADDRS
07672   014051          ISZ COUNT
07673   000773          JMP STORE
07674   101004          MOVE 0,0,SZR
07675   063077  CHKER:  HALT
07676   000736          JMP BLOCK

07677   125224  TEST:   MOVZR 1,1,SZR
07700   000411          JMP IGNOR
07701   101004          MOV 0,0,SZR
07702   000773          JMP CHKER
07703   030441          LDA 2,ADDRS
07704   062677          IORST
07705   151113          MOVL# 2,2,SNC
07706   001000          JMP 0,2
07707   063077          HALT
07710   000777          JMP .-1

07711   004414  IGNOR:  JSR GTCHR
07712   020447          LDA 0,C377
07713   116404          SUB 0,3,SZR
07714   000775          JMP IGNOR
07715   000717          JMP BLOCK

07716   054423  BUILD:  STA 3,TEMO1
07717   004406          JSR GTCHR
07720   171300          MOVS 3,2
07721   004404          JSR GTCHR
07722   173300          ADDS 3,2
07723   143000          ADD 2,0
07724   002415          JMP @TEMP1

07725   054415  GTCHR:  STA 3,TEMP2
07726   034417          LDA 3,SAVE
07727   175103          MOVL 3,3,SNC
07730   000405          JMP .+5
07731   063612          SKPDN PTR
07732   000777          JMP .-1
07733   074512          DIAS 3,PTR
07734   002406          JMP @TEMP2
```

Table 3-1. Boot Load Program (Continued)

```
07735   063610          SKPDN TTI
07736   000777          JMP .-1
07737   074510          DIAS 3,TTI
07740   002402          JMP @TEMP2


07741   TEMP1:  0
07742   000000  TEMP2:  0
07743   000000  COUNT:  0
07744   000000  ADDRS:  0
07745   000000  SAVE:   0
07746   000020  C20:    20
07747   000077  C77:    77


07750   175400  RECAL:  175400
07751   020777  MHDBT:  LDA 0,RECAL
07752   061333          DOAP 0,33
07753   063633          SKPDN 33
07754   000777          JMP .-1
07755   062677  BOOT:   IORST
07756   060100  STDEV:  NIOS 0          ;MODIFY WITH PROPER DEV CODE
07757   020402          LDA 0,C377
07760   040377          STA 0,377
07761   000377  C377:   JMP 377


07762   020415  MTST:   LDA 0,TOP       ;MEMORY ADDRESS TEST
07763   126440          SUBO 1,1        ;CLEAR AC1 AND CARRY
07764   152000  A:      ADC 2,2         ;COMPL CARRY ON INC 2,2
07765   151402  B:      INC 2,2,SZC     ;CARRY =1 FILL/CHK
07766   051000          STA 2,0,2       ;CARRY =0 CHK ONLY
07767   035000          LDA 3,0,2
07770   156414          SUB# 2,3,SZR
07771   063077          HALT            ;AC2=ERROR ADDRESS

07772   112414          SUB# 0,2,SZR    ;END OF PASS?
07773   000772          JMP B           ;NO
07774   125400          INC 1,1         ;BUMP PASS COUNTER
07775   062301          DSPD            ;DISPLAY IT
07776   000766          JMP A           ;LOOP
07777   000000  TOP:    0

                        .END
```

NOTE 1: Octal numbering is normally used to represent the address (location) and data content. For those unfamiliar with this notation, refer to Paragraph 3.29.

NOTE 2: Address character X=3 for a 16K-word memory, X=7 for 32K-word memory, etc.

Selection of device code 77_8 does not activate a program load device, but, rather, it initiates a memory addressing test program. The proper execution of this very basic program indicates that all memory locations from 0 up to X7600 are correctly addressable. (X = 3 for 16K of memory, X = 7 for 32K, etc.) Thus, a quick check of memory availability is provided (accumulator 0 holds the address of the top of memory when this test is run.).

It should be noted that although the top 127 locations in memory are used by the BOOT LOADER during program load, these locations may be used subsequently by a user program, perhaps as a temporary data area. However, as soon as the BOOT LOAD switch is depressed again, these locations will be overwritten.

3.8 Loading Programs from Paper Tape

This section gives an example of a typical usage of the BOOT LOAD switch. The following procedure describes use of an ASR-33 Teletype for the loading into memory of a program stored on paper tape.

Turn the LINE-OFF-LOCAL switch on the Teletype to LINE. Position the three-position reader switch on the Teletype to FREE. Mount the program tape in the Teletype reader with blank leader under the read head of the Teletype. Press RESET on the control panel. Set the Teletype reader switch to START. Set 000010 into the data switches. Press the BOOT LOAD switch on the front panel.

The tape should now be read into memory. As each block is read, the program will display the first address of the block in the DATA lights. At the end of the tape, the loader program will either halt with 710 (octal) displayed in bits 7–15 of the ADDRESS lights, or it will transfer control to the newly loaded program (depending upon the final block on the tape).

If there is an error in attempting to load the paper tape, any of several things may happen. For example:

1. The Teletype may not advance the tape at all. Check that:
   a. The Teletype is connected to a power source and to the computer.
   b. The Teletype is in the LINE mode.
   c. The tape is correctly mounted in the reader so that the leader will be read first and so that the tape will not jam.
   d. The Teletype reader switch is set to START at the appropriate time.
2. The loader may read through the blank trailer and off the end of the tape. In this case press RESET on the control panel and attempt another load.

3. The loader may halt at the end of a block with 676 (octal) displayed in bits 7–15 of the ADDRESS lights. In this event, the tape can either be repositioned at the start or can be backed up one block. Then press BOOT LOAD again with 000010 still in the DATA switches.

3.9 INSTRUCTION SUMMARY

The 1602B instructions and their encodings are summarized in Figures 3-2 and 3-3. They are grouped into two major classes, which are referred to as Type I and Type II. The Type I instructions are compatible with the same instructions on all other models in ROLM's family of military computers, as well as on Data General computers. The Type II instructions are common to the 1602, 1650, and 1664 computers.

The action of individual instructions is described in the following sections. At the left edge of the instructions shown in Figure 3-2, the various instruction execution times (in microseconds) are given. In some cases, the execution time may vary; if so, the execution time given is for the most basic version of the instruction. In some instructions where the execution time is particularly dependent upon data or arguments, no execution time is supplied. Execution times are for core memory.

In all of the following descriptions, ACD is used to symbolize the accumulator specified in bits 3–4 on the instruction.

3.10 Type I Memory Reference Addressing

Bits 5–15 have the same format in every memory reference instruction whether the effective address is used for storage or retrieval of an operand, or to alter program flow. Bit 5 is the indirect bit (I), bits 6 and 7 are the index bits (X), and bits 8–15 are the displacement (D).

The 15-bit effective address E of the instruction depends on the values of I, X, and D. If X is 00, it addresses one of the first 256 memory addresses in the octal range 00000–00377. This group of locations is referred to as page zero.

If X is nonzero, D is a displacement that is used to produce a memory address by adding it to the contents of the register specified by X. The displacement is a signed binary integer in two's-complement notation. Bit 8 is the sign (0 positive, 1 negative), and the integer is in the octal range -200 to $+177$ (decimal -128 to $+127$). If X is 01, the instruction addresses a location relative to its own position; i.e., D is added to the address in PC (which is the address of the instruction being executed). This is referred to as relative addressing. If X is 10 or 11, respectively, it selects AC2 or AC3 as a base register to which D is added. The rightmost 15 bits of the sum yield E, the effective address.

If I is 0, addressing is direct, and the address already determined from X and D is the effective address used in the execution of the instruction. Thus a memory reference instruction can directly address up to 1024 locations: 256 in page zero; and three sets of 256 in the octal range 200

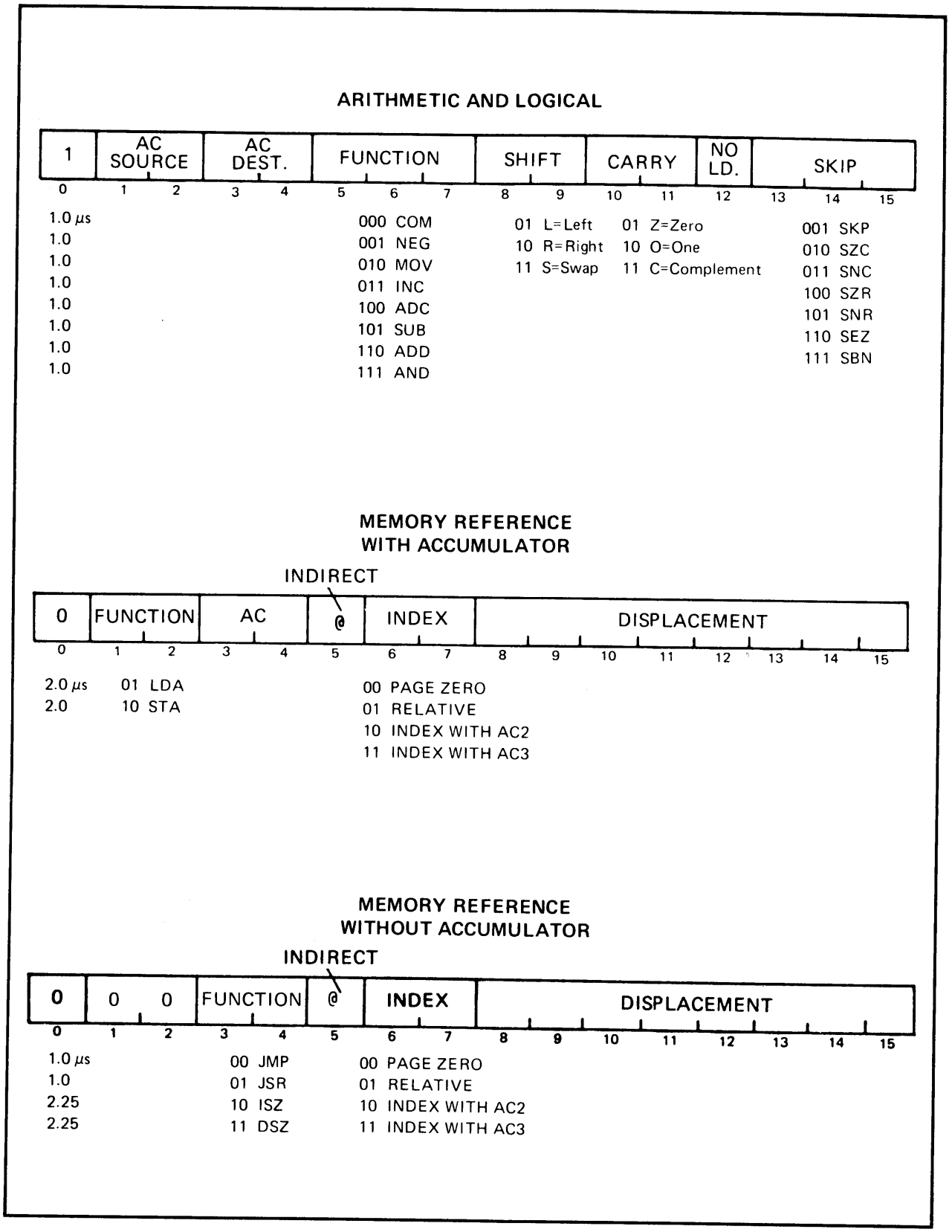
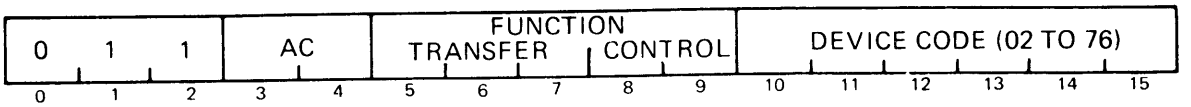


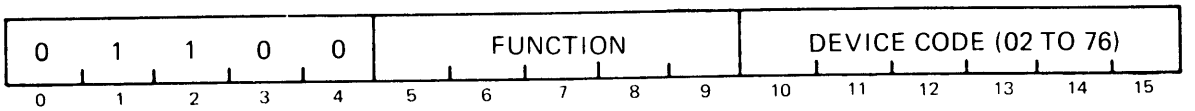
Figure 3-2. Instructions, Type I (1 of 2)

INPUT/OUTPUT WITH ACCUMULATOR



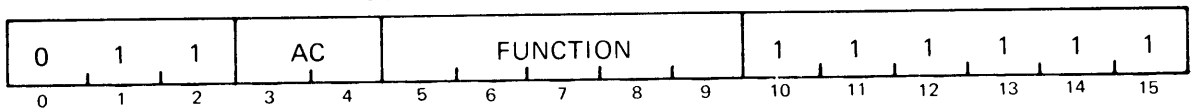
1.8 μs	001 DIA	01 S	S = START DEVICE
1.6	010 DOA	10 C	C = CLEAR DEVICE
1.8	011 DIB	11 P	P = PULSE "IOPLS" LINE
1.6	100 DOB		
1.8	101 DIC		
1.6	110 DOC		

INPUT/OUTPUT WITHOUT ACCUMULATOR



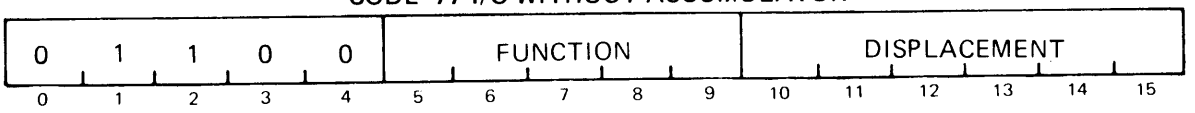
1.2 μs	00000 NIO
1.2	00001 NIOS
1.2	00010 NIOC
1.2	00011 NIOP
1.6	11100 SKPBN
1.6	11101 SKPBZ
1.6	11110 SKPDN
1.6	11111 SKPDZ

CODE-77 I/O WITH ACCUMULATOR



1.95 μs	00100 READS
1.8	01100 INTA
1.6	10000 MSKO
1.6	10001 MSKOS

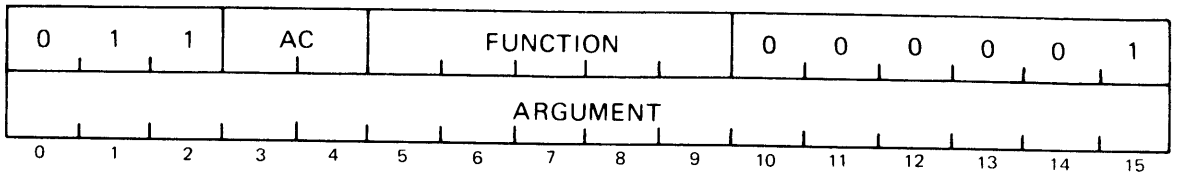
CODE-77 I/O WITHOUT ACCUMULATOR



1.2 μs	00001 INTEN
1.2	00010 INTDS
1.2	00011 CLRD
1.2	10110 IORST
1.2	11000 HALT
1.2	11100 Skip if ION set
1.2	11101 Skip if ION clear
1.2	11110 Skip if power failing
1.2	11111 Skip if power OK

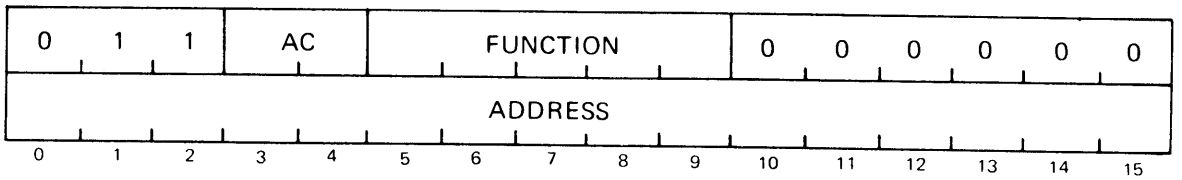
Figure 3-2. Instructions, Type I (2 of 2)

MEMORY TO ACCUMULATOR INSTRUCTIONS



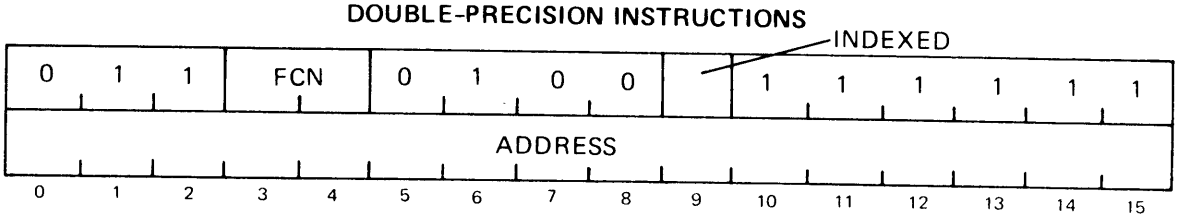
3.0 μs	00100 LDFNA
3.0	00101 ADFNA
3.0	00110 SBFNA
3.0	00111 ANFNA
3.0	01100 LDFNX
3.0	01101 ADFNX
3.0	01110 SBFNX
3.0	01111 ANFNX
2.0	10100 LDFNW
2.0	10101 ADFNW
2.0	10110 SBFNW
2.0	10111 ANFNW

ACCUMULATOR-TO-MEMORY



3.25 μs	00100 STTNA
3.25	00101 ADTNA
3.45	00110 MGTNA
3.25	00111 ANTNA
3.25	01100 STTNX
3.25	01101 ADTNX
3.45	01110 MGTNX
3.25	01111 ANTNX

DOUBLE-PRECISION INSTRUCTIONS



4.2 μs	00 DST
4.2	01 DAD
4.2	10 DNA
4.2	11 DLD

Figure 3-3. Instructions, Type II (1 of 3)

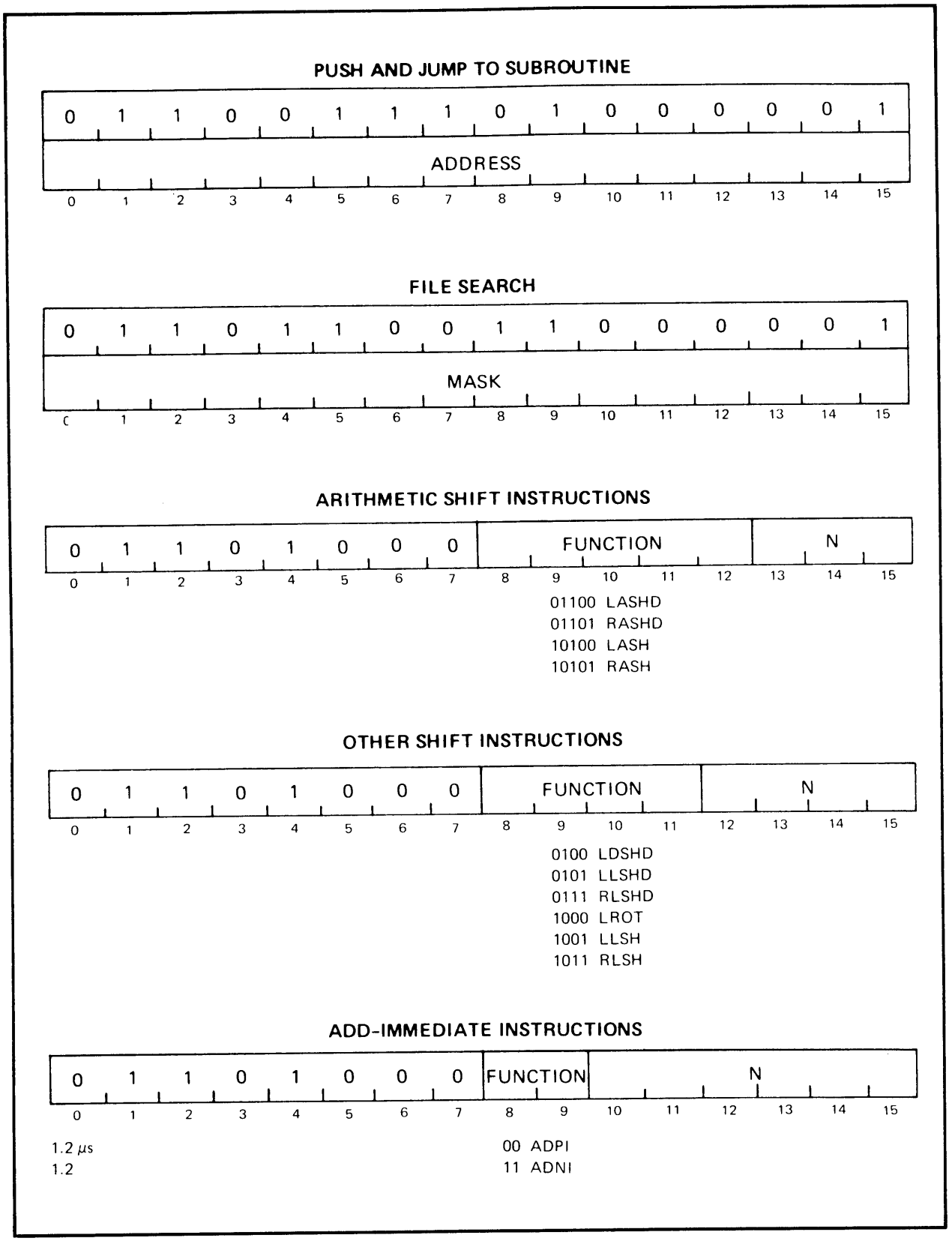


Figure 3-3. Instructions, Type II (2 of 3)

SINGLE-WORD INSTRUCTIONS
WITH ACCUMULATOR (IN BITS 3-4)

Octal Code	Operator	Execution Time (Microseconds)
061001	RSP	1.4 μs
061101	PSH	2.2
061201	POP	2.2
061277	SMPY	5.2
061301	WSP	1.4
061377	SDVD	9.2
062001	XOR	1.6
062101	IOR	1.4
062201	DEC	1.6
063001	UMPY	5.4
063101	UDVD	12.6
063201	UDVI	12.6
063301	UMPA	5.4

SINGLE-WORD INSTRUCTIONS
WITH NO ARGUMENTS

Octal Code	Operator	Execution Time (Microseconds)
060001	CLEM	2.6 μs
060101	STEM	2.6
060201	PRT	2.4
060301	RTFNI	4.4
062301	DSPD	2.8
063401	TCO	1.6
063601	STISZ	2.65
063701	PST	2.6
072301	STIBN	1.6
076301	CLIBN	1.6

Figure 3-3. Instructions, Type II (3 of 3)

less than, to 177 greater than, the addresses in PC, AC2, and AC3. If I is 1, addressing is indirect, and the processor retrieves another adddress from the location specified by the address already determined. In this new word bit 0 is the indirect bit: bits 1-15 are the effective address if bit 0 is 0. Otherwise (if bit 0 is a 1), they specify a location for yet another level of address retrieval. This process continues until some referenced location is found with a 0 in bit 0; bits 1-15 of this location are then the effective address E. However, if the Expanded Memory flag in the processor is set, at most one level of indirect addressing may be performed.

If at any level in the effective address calculation an address word is fetched from locations 00020–00037, it is automatically incremented or decremented by one, and the new value is written back whether bit 0 is 0 or 1. Addresses taken from locations 00020–00027 are incremented; those from locations 00030–00037 are decremented. When the Expanded Memory flag is set, locations 100020 through 100037 are autoindexing, i.e., they behave as do locations 00020 through 00037.

3.11 Type I Memory Reference Operations

The previous discussion described how the effective address is found from a memory reference instruction. The word stored at this location is operated upon in accordance with one of the following functions:

Instruction	Bits 0–4	Function
LDA Load Accumulator	001XX	The contents of memory location E (specified by bits 5-15 of the instruction) are loaded into ACD (the accumulator specified in bits 3-4 of the instruction).
STA Store Accumulator	010XX	The contents of ACD are stored in location E.
ISZ Increment and Skip if Zero	00010	Add 1 to the contents of location E and place the result back in E. Skip the next instruction in sequence if the result is zero.
DSZ Decrement and Skip if Zero	00011	Subtract 1 from the contents of location E and place the result back in E. Skip the next instruction in sequence if the result is zero.
JMP Jump	00000	Load E into PC. Take the next instruction from E and continue sequential operation from there.
JSR Jump to Subroutine	00001	Load an address one greater than that in PC into AC3 (hence AC3 receives the address of the location following the JSR instruction). Load E into PC. Take the instruction from location E and continue sequential operation from there.

3.12 Arithmetic-Logical (ALC) Instructions. An instruction that has a 1 in bit 0 performs one of eight arithmetic and logical functions as specified by bits 5–7 of the instruction word. The function always operates on the contents of the accumulator specified by bits 1 and 2. If a second operand is required, it comes from the accumulator addressed by bits 3 and 4.

The contents of the accumulator(s) specified are supplied to the adder, along with a carry bit, as determined by bits 10–11 of the instruction. This carry bit can be 0, 1, the contents of the CARRY flip-flop, or its complement. The adder performs the specified function on its inputs, and produces a 16-bit result plus a carry output. This main adder operation in the ALC instructions may also set the OVF flag if a signed overflow occurs. The carry bit output from the adder is identical to the carry bit supplied if there is no carry generated in the last stage of the adder (there is a carry generated in the last stage of the adder if and only if the true unsigned result of the adder function is too large to fit the 16 bits, i.e., is greater than or equal to 2^{16}). In the event that the last stage of the adder does generate a carry, the carry bit output from the adder is the complement of the bit supplied to it.

The 17-bit word consisting of the carry bit and the 16-bit result is then shifted as specified by bits 8 and 9. The shift may be a left or right one-place rotation, or a byte swap, or no operation whatever. In the left rotation, bit 0 is rotated into the carry position, the carry bit into bit 15, and all other bits move left one position. In the case of a right rotation, bit 15 is rotated into the carry position, the carry bit into bit 0, and all other bits are shifted right one position. In the case of a byte swap, the left and right 8-bit halves of the result are exchanged; the carry bit is not affected.

The shift result is then tested for a skip according to the condition specified by bits 13–15. The processor skips the next instruction if the specified condition is satisfied. The eight possible skip conditions are as follows: Never Skip, Always Skip, Skip on Zero Carry, Skip on Nonzero Carry, Skip on Zero Result, Skip if Either Carry or Result is Zero, and Skip if Both Carry and Result are Nonzero.

If bit 12 of the instruction is a 0, the shifted result is loaded into the CARRY flip-flop and the accumulator specified in bits 3–4 of the instruction. If bit 12 is a 1, neither of the accumulators nor the CARRY flip-flop are changed, although the PC may be altered as a result of the skip.

On all arithmetic-logical instructions, ACS denotes the source accumulator specified in bits 1–2, and ACD denotes the destination accumulator specified in bits 3–4. The eight arithmetic-logical functions are:

Instruction	Bits 5–7	Function
COM Complement	000	The adder output is the logical complement of the word from ACS. The carry bit output from the adder is the same as the bit supplied to the adder. COM cannot cause a signed overflow.

Instruction	Bits 5–7	Function
NEG Negate	001	The two's complement (logical complement + 1) of the word from ACS is the adder output. The carry bit output from the adder is the same as the bit supplied to the adder unless ACS held 0. Signed overflow occurs only if AC held 100000.
MOV Move	010	The output of the adder is just the word from ACS. The carry bit output is the same as the carry bit supplied. MOV cannot cause OVF to set.
INC Increment	011	The output from the adder is 1 plus the word from ACS (modulo 2^{16}). The bit in the carry position is inverted only if the contents of ACS were 177777. INC sets OVF if ACS held 077777.
ADC Add Complement	100	The logical complement of the word from ACS is added to the word from ACD. The sum modulo 2^{16} is the adder output. If the sum was greater than or equal to 2^{16}, the bit in the carry position is inverted. A signed overflow occurs only if ACD and ACS held words with different signs and the result of the operation has the same sign as the word from ACS.
SUB Subtract	101	The logical complement of the word from ACS, the word from ACD, and 1 are added together. The sum modulo 2^{16}, the bit in the carry position is inverted. OVF is set if ACD and ACS held words of opposite sign and the result of the subtraction has the same sign as the word from ACS.
ADD Add	110	The word from ACS and the word from ACD are added. The sum module 2^{16} forms the adder output. Supplies the carry bit input to the adder as the carry output unless the sum is greater than or equal to 2^{16}. Generates a signed overflow when the words in ACS and ACD have the same sign and the sum has the opposite sign.

Instruction	Bits 5-7	Function
AND AND (logical)	111	The word from ACS and the word from ACD are logically ANDed bit by bit to yield the adder output. Supplies as carry output the same value that was supplied to the adder. Cannot affect OVF.

3.13 Input/Output Instructions. This section gives a brief introduction to the 1602B programmed I/O operation and summarizes the programmed I/O instructions. A complete description of I/O operation is contained in Appendix A, which includes I/O programming, program interrupt and data channel operation, I/O bus signals and timing, and basic interface design.

Instructions in the I/O class govern all transfers of data to and from the peripheral equipment, and also perform various operations within the processor. An instruction in this class is designated by 011 in bits 0-2. Bits 10-15 select the device that is to respond to the instruction. The format thus allows for 64 codes, of which 61 can be used to address devices (octal 02-76). The codes 00 and 01 are not used for I/O, and 77 is used for a number of special functions, including reading the console data switches and controlling the program interrupt.

In general, a device interface has a 6-bit device selection network, an Interupt Disable flag, and BUSY and DONE flags. The selection network decodes bits 10-15 of the instruction so that only the addressed device responds to signals sent by the processor over the I/O bus. The BUSY and DONE flags together denote the basic state of the device. When both are clear the device is idle. To place the device in operation, the program sets BUSY. If the device will be used for output, the program must give a data-out instruction that sends the first unit of data — a word or character, depending on how the device handles information. (The word "output" used without qualification always refers to the transfer of data from the processor to the peripheral equipment; "input" refers to the transfer in the opposite direction.) When the device has processed a unit of data, it clears BUSY and sets DONE to indicate that it is ready to receive new data for output, or that it has data ready for input. In the former case, the program would respond with a data-out instruction to send more data; in the latter, with a data-in instruction to bring in the data that is ready. If the Interrupt Disable flag is clear, the setting of DONE signals the program by requesting an interrupt; if the program has set Interrupt Disable, then it must keep testing DONE or BUSY to determine when the device is ready.

On all I/O instructions, except the BUSY-DONE skips (bits 5-7 = 111), bits 8-9 specify whether a control function is to be performed, and if so, what function. Three functions are available. The start (S) function causes the CPU to pulse the STRT line in the bus. This sets BUSY and clears DONE. The clear (C) function causes the CPU to pulse the CLR line, which clears BUSY and DONE. The pulse command (P) causes the CPU to place a pulse on the IOPLS line of the bus. The IOPLS line may be used to perform miscellaneous device control functions, depending on the interface.

Bits 5-7 determine the basic input-output operation to be performed, as follows:

Instruction	Bits 3-9	Function
NIO No I/O Transfer	00000XX	Perform the control function as specified in bits 8-9 of the instruction.

Instruction	Bits 3-9	Function
DIA Data In A	XX001XX	Move the contents of the A buffer in the device interface into the accumulator specified in bits 3-4. Perform the control function specified in bits 8-9.
DIB Data In B	XX011XX	Move the contents of the B buffer in the device interface into the accumulator specified in bits 3-4. Perform the control function specified in bits 8-9.
DIC Data In C	XX101XX	Move the contents of the C buffer in the device interface into the accumulator specified in bits 3-4. Perform the control function specified in bits 8-9.
DOA Data Out A	XX010XX	Send the contents of the accumulator specified by bits 3-4 to the A buffer in the device interface. Perform the control function specified in bits 8-9.
DOB Data Out B	XX100XX	Send the contents of the accumulator specified by bits 3-4 to the B buffer in the device interface. perform the control function specified in bits 8-9.
DOC Data Out C	XX110XX	Send the contents of the accumulator specified by bits 3-4 to the C buffer in the device interface. Perform the control function specified in bits 8-9.
SKPBN Skip if BUSY is Nonzero	0011100	Skip the next instruction in sequence if the BUSY flag in the device interface is set.
SKPBZ Skip if DONE is Zero	0011101	Skip the next instruction in sequence if the BUSY flag in the device interface is clear.
SKPDN Skip if DONE is Nonzero	0011110	Skip the next instruction in sequence if the DONE flag in the device interface is set.
SKPDZ Skip if DONE is Zero	0011111	Skip the next instruction in sequence if the DONE flag in the device interface is clear.

3.14 Special Code 77 Functions. I/O instructions with the device code 77 (CPU mnemonic code) in bits 10-15 perform a number of special functions, rather than control a specific device. In all but the skip instructions and the DOA instruction, bits 8 and 9 are used to enable or

disable interrupts. The mnemonics are the same as those for controlling BUSY and DONE in I/O devices, but with code 77 they perform the following special functions. A START (S) sets the ION flag to enable the processor interrupt capability. CLEAR (C) clears the ION flag to prevent the processor from responding to interrupt requests. A PULSE (P) instruction has no effect with a code 77, other than to clear the control panel DATA display.

The I/O transfer bits 5, 6, and 7 define the function to be performed with an I/O instruction. When a device code 77 is used, the following functions will be performed.

Instruction	Bits 3–9	Function
NIO CPU Interrupt Control	00000XX	Perform the interrupt control function specified in bits 8–9.
DIA ac, CPU Read Switches	XX001XX	Read the contents of the control panel data switches into accumulator ACD (specified in bits 3–4) and perform the interupt control function specified in bits 8–9.
DIB ac, CPU Interrupt Acknowledge	XX011XX	Place the device address of the highest priority device which is requesting an interrupt into bits 10–15 of accumulator ACD. Perform the interrupt control function specified in bits 8–9.
DOB ac, CPU Mask Out	XX100XX	Set up the Interrupt Disable flags in the device interfaces according to the pattern in accumulator ACD. Each device interface is connected to a given data line, and its flag is set or cleared if the mask bit is 1 or 0. Perform the interrupt control function specified by bits 8–9.
DIC ac, CPU Clear I/O Devices	00101XX	Pulse the IORST line of the bus, and perform the interrupt control function specified in bits 8–9. This instruction is conventionally used to clear the BUSY, DONE, and Interrupt Disable flags in all devices.
DOC ac, CPU Halt	00110XX	Perform the interrupt control function specified in bits 8–9, and then halt the processor.
SKPBN CPU Skip if Interrupts are Enabled	0011100	Skip the next instruction in sequence if the Interrupt On flag in the CPU is set.
SKPBZ CPU Skip if Interrupts are Disabled	0011101	Skip the next instruction in sequence if the Interrupt On flag is clear.

Instruction	Bits 3-9	Function
SKPDN CPU Skip if Power is Failing	0011110	Skip the next instruction in sequence if the Power Failure flag is set.
SKPDZ CPU Skip if Power is OK	0011111	Skip the next instruction in sequence if the Power Failure flag is clear.

The assembler recognizes convenient mnemonics for code 77 instructions — these are listed in Paragraph 3.37, and shown in Figure 3-2.

3.15 Type II Instructions

3.16 Double-Word Memory Reference Addressing. In all of these instructions, the operation part of the instruction is contained in the first word, whereas the second word holds either data or a memory address. The memory address in the second word can be either the effective address from (or to) which the data is transferred, or it can be used to develop the effective address by means of indexing. In the case of indexed instructions, the contents of AC2 are added to the address contained in the second word of the instructions, and the resulting sum is the effective address. In the following descriptions, E denotes the effective address and ACD denotes the accumulator specified in bits 3-4 of the first word of the instruction.

3.17 Memory to Accumulator Instructions.

Instruction	Bits 5-9	Function
LDFNW Load From Next Word	10100	Fetches the second word of the instruction, and writes it into ACD. Leaves OVF and CARRY unchanged.
ADFNW Add From Next Word	10101	Fetches the second word of the instruction, and adds it into ACD. Leaves CARRY unchanged, but sets OVF if the addition involved a signed overflow.
SBFNW Subtract From Next Word	10110	Fetches the second word of the instruction, and subtracts it from ACD. Leaves CARRY unchanged, but sets OVF if the subtraction involved a signed overflow.
ANFNW AND From Next Word	10111	Fetches the second word of the instruction, and logically ANDs it into ACD. Leaves OVF and CARRY unchanged.

Instruction	Bits 5–9	Function
LDFNA Load From Next Address	00100	Fetches the word in memory location E (E is given by the contents of the second word of the instruction), and writes it into ACD. Leaves OVF and CARRY unchanged.
ADFNA Add From Next Address	00101	Fetches the word in memory location E, and adds it into ACD. Leaves CARRY unchanged, but sets OVF if the addition involved a signed overflow.
SBFNA Subtract From Next Address	00110	Fetches the word in memory location E, and subtracts it from ACD. Leaves CARRY unchanged, but sets OVF if the subtraction involved a signed overflow.
ANFNA AND From Next Address	00111	Fetches the word in memory location E, and logically ANDs it into ACD. Leaves CARRY and OVF unchanged.
LDFNX Load From Next Address, Indexed	01100	Adds the contents of AC2 to the second word of the instruction to develop the effective address E. Fetches the word in memory location E, and writes it into ACD. Leaves OVF and CARRY unchanged.
ADFNX Add From Next Address, Indexed	01101	Fetches the word in memory location E, and adds it into ACD. Leaves CARRY unchanged, but sets OVF if the addition involved a signed overflow.
SBFNX Subtract From Next Address, Indexed	01110	Fetches the word in memory location E, and subtracts it from ACD. Leaves CARRY unchanged, but sets OVF if the subtraction involved a signed overflow.
ANFNX AND From Next Address, Indexed	01111	Fetches the word in memory location E, and logically ANDs it into ACD. Leaves CARRY and OVF unchanged.

3.18 Accumulator To Memory Instructions.

Instruction	Bits 5–9	Function
STTNA Store to Next Address	00100	Develops the effective address E (E is the contents of the second word of the instruction), and stores the contents of ACD at memory location E. Leaves OVF and CARRY unchanged.

Instruction	Bits 5-9	Function
ADTNA Add To Next Address	00101	Adds the contents of ACD into memory location E. Leaves CARRY unchanged, but sets OVF if the addition involved a signed overflow.
MGTNA Merge To Next Address	00110	Uses the contents of AC1 as a mask to determine which bits of memory location E are changed. In each bit position where AC1 holds a 1, the corresponding bit of memory location E is replaced by the bit at that position in ACD. In those bit positions where AC1 holds 0's, memory location E is unchanged. Leaves OVF and CARRY unchanged. Note: MGTNA 1 performs an Inclusive-OR to memory.
ANTNA AND To Next Address	00111	Logically ANDs the contents of ACD into memory location E. Leaves OVF and CARRY unchanged.
STTNX Store to Next Address, Indexed	01100	Develops the effective address E by adding the contents of AC2 to the second word of the instruction. Stores the contents of ACD at memory location E. Leaves OVF and CARRY unchanged.
ADTNX Add To Next Address, Indexed	01101	Adds the contents of ACD into memory location E. Leaves CARRY unchanged, but sets OVF if the addition involved a signed overflow.
MGTNX Merge To Next Address, Indexed	01110	Uses the contents of AC1 as a mask to determine which bits of memory location E are changed. In each bit position where AC1 holds a 1, the corresponding bit of memory location E is replaced by the bit at that position in ACD. In those bit positions where AC1 holds 0's, memory location E is unchanged. Leaves OVF and CARRY unchanged. Note: MGTNX 1 performs an Inclusive-OR to memory.
ANTNX AND To Next Address, Indexed	01111	Logically ANDs the contents of ACD into memory location E. Leaves OVF and CARRY unchanged.

3.19 Double-Precision Instructions.

Instruction	Bits 3-9	Function
DST Double Store	0001000	Reads the second word of the instruction to develop the effective address E. Stores the contents of AC0 in memory location E, and the contents of AC1 in memory location E + 1. Leaves OVF and CARRY unchanged.
DAD Double Add	0101000	Reads the double-precision number from memory locations E and E + 1. Adds it into the double-precision quantity in AC0–1. Leaves OVF and CARRY unchanged.
DNA Double Negate and Add	1001000	Negates the double-precision quantity in AC0–1, and then adds in the double-precision number from memory locations E and E + 1. Leaves OVF and CARRY unchanged.
DLD Double Load	1101000	Reads the contents of memory location E and places it in AC0. Reads the contents of memory location E + 1, and places it in AC1. Leaves OVF and CARRY unchanged.
DSTX Double Store, Indexed	0001001	Develops the effective address E by adding the contents of AC2 to the second word of the instruction. Stores the contents of AC0 in memory location E. Stores the contents of AC1 in memory location E + 1. Leaves OVF and CARRY unchanged.
DADX Double Add, Indexed	0101001	Reads the double-precision number from memory locations E and E + 1. Adds it into the double-precision quantity in AC0–1. Leaves OVF and CARRY unchanged.
DNAX Double Negate and Add, Indexed	1001001	Negates the double-precision quantity in AC0–1, and then adds in the double-precision number from memory locations E and E + 1. Leaves OVF and CARRY unchanged.

DLDX Double Load, Indexed	1101001	Reads the contents of memory location E and places it in AC0. Reads the contents of memory location E + 1, and places it in AC1. Leaves OVF and CARRY unchanged.

3.20 Multiply and Divide Instructions.

Instruction	Function
SMPY Signed Multiply	Multiplies the contents of AC1 by the contents of ACD (the accumulator specified in bits 3–4 of the instruction). Puts the double precision result in AC0–1. All quantities are considered signed integers. Leaves OVF and CARRY unchanged.
UMPY Unsigned Multiply	Multiplies the contents of AC1 by the contents of ACD. Puts the double-precision product in AC0–1. All quantities are considered unsigned integers. Leaves OVF and CARRY unchanged.
UMPA Unsigned Multiply	Multiplies the contents of AC1 by the contents of ACD, and adds in the contents of AC0. Puts the double-precision product in AC0–1. All quantities are considered unsigned integers. Leaves OVF and CARRY unchanged.
SDVD Signed Divide	Divides the double-precision quantity in AC0–1 by the contents of ACD (normally AC2 of AC3). Puts the remainder in AC0 and the quotient in AC1. All quantities are considered signed integers. Checks for an overflow situation: Overflow occurs when the divisor is zero or the correct (mathematically) quotient is greater than or equal to 2^{15} in magnitude. If overflow occurs, sets CARRY and OVF, and leaves AC0 and AC1 unchanged. If no overflow occurs, clears CARRY.
UDVD Unsigned Divide	Divides the double-precision quantity in AC0–1 by the contents of ACD (normally AC2 or AC3). Puts the remainder in AC0 and the quotient in AC1. All quantities are unsigned integers. Checks for overflow: Overflow occurs when the contents of AC0 are greater than or equal to the contents of ACD. If overflow occurs, sets CARRY, and leaves AC0 and AC1 unchanged. If there is no overflow, clears CARRY. Leaves OVF unchanged.

Instruction	Function
UDVI Unsigned Divide,Integer	Divides the quantity in AC1 by the contents of ACD. Puts the remainder in AC0 and the quotient in AC1. All quantities are considered to be unsigned integers. Checks for overflow: Overflow occurs when the contents of ACD are 0. If overflow occurs, sets CARRY, and leaves AC0 and AC1 unchanged. Clears CARRY if there is no overflow. Leaves OVF unchanged.

3.21 Shift Instructions

These instructions shift the contents of AC0 (or the contents of AC0–1 in the case of a double-length shift) N positions to the left or right. There are four shift modes: logical, arithmetic, circular, and dual. The arithmetic shifts can be up to 7 positions long. The other shifts can be as long as 15 positions.

Instruction	Bits 8–12	Function
LLSH Left Logical Shift	1001X	Performs a logical left shift of n positions ($0 \leq n \leq 15$) on the contents of AC0. Zeros are shifted in on the right, bits shifted out on the left are lost. CARRY and OVF are unchanged.
LLSHD Left Logical Shift, Double	0101X	Performs a logical left shift of n positions ($0 \leq n \leq 15$) on the double-precision quantity in AC0–1. Zeroes are shifted into the right of AC1. Bits shifted out of AC1 on the left shift into AC0 on the right. Bits shifted out of AC0 are lost. CARRY and OVF are unaffected.
RLSH Right Logical Shift	1011X	Performs a logical right shift of n positions ($0 \leq n \leq 15$) on the contents of AC0. Zeros are shifted in on the left; bits shifted out on the right are lost. CARRY and OVF are unchanged.
RLSHD Right Logical Shift, Double	0111X	Performs a logical right shift of n positions ($0 \leq n \leq 15$) on the double-precision quantity in AC0–1. Zeros are shifted into AC0. Bits shifted out of AC1 are lost. CARRY and OVF are unchanged.
LASH Left Arithmetic Shift	10100	First checks for an overflow situation: overflow occurs when the leftmost $n+1$ ($0 \leq n \leq 7$) bits of AC0 are not all the same. If an overflow occurs, sets OVF and CARRY, and leaves AC0 unchanged. If no overflow occurs, clears CARRY and shifts AC0 left n positions. Zeros enter AC0 on the right.

Instruction		Function
LASHD Left Arithmetic Shift, Double	01100	First checks for an overflow situation: overflow occurs when the leftmost n + 1 ($0 \leq n \leq 7$) bits of AC0 are not all the same. If an overflow occurs, sets OVF and CARRY, and leaves AC0 and AC1 unchanged. If no overflow occurs, clears CARRY and shifts AC0–1 left n positions. Zeros enter AC1 on the right. Bits shifted out of AC1 enter AC0.
RASH Right Arithmetic Shift	01101	Performs a right arithmetic shift of n positions ($0 \leq n \leq 7$) on the contents of AC0–1. If AC0 is positive, 0's are shifted into AC0; if AC0 is negative, 1's are shifted in. Bits shifted out of AC0 enter AC1. CARRY and OVF are unchanged.
RASHD Right Arithmetic Shift, Double	01101	Performs a right arithmetic shift of n positions ($0 \leq n \leq 7$) on the contents of AC0–1. If AC0 is positive, 0's are shifted into AC0; if AC0 is negative, 1's are shifted in. Bits shifted out of AC0 enter AC1. CARRY and OVF are unchanged.
LROT Left Rotate	1000X	Performs a left circular shift of n positions ($0 \leq n \leq 15$) on the contents of AC0. Bits shifted out of AC0 on the left enter on the right. CARRY and OVF are unchanged.
LDSHD Left Dual-Mode Shift, Double	0100X	Shifts AC0 left logically n positions ($0 \leq n \leq 15$). Places the result into AC1. Restores the original contents of AC0. Rotates AC0 left n positions. Leaves CARRY and OVF unchanged.

3.22 Stack Instructions

These instructions facilitate the use of a last-in first-out file in main memory. The address of the last file location written, or stack pointer (SP), is contained in a hardware register in the central processor. The SP is automatically incremented at the end of pop-type operations, and decremented at the beginning of push-type operations. The stack is filled in descending memory locations, i.e., if the pointer is initialized at 500, then the first data pushed will go into location 477, the next into 476, and so on.

Stack overflow is checked for on all push-type operations (the PSH, PJS, and PST instructions, as well as the nesting interrupt sequence). Stack overflow occurs when the stack pointer has been decremented to contain an address smaller than 420_8. In the event of a stack overflow the push operation is completed, but the normal instruction sequence is not followed. Instead the ION flag is cleared, thus disabling interrupts. The address of the next instruction that would normally be executed is stored in main memory location 44, and a JMP@45 is executed.

Instruction	Function
WSP Write Stack Pointer	Moves the contents of ACD to the SP register. Does not test for stack overflow.
RSP Read Stack Pointer	Moves the contents of the SP register to ACD.
PSH Push Accumulator onto Stack	Decrements SP and stores the contents of ACD in the memory location whose address is held in SP. Tests for stack overflow, and enters the stack overflow sequence if appropriate.
POP Pop Accumulator From Stack	Reads from the memory location whose address is held in SP. Places the memory data into ACD. Then increments SP.
PJS Push and Jump to Subroutine	Decements SP. Stores PC + 2 (i.e., a number 2 greater than the address of the first word of the PJS) into the memory location whose address is contained in SP. Goes next to the instruction whose address is held in the second word of the PJS. Tests for stack overflow.
PRT Pop and Return	Moves the contents of the memory location addressed by SP into PC, then increments SP. The next instruction to be executed is at the address that was popped from the stack.
STISZ Increment Top Element of Stack, Skip if Zero	Adds 1 to the main memory location whose address is held in SP. Leaves SP unchanged. If the incremented data is zero, skips the next instruction.
PST Push Status	Decrements SP and stores the CPU STATUS word in the main memory location addressed by SP. Tests for stack overflow.

Note: The format of the STATUS word is as follows:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ION	IBN	OVF	CAR-RY	EM	SC	1	1	1	1	1	1	1	1	0	0

Bit SC of the STATUS word is a 1 if the last memory access was to semiconductor memory. DMA is inactive, and bit SC is a 1 if the PST instruction itself resided in semiconductor memory.

3.23 Interrupt and Expanded Memory Mode Control Instructions

Instruction	Function
STEM Set Expanded Memory Flag	Set the Expanded Memory flag (EM). This will cause the 1602B to operate in such a way that it can address up to 64K of main memory. In particular, having EM set will disable the multilevel indirect addressing capability, and will allow the PC register to hold a 1 in bit 0. When EM is set, compatibility with other processor models is lost.
CLEM Clear Expanded Memory Flag	Clear the Expanded Memory flag (EM). This enables the multilevel indirect addressing capability, causes bit 0 of PC to be held to zero, and causes bit 0 of all addresses sent to memory to be forced to zero. Note: EM is clear on power-up and after the RESET switch is depressed.
STIBN Set Interrupt Branch/Nest Flag	Set the IBN flag, causing branching interrupt sequences.
CLIBN Clear Interrupt Branch/Nest Flag	Clear the IBN flag, causing standard interrupt sequences. Note: IBN is clear on power-up and after the RESET switch is depressed.
RTFNI Return from Nested Interrupt	Pop the previous mask from the stack, store it in location 5, and use it to get interrupt masks in devices. Then pop the previous PC from the stack into PC and fetch the next instruction from that address. Leave ION unchanged.

3.24 Special Instructions

Instruction	Function
ADPI Add Positive, Immediate	Adds the quantity n ($0 \leq n \leq 77_8$) to AC2. Does not affect OVF or CARRY.
ADNI Add Negative, Immediate	Adds to AC2 the quantity $n - 100_8$, where n is the range 0 to 77_8. Does not affect OVF or CARRY. ADNI allows a number in the range -100_8 to -1_8 to be added to AC2.

Instruction	Function
XOR Exclusive OR	Computes the logical Exclusive-OR function of the contents of AC0 and the contents of ACD. Places the result into ACD. Does not affect OVF or CARRY.
IOR Inclusive OR	Computes the logical Inclusive-OR function of the contents of AC0 and the contents of ACD. Places the result into ACD. Does not affect OVF or CARRY.
DEC Decrement Accumulator	Decreases the contents of ACD by one. Does not affect OVF or CARRY.
TCO Test and Clear OVF	Clears OVF flag. If OVF was already clear, skips the next instruction. If OVF was set, does not skip.
DSPD Display Data	Writes the contents of AC1 into the control panel Data Display register. This quantity will remain in the CP DATA lights until one of the following occurs: (1) a CLRD-type instruction is executed, (2) another DSPD instruction is executed, (3) the processor halts; when the program resumes after a halt (whether due to a HALT instruction or to some control panel operation), the quantity in the DATA lights is lost.
FS File Search	Searches a file whose first address is one greater than the contents of AC2, and whose last address is contained in AC3. Masks each word of the file (with the mask held in the second half of the FS instruction), and then checks to see whether it is within a specified range given by AC0 and AC1. If a match is found, it skips the next instruction and exits with AC2 holding the address of the matching file entry. If no word in the file meets the requirements, it does not skip an instruction, but sets AC2 to the last address of the file. More precisely: Fetches the MASK from memory location PC + 1, then iterates the following sequence of events: Compares the contents of AC2 and AC3. If they are equal, then the file has been completely searched, and the next instruction is fetched from PC + 2. If AC2 and AC3 are unequal, increments AC2. Fetches the main memory data with the MASK. Compares the masked data with the contents of AC0 and AC1. If C(AC0) ≤ MASKED DATA ≤ C(AC1), fetched the next instruction from PC + 3. Otherwise, again compares the contents of AC2 and AC3, and proceeds as before.

3.25 BEHAVIOR WHEN PRIMARY POWER IS LOST OR RESTORED

The 1602B includes as standard equipment a Power Monitor and Autorestart capability. The Power Monitor allows an executing program to perform an orderly shutdown (CPU first, then all I/O devices) when input power is interrupted. Autorestart allows a program to resume automatically after power is restored. This section discusses the software aspects of the Power Monitor and Autorestart.

3.26 Power Monitor

The power supply senses the interruption of input power. This causes the Power Failure flag to be set in the processor. The power supply stores sufficient energy to allow the program to run for at least 500 microseconds after the Power Failure flag is set.

The program can check the state of the Power Failure flag at any time by means of the code 77 instructions SKPDN CPU and SKPDZ CPU. The former instruction skips if and only if the flag is set; the latter skips when the flag is clear.

The setting of the Power Failure flag causes an interrupt to be requested. This interrupt will be granted if ION is set. The program normally responds to a power failure interrupt by storing the contents of volatile registers in memory, and then executing a HALT instruction. If the program does not execute a HALT, the processor will be unconditionally halted before the power levels become dangerously low.

The power failure interrupt request responds to INTA with a word of all zeros. Thus, a power failure interrupt appears like an interrupt from I/O device 00.

The INTA (daisy-chaining) priority of a power failure interrupt will be lowest priority for standard interrupts. For simple branching and branch and next interrupts it will be highest priority. The software can make the standard interrupts give effective highest priority to power failure interrupts by testing the Power Failure flag when servicing interrupts.

3.27 Behavior When Power is Restored

The restoration of power to the processor causes a general reset to occur. This will clear the ION, IBN, and EM flags, and send an IORST signal out on the I/O bus. The processor may start up either running or halted, dependent upon the setting of the power switch on the control panel.

If the power switch is in the ON position, the processor will start up halted. The state of the accumulators, PC, stack pointer, CARRY flag, and OVF flag will be indeterminate.

If the power switch is set to LOCK, or if no control panel is attached, the processor will start up running. The state of the accumulators, etc., will again be indeterminate. When the power switch is in the LOCK position, the processor will normally start running by executing the instruction at location 0.

3.28 NUMBERING REPRESENTATIONS AND CONVENTIONS

3.29 Binary and Octal Representations

A light on the control panel represents a "1," or "yes" condition, when it is lit. It represents a binary "0," or a "no" condition, when it is off. A DATA switch represents binary "1" when it is up, and binary "0" when it is down. A switch in the up position is said to be set.

Binary quantities are written and read from left to right. For example, to place the binary quantity 1010110100100000 in the data switches, one would set DATA switches 0, 2, 4, 5, 7, and 10 up, and the rest of the switches down.

An equivalent but more compact representation for binary quantities is the octal format. To convert from binary to octal representation, the following procedure should be followed. Starting at the right-hand end of the binary quantity, group it into sets of three bits each. If necessary, add one or two zeros at the left so there will be no additional bits left over. Then, to each of the groups of three bits, assign the appropriate octal digit (from 0 to 7), as given in the correspondence list shown below:

Binary	Octal
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

For example, to convert 0101010110010001 to octal, one breaks the number into six groups of three bits (adding two 0's at the left).

000 101 010 110 010 001

Then the various groups of three bits are each converted to octal digits in the same order. Thus the binary number in this example becomes the octal number 052621.

To convert from octal to binary, the procedure is simply reversed. For example, to convert 126440 (octal) to binary, use the binary-octal conversion data given earlier. The conversion will appear as follows:

1	2	3	4	0	
001	010	110	100	100	000

Drop the two leftmost zeros since the processor uses only 16 bits. Thus, octal 126440 represents binary 1010110100100000.

Since addresses are often restricted to being less than 32K (2^{15}), addresses are frequently written using five octal digits. The ASCII code (Table 3-2) requires seven bits, and therefore each code is written using three octal digits.

3.30 Representation of Single- and Double-Precision Numbers

By using the standard binary representation, a 16-bit word can represent unsigned integers in the range 0 to 65535. To represent signed numbers, the two's complement convention is utilized. This allows integers in the range −32768 to +32767 to be represented with one 16-bit word.

Two 16-bit words together can be used to represent much larger numbers in the range 0 to 4294967295, or signed numbers in the range −2147483648 to +2147483647. Such numbers, called double-precision integers, are represented either in two accumulators or in two memory locations. The most significant half of the number is conventionally in AC0, AC2, or the lower numbered memory location. The least significant half is in AC1, AC3, or at the next higher memory address. Signed double-precision numbers are represented by means of the two's complement convention applied to 32-bit quantities.

3.31 SYSTEM SOFTWARE

Software used with the Model 1602B Processor is listed in the *Software Catalog*. Pertinent instructions for operation, programming, and diagnostic troubleshooting is contained in the *Programmer's Reference Manual*, number 493-150053.

3.32 ASSEMBLY LISTING FORMAT SUMMARY

In operation and maintenance of the ROLM Model 1602B Processor, it is frequently necessary to refer to assembly listings of programs. This section provides a brief summary of the assembly listing format.

For an assembly listing, a typical line contains, in order, the memory location of the instruction word, the octal encoding of the instruction, and the instruction as it appeared on the original program tape. For example, the line

```
03700   004757   BLOCK:    JSR GTCHR        ;GET A CHARACTER
```

indicates that memory location 03700 (octal) contains octal word 004757, which is the encoding of the JSR GTCHR instruction.

3.33 Mnemonic Instruction Format

The mnemonic form of an instruction word contains up to four fields. From left to right, they are: label field, operation field, operand field, and comment field.

Table 3-2. ASCII Code

7-Bit Octal Code	Character	7-Bit Octal Code	Character	7-Bit Octal Code	Character
000	NUL	053	+	126	V
001	SOH	054	,	127	W
002	STX	055	–	130	X
003	ETX	056	.	131	Y
004	EOT	057	/	132	Z
005	ENQ	060	0	133	[
006	ACK	061	1	134	\
007	BEL	062	2	135	]
010	BS	063	3	136	↑
011	HT	064	4	137	←
012	LF	065	5	140	`
013	VT	066	6	141	a
014	FF	067	7	142	b
015	CR	070	8	143	c
016	SO	071	9	144	d
017	SI	072	:	145	e
020	DLE	073	;	146	f
021	DC1	074	<	147	g
022	DC2	075	=	150	h
023	DC3	076	>	151	i
024	DC4	077	?	152	j
025	NAK	100	@	153	k
026	SYN	101	A	154	l
027	ETB	102	B	155	m
030	CAN	103	C	156	n
031	EM	104	D	157	o
032	SUB	105	E	160	p
033	ESC	106	F	161	q
034	FS	107	G	162	r
035	GS	110	H	163	s
036	RS	111	I	164	t
037	US	112	J	165	u
040	SP	113	K	166	v
041	!	114	L	167	w
042	"	115	M	170	x
043	#	116	N	171	y
044	$	117	O	172	z
045	%	120	P	173	{
046	&	121	Q	174	|
047	'	122	R	175	}
050	(	123	S	176	~
051	)	124	T	177	DEL
052	*	125	U		

If a label field is present, it is the leftmost field, and is terminated with a colon. For example, in the instruction shown above, the label field is BLOCK. The presence of a label field "attaches" the label to the instruction. That is to say, the label is defined as a symbolic abbreviation for the address of the instruction (e.g., 03700).

The operation field contains the basic operation mnemonic, and sometimes some option mnemonics as well. In the above example, the operation field is JSR, and says that the instruction is a Jump-to-Subroutine instruction.

The argument field supplies the remaining information that is needed to complete the instruction. If the argument field contains several subfields, they are separated by commas. In the given example, the argument field indicates that the JSR instruction is to jump to the location defined by GTCHR. As an example, GTCHR might be defined elsewhere as a symbolic equivalent of location 03657.

The comment field begins with a semicolon and occupies the rest of the line. The comment field is often used by the programmer to describe the instruction. For example, the comment can descibe the JSR GTCHR instruction as causing the computer to get a character (from a peripheral device).

3.34 Type I Memory Reference Instruction Format

For memory reference instructions, the operation field contains the basic operation mnemonic, and nothing else. The argument field of a memory reference instruction may contain several subfields. The LDA and STA instructions specify an accumulator in the first subfield of the argument field. The rest of the argument field specifies the address. The ISZ, DSZ, JSR, and JMP instructions specify only an address in the argument field.

The address may be specified in several ways. One way is to directly supply the address or its equivalent. In such a case, the generated instruction word may use either page zero (X = 00) or relative (X = 01) addressing. An example would be:

```
JMP     371
```

If indexing is desired, the address format includes the displacement field (D) and then the index field. For example,

```
LDA     2, 103, 3
```

would specify an instruction to load accumulator 2 from the memory word whose address is 103 (octal) greater than the quantity in accumulator 3 (D = 103, X = 11 for AC3 index register).

In any memory reference instruction, indirect addressing is specified by the appearance of an "@" character anywhere in the operand or arguments field. For example,

```
LDA@  2,103,3     or
LDA   2,@103,3
```

would yield the same instruction as without the "@", except that bit 5 (I) would contain a 1, and thus addressing is indirect.

3.35 Arithmetic-Logical Instruction Format

Several options of the arithmetic-logical instructions are specified in the operation field. The format of the operation field is given below.

Basic Operation	Carry Setup Option	Shift Option	No Load Option
COM			
NEG			
MOV	None	None	
INC	Z	L	None
ADC	O	R	#
SUB	C	S	
ADD			
AND			

Thus INCOS# in the operation field would describe an increment operation, such that a carry bit of 1 was supplied, the resultant bytes were swapped, and the no-load option was enabled. Similarly, SUBL would specify a subtract operation such that the carry bit supplied was the contents of the CARRY flag, the result was rotated left, and the results were loaded.

The argument field of an arithmetic-logical instruction contains either two or three subfields. The first subfield specifies the source accumulator (bits 1–2). The second subfield specifies the destination accumulator (bits 3–4). Both of these subfields are obligatory. The third subfield specifies the skip condition. The absence of a third subfield indicates that the instruction should never skip. For example, the ADCZ 3,2,SNC specifies an ADC instruction with supplied carry bit = 0. The source accumulator is AC3, and the destination accumulator is AC2. The skip condition is Skip on Nonzero Carry.

3.36 Input/Output Instruction Format

All I/O instructions specify a device address. A control function and accumulator are sometimes specified also. On all I/O instructions except the I/O skips, a control function (Start, Clear, Pulse, or none) may be specified. If a Start, Clear, or Pulse function is desired, an "S," "C," or "P" is appended to the operation mnemonic. Thus a data-out-A instruction with a start pulse may be described by the mnemonic DOAS.

The argument field of an I/O instruction usually consists of an accumulator number followed by a device address. The NIO and in-out skip instructions, however, do not specify an accumulator. Thus the following are legitimate instruction mnemonics:

DIAC	0,10	NIOC	22
DOAS	2,11	SKPDZ	77

Certain mnemonic abbreviations are often used for standard peripheral devices. The meanings of the mnemonics are generally obvious (e.g., PTR for paper tape reader, etc.).

3.37 Code 77 I/O Mnemonics

Several mnemonics are used for certain code 77 I/O functions; these are:

READS ac	is equivalent to DIA ac, 77
IORST	is equivalent to DICC 0, 77
HALT	is equivalent to DOC 0, 77
INTEN	is equivalent to NIOS 77
INTDS	is equivalent to NIOC 77
CLRD	is equivalent to NIOP 77
INTA ac	is equivalent to DIB ac, 77
MSKO ac	is equivalent to DOB ac, 77
MSKOS ac	is equivalent to DOBS ac, 77

3.38 Double-Word Instructions

All double-word instructions require two lines of assembly language input. The first line specifies the first word of the instruction, and the second line specifies the second word. Thus the following pairs specify double-word instructions.

ADFNX 3	DLD	PJS	FS
535	D1	SBRT3	177777

3.39 Other Mnemonics

Occasionally there will be certain mnemonics that will be difficult to interpret in a limited context. In some cases it is possible to examine the octal instruction encoding to determine what the instruction will do.

SECTION IV
THEORY OF OPERATION

4.1 INTRODUCTION

The theory of operation for the ROLM Model 1602B Processor is divided into five sections:

1. Power Input, Paragraphs 4.2 through 4.4.
2. DC Power Supply, Paragraphs 4.5 through 4.14.
3. Core Memory, Paragraphs 4.15 through 4.41.
4. Control Panel, Paragraphs 4.42 through 4.50.
5. Central Processing Unit (CPU), Paragraphs 4.51 through 4.53.

Appendix A contains interface information for the CPU. It includes an applications-oriented theory of operation for generalized Input/Output (I/O) device controllers. If optional items have been installed in the processor system before shipment, an applicable theory of operation for each is found in Appendices B or D (I/O Options) or Appendix C (Processor Options).

4.2 POWER INPUT

4.3 Fusing

Power is separately fused for ac and dc input. DC input is protected by fuses F1 and F2 (30A). Fuses F3 and F4 are reserved for processor configuration with an ac power supply.

4.4 Filtering

A line filter (Figure 5-6) is connected between the fuses and the power supply to reduce conducted interference on the input supply lines.

4.5 DC POWER SUPPLY

4.6 Introduction

The Model S665 Power Supply operates from a dc voltage in the range of 20 to 36 volts (measured at the input to the power supply); transient behavior is in accordance with MIL-STD-704B.

A pulse-width modulated chopper converts the dc input voltage to an ac voltage, which is transformer-coupled to the loads. Isolation from load to line is provided by the chopper transformer and by floating the chopper control circuits at line potential. Coupling from the load circuits back to the chopper control circuits is accomplished through optical isolators.

4.7 Theory of Operation

A block diagram of the supply is shown in Figure 4-1. Referring to this diagram, the input is connected to the center tap of chopper transformer T1. It is also fed to a control regulator, which generates a 5 Vdc output that powers the control circuits. Note that this control voltage is referenced to the dc input return, which may or may not be at logic ground potential.

The dc input is converted to an ac voltage by the 10 kHz chopper. The chopper output is coupled through a transformer to generate regulated outputs of ±15, −6, and +5 Vdc. The +5V output is compared to a stable reference voltage in a comparator, and the resultant error voltage is coupled through an optical isolator to the chopper control circuits where it is used to regulate the width of the chopper pulses. Regulation of the output dc voltages is achieved by chopping at a constant frequency and varying the ration of *on* to *off* time as the dc input or load currents vary. Since only the +5V output is sensed (and thus tightly regulated), postregulators are used to generate ±12 Vdc and −5 Vdc outputs from the coarsely regulated ±15 Vdc and −6 Vdc outputs.

The voltage monitor circuits include undervoltage sensors to facilitate the power monitor/autorestart feature, and overvoltage sensors used to halt the chopper in the event of an overvoltage condition on either input or output.

The circuits used are described in the paragraphs that follow. Components, assemblies, interconnections, and interface connector details are illustrated in schematic diagram 00-110920.

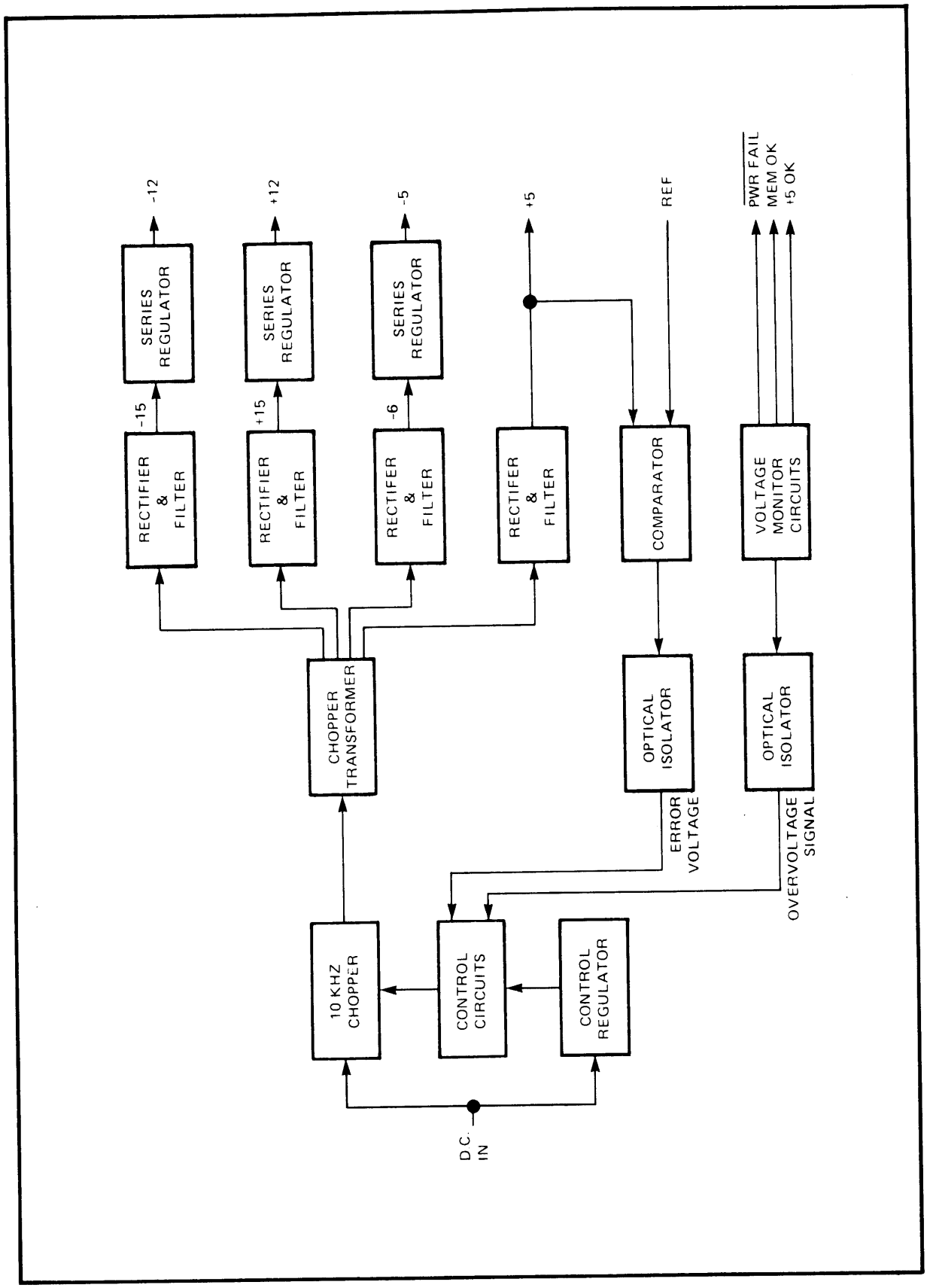


Figure 4-1. Block Diagram, Model 5686 Power Supply

4.8 Input Filter. Two 2300 μf capacitors (C78 and C79) provide filtering and energy storage for power-fail shutdown (Paragraph 3.26). In addition, a 760 μf capacitor (C75) is connected across the input to the control regulator.

4.9 Control Regulator. Voltage regulator U8, transistor Q7, and associated components comprise a voltage regulator that generates a 5 Vdc output to power the circuits that control the chopper.

4.10 Chopper. Chopper transistors Q5 and Q6 are operated in push-pull fashion to alternately connect the 28 Vdc input to one side of the primary of T1 and then to the other. These transistors are operated as switches, i.e., when conducting, they are driven to the verge of saturation. The chopping signal, which is pulse-width modulated by the output from U5, is coupled to Darlington transistors Q5 and Q6 by U1, U4, and U7. The chopping rate is 10 kHz, with a maximum pulse width of 47 μs. The NAND gates of U1 gate the chopping signals in such a manner that bidirectional base drive current is produced for the Darlingtons. U4 contains two PNP transistor pairs (each pair connected in parallel) that provide base drive to the upper NPN transistor of each totem-pole connected transistor pair of U7. This transistor provides base drive to turn the Darlingtons on. The lower NPN transistor of the totem-pole pair, driven from the NAND gates of U1, provides negative base current to turn the Darlingtons off.

Darlington transistors Q5 and Q6 require about 40 mA of base drive current, which is controlled as follows. The collectors of each U4 PNP transistor pair are connected through diodes CR42 and CR44 to the collectors of Q5 and Q6. These diodes clamp the collector voltage to approximately the value at the base, which prevents the collector-base junction from forward-biasing and thus causing transistor saturation.

The outputs of transformer T1 are alternating pulses with amplitudes related to the 28 Vdc input by the turns ratios and widths equal to the widths of the chopper drive pulses. Rectification of these pulses yields a pulse train with an average dc value equal to the product of the duty factor (ratio of the pulse width to the 50 μs period between pulses) and the pulse amplitude.

4.11 Control Circuits. Oscillator U3 sets the chopper rate. It generates a 20 kHz sawtooth output at pin 10 and a TTL-compatible logic output at pin 4. The level at pin 4 is low when the sawtooth slope is negative and high when the slope is positive. A chopping signal is generated by comparing this sawtooth to a dc error voltage in comparator U6. This chopping signal is commutated from one Darlington to the other by a flip-flop (½ of U2), which is clocked by the oscillator logic output. The dc error voltage, which is generated by comparing the +5 Vdc output to a stable reference in U11, is coupled to pin 10 of U6 by an optical isolator, U9.

The other half of U2 is used as a latch to inhibit generation of the chopping signal by pulling pin 10 of U6 to a level lower than the minimum sawtooth potential. This latch is set by this overvoltage signal coupled through optical isolator U9. It may also be set by the overcurrent sensor (¼ of comparator U6), which monitors the sum of the Darlington emitter currents. The latch is reset by the output of another comparator (¼ of U6), which generates a pulse each time power is turned on.

4.12 Five-Volt Output. Rectifiers CR63 and CR65, together with the choke input filter consisting of L1 (in the A6 Magnetics Assembly), C73, and C74, produce a 5 Vdc output from the alternating pulses present at the secondary of T1. This voltage is compared to the internal Zener reference in

U11, and the resultant error voltage is coupled through optical isolator U9 to comparator (¼ of U6), which generates the pulse-width modulated chopping signal. Inspection will show that a rise in the 5 Vdc output would cause an increase in photodiode current, a decrease in the error voltage at pin 10 of U6, a decrease in the pulse width into U1, and the desired reduction in duty factor and 5 Vdc output.

4.13 Other Outputs. A negative 6 Vdc output is generated from the same secondary by CR61 and the filter consisting of L3 (in the A6 Magnetics Assembly), C63 and C64. It, in turn, produces the regulated −5 Vdc output through the series regulator consisting of Q13, one NPN transitor in U12, two transistors in U14, and the associated passive components.

Similarly, another secondary is used to generate ±15 Vdc outputs which are fed to series regulators to provide the ±12 Vdc regulated outputs.

4.14 Voltage Monitor Circuits. A voltage generated by a peak-detector consisting of CR21, CR22, and C38 connected to the 5 Vdc secondary is used to generate the $\overline{\text{PWR FAIL}}$, MEM OK, and +5 OK signals. During the power-on transient, this voltage is clamped by CR24 to the 5 Vdc output, preventing this output from rising until all voltages are at their proper levels. During the power-down transient, $\overline{\text{PWR FAIL}}$ drops when the peak-detector voltage (which is proportional to the voltage stored on capacitors C78 and C79) drops to a level indicating that insufficient energy is stored to maintain computer operation for more than one-half millisecond. MEM OK drops one-half millisecond later and is followed by +5 OK.

The overvoltage sensors consisting of VR11, VR12, and VR13 sense when the peak detector maximum voltage, +5 Vdc, or +12 Vdc output exceeds a preset limit and shuts the chopper down via an optical isolator of U9 and a flip-flop of U2. Temperature-sensing resistor R22 will also cause the supply to shut down if the internal temperature exceeds 105 °C.

4.15 CORE MEMORY, 16K

The Model 2011 core memory is a 3-D, 3-wire coincident-current memory packaged in 16K x 16-bit modules. Nominal cycle times are 1.0 μs for the read-restore or clear-write cycles. Eighteen-mil lithium cores are used in the planar stack to permit operation over the specified range of −55° to +95°C. Each module has complete read/write electronics and is internally temperature-compensated. Timing signals are provided by the CPU over the memory bus. Regulated supply voltages of ±12V and +5V are provided by the system power supply.

4.16 Organization

Core memories utilize the remanent property of nonlinear magnetic materials; i.e., if saturation flux density (Bs) is produced in a ferrite core by an applied field, the residual flux density (Br) after the field is removed will be only slightly below the saturation level. Binary information is stored by driving a core to positive or negative saturation (a residual flux density of +Br is defined as a binary 0, and −BR as a 1). Information is retrieved from a core by driving it toward +Bs and observing the voltage across a winding threading the core. A core in the

stored-zero state undergoes only a slight change in flux density (Bs − Br) and induces a very small voltage in the output winding, but a core in the stored-one state has a much large flux-density change (Bs + Br) and a correspondingly larger induced output voltage. Since interrogating a core places it in the stored-zero state, each read operation must be followed by a write operation to restore the information or to insert new or modified information.

Ferrites exhibit a second useful nonlinear property that makes coincident-current memories possible. The B-H loop is square; i.e., a threshold field exists which must be exceeded before any significant change in flux density can occur. For a given core material and geometry, there is a corresponding threshold current, Isw, which must link the core aperture before the core can be switched. Isw may flow in a single wire or it may be the algebraic sum of currents flowing in several wires through the core. A total of +Isw must flow for a time Tsw to switch the core from −Bs to +Bs (switch from a stored 1 to a stored 0). conversely, the currents must total −Isw for a time Tsw to return the core to the 1 state, −Br.

A 16k x 16-bit core mat consists of 16 identical bit planes. Each bit plane contains 16,384 cores arranged in a planar array of 128 rows by 128 columns. Each core is threaded by three wires: one of 128 Y-drive lines, one of 128 X-drive lines, and a sense-inhibit (Z) line that threads all cores in a bit plane. Each X-drive line is series connected to equivalent lines in the other 15-bit planes, as is each Y-drive line. The 16 Z lines are independent. Thus, a 16-bit word location (one core in each bit plane) is uniquely identified by a 7-bit X address and a 7-bit Y address, which are decoded, respectively, to select one of the 128 X-drive lines and one of the 128 Y-drive lines.

A word location is interrogated by sending partial read current pulses of amplitude Isw/2 and duration Tsw down the appropriate X- and Y-drive lines. Each of the 16 selected cores at the intersections of the driven lines thus is linked to a total current of +Isw, and will be driven to the zero state. A core that was previously in the one state produces an output voltage on its Z line that is sensed as a 1 stored in a data register. A core that was in the zero state produces a negligible output, so its state is recorded in the data register as a 0. Cores on the driven X and Y lines but not at the intersections are referred to as half-selected, since they are linked by a current +Isw/2, which is insufficient to cause switching. Unselected cores are those not linked by either line.

The subsequent write operation consists of sending current pulses of −Isw/2 (i.e., identical in magnitude and duration but opposite in direction to the partial read currents) through the X- and Y-drive lines. Each selected core receives a current of −Isw, which is sufficient to switch it to the one state. Those cores that are to store 1's (as determined by the bit pattern in the data register) receive only the X- and Y-drive currents. A core that is to store a 0 receives a coincident inhibit current pulse of +Isw/2 that is sent through the sense-inhibit wire. The algebraic sum of the three current pulses is thus only −Isw/2, and the core remains in the zero state.

Figure 4-2 illustrates the organization of a 16K memory module. A 16-bit register stores 14 bits that specify the word location and 2 bits that identify the module. X and Y decoders select the appropriate X- and Y-drive lines that are connected to the read and write (R/W) cur-

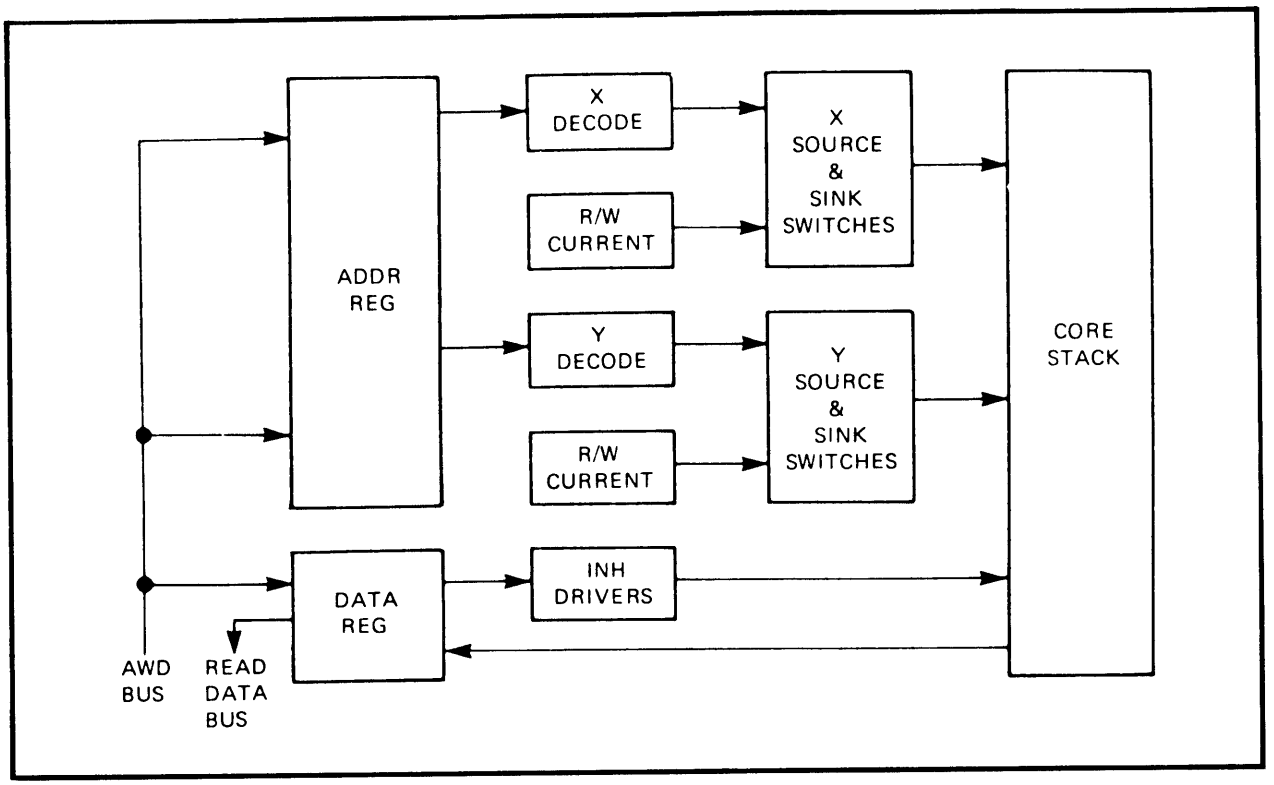


Figure 4-2. Simplified Block Diagram, 16K Core Memory Module

rent generators by the source and sink switches. A 16-bit data register stores the word retrieved from memory during the read operation and enables the appropriate inhibit current generators during the write operation. The AWD (Address Write Data) bus carries the address to the address register and write data to the data register when it is desired to alter the contents of the addressed location. Data read from memory are placed on the Read Data bus upon command from the CPU.

4.17 Timing

Operation of the memory is controlled entirely by timing signals generated in the memory-controller portion of the CPU and fed in parallel to all memory modules. Figure 4-3 shows the time relationship of these signals, which (except for READ) are all active low. Read-Modify-Write exemplifies memory operation; Read-Restore is a special case of this basic cycle.

Each memory cycle begins with the CPU placing a memory address on the AWD bus and issuing a strobe, $\overline{\text{MAST}}$, which loads all memory address registers. Bits 0 and 1 of the addresses are decoded by the desired module to generate a module-select (MOSL) signal which gates all the other timing signals into the selected module. Bits 2–8 are decoded to select the X-drive line and bits 9–15 to select the Y-drive line.

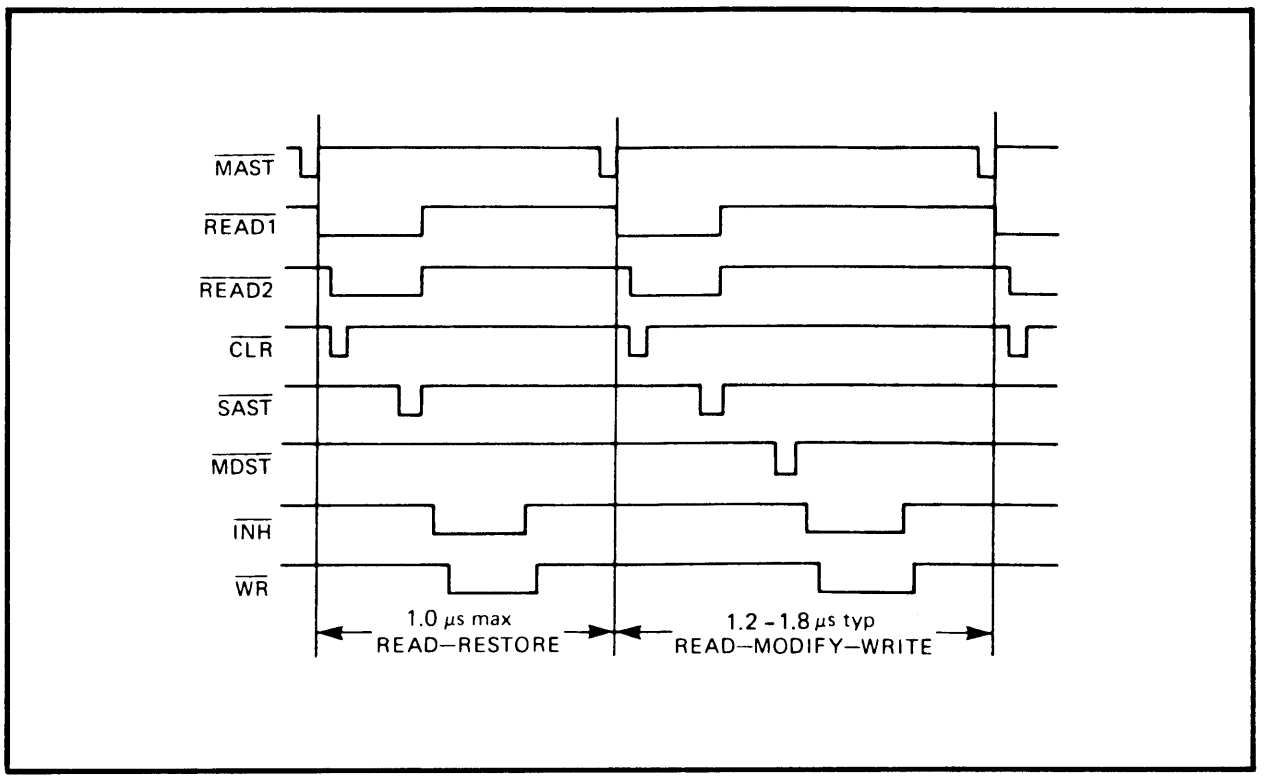


Figure 4-3. Memory Timing

READ1 and READ2 turn on the Y and X read-current generators, respectively. READ1 begins 50 ns before READ2 to minimize the effect of noise perturbations (from half-selected cores) on the desired outputs. All bits in the data register are cleared by the CLR signal at the start of READ2. Sense amplifiers, connected to the 16 sense-inhibit lines, translate the low-level core outputs of TTL-compatible signals. STRA and STRB, which are generated in the memory to coincide with the peak core outputs, gate the sense-amplifier outputs to the preset inputs of the data register. Cores switched from the one state set their corresponding bits in the data register to 1's; those that were already in the zero state produce outputs below the sense-amplifier threshold and consequently do not alter the states of the associated data register bits. MSEL places the contents of the data register on the Read Data (RD) bus at the end of the read operation.

Following the read half-cycle, and after the CPU has performed whatever operations are required on the word retrieved, the modified data are placed on the AWD bus and loaded into the data register by MDST. INH turns on the Y write-current generator and activates those inhibit drivers whose controlling bits in the data register are 0's. WR turns on the X write-current generator 50 ns later.

4.18 Circuit Description

Figure 4-4 is a detailed block diagram illustrating the partitioning of the memory into three circuit modules, the interconnection of these modules, and the interface with the memory bus.

4.19 Address Board. This board stores the memory address (AWD0–15) and generates read and write currents in the module determined by the contents of bits 0 and 1 of the memory address. These currents are routed through the selected X and Y lines (determined by bits 2–8 and 9–15 of the address, respectively) to the core module. All of the control signals for the inhibit board and the core module are routed through the address board; these signals are gated by the MOSL (Module Select) signal, produced by decoding bits 0 and 1 of the address.

The stack is strung to use an 8K sense. Each 16K-bit plane is divided into dual 8K sections. Thus, only half the winding need be driven by the inhibit current, and the sense amplifier is connected across only half the winding. This improves the rise time of the inhibit current and improves the signal-to-noise ratio during the read portion of the cycle. A separate inhibit driver and sense amplifier is required for each half of the 16K-bit plane. Bits 9, 10, and 11 of the address are decoded to specify which half of each plane is selected. The output of this decoder routes the sense amplifier strobe signal to the proper sense amplifier and the inhibit drive pulse signal to the proper drivers.

A Dynamic Bias (DB) level that is high during read and low during write is also generated on this board. It is used to bias the decoding diodes on the stack.

4.20 ***Address Register.*** Four-bit latches, which store the memory address, are loaded by $\overline{\text{MAST}}$. When $\overline{\text{MAST}}$ goes low, the address data on the AWD lines are transferred to the outputs of the latches. When $\overline{\text{MAST}}$ goes high, the information present is trapped and the outputs no longer follow the inputs.

4.21 ***Decoders.*** Three-line to 8-line decoders are used to select the source and sink switches indicated by bits 2–15 of the address. Bits 0 to 1 are connected to two-input Exclusive-OR gates; other inputs are connected in the memory motherboard so that the memory module address is determined by the physical location of the memory. The outputs of these Exclusive-OR gates are connected to a three-input AND gate along with the $\overline{\text{SC}}$ signal to generate the Module Select (MOSL) signal. This signal is gated with CLR to generate the $\overline{\text{CDR}}$ signal to clear the data register; with MSEL to generate $\overline{\text{SRD}}$, which places data stored in the data register on the RD bus; with $\overline{\text{INH}}$ to generate the $\overline{\text{IDA}}$ and $\overline{\text{IDB}}$ pulses that turn on inhibit drivers; with SAST to generate to $\overline{\text{STRA}}$ and $\overline{\text{STRB}}$ pulses to strobe the sense amplifiers during the read half-cycle; with MDST to generate $\overline{\text{LWD}}$, which loads the data register from the AWD lines; and with READ1, READ2, INH and WRITE to turn on the X and Y current sources.

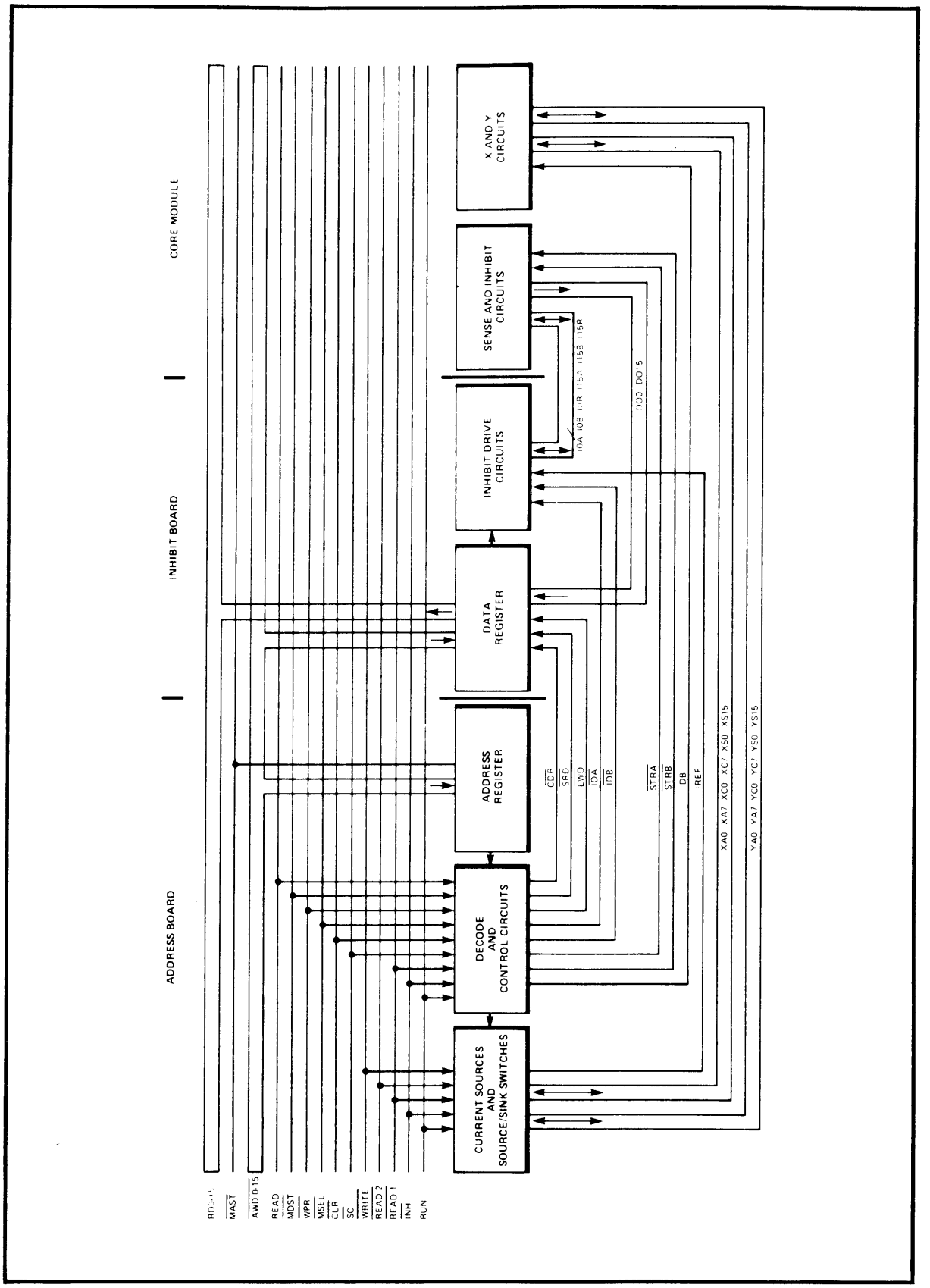


Figure 4-4. Interconnection Diagram, 16K Core Memory Module

Exclusive-OR gates are used to determine, by looking at address bits 9, 10, 11, which half of the sense/inhibit winding is to be driven. When the B side is selected, the $\overline{IDB}$ and $\overline{STRB}$ pulses are generated at the appropriate times. When the A side is selected, $\overline{STRA}$ and $\overline{IDA}$ are generated.

4.22 ***Source and Sink Switches.*** During the read half-cycle, the X-read current is routed to the memory via one of eight lines (XA0–XA7) determined by address bits 2–4, and it returns on one of 16 lines (XS0–XS15) determined by bits 5–8. Similarly, the Y-read current path is selected by bits 9–15. The subsequent write current pulses are sent through the stack in the opposite direction. The X-write goes out on the same line (XS0–XS7) used for the read current. Since each read current may be sent out on one of 8 lines and returned by one of 16 lines, it follows that 128 possible paths through the stack may be selected for each of the X and Y currents.

During the read half-cycle, all of the source collector (SC) inputs are tied together and connected to the read current generator to give eight possible current paths to the stack (YA0–YA7). The negative-true strobe inputs (S1, Figure 4-5) are tied together and pulled down when the read current generator is turned on by $\overline{READ \bullet MOSL}$. The low output from the decoder determines which line carries the current. During the same interval, S2 inputs are tied together and pulled down, enabling the sink switches. Address decoders select one of the 16 switches to carry the return current from the stack.

During the write half-cycle, $\overline{INH \bullet MOSL}$ pulls down the S1 and S2 inputs. The write current pulse is routed through the selected YS line and returns via the selected YC line.

4.23 ***Read and Write Current Generators.*** All four of the read and write current generators on the X- and Y-boards use the same circuit, which is shown in Figure 4-6. When the open-collector gate is off, the base of Q2 is at a potential of V+ and Q1, Q2, and Q3 are off. When the open-collector gate is turned on, the load current will rise to a value nearly equal to Vref/Re. A qualitative description of the turn-on transient follows:

1. Q2 and Q3 begin to conduct, but the stack load, being inductive, limits the rate of change of load current.

2. The collector potential of Q2 rises, but diodes CR1 and CR2 clamp it just short of saturation. The load current rises approximately as

$$\frac{dI_L}{dT} \approx \frac{V+ \ -2Vbe}{L_S}$$

where L_S is the inductance of the stack winding.

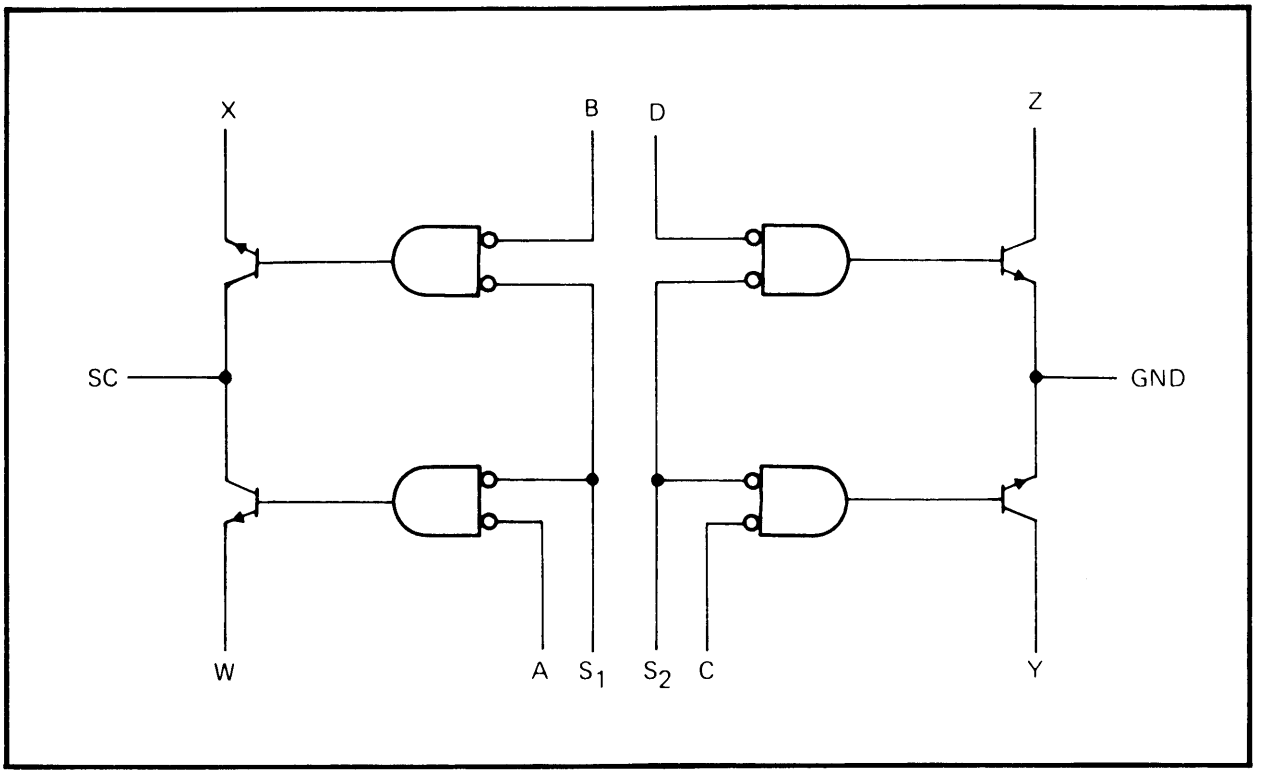


Figure 4-5. Dual Source-Sink Switch

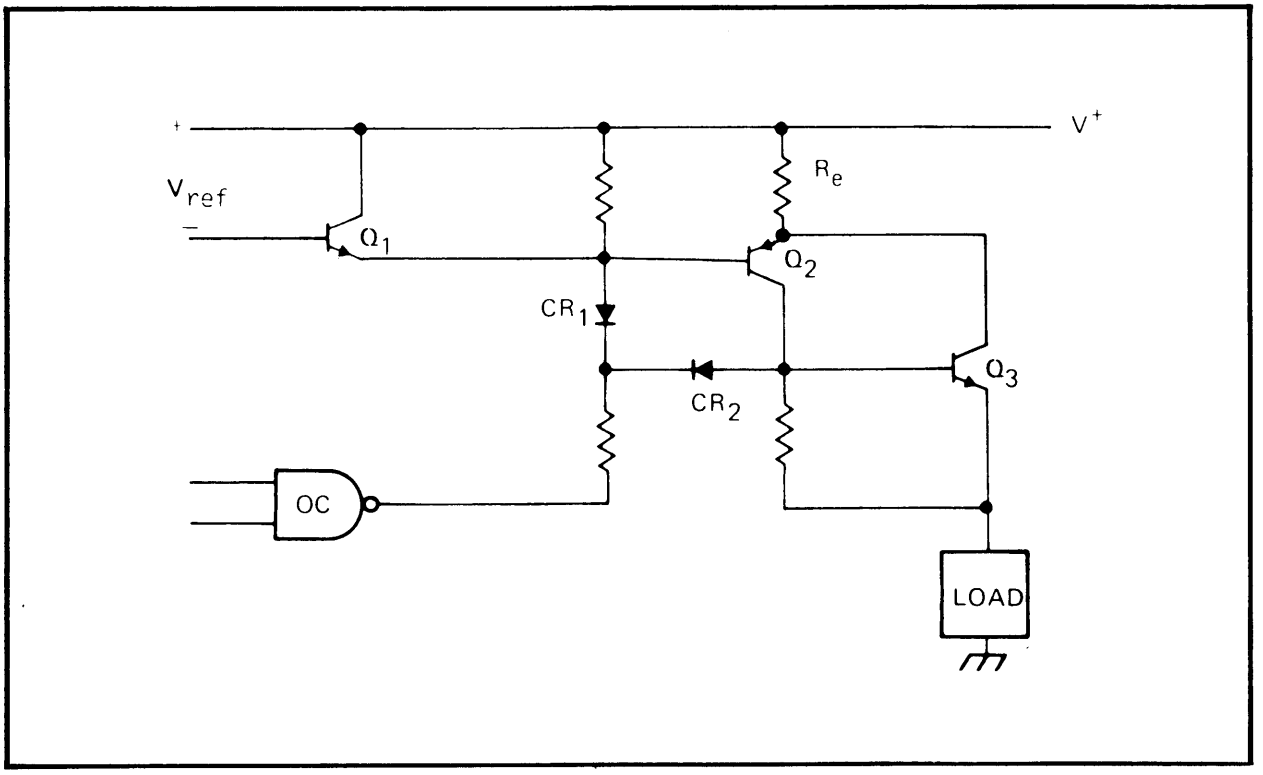


Figure 4-6. Current Generator Circuit

3. This increasing ramp of current causes a decreasing ramp of base potential for Q2 (and emitter potential for Q1).

4. When the base potential of Q2 reaches a value of: Vb2 = V+ − Vref − Vbe, Q1 turns on, clamping it at that value.

5. The current through R3, and consequently the load, is thus clamped at a value

$$I_L = \frac{Vref}{Re}$$

and the load voltage drops to a level just sufficient to sustain this current.

Snubber circuits consisting of zener diodes and series resistors are connected from the current source outputs to ground to limit overshoot on the rise of the currents. When the currents reach steady state, the voltage across the stack is less than the zener voltage and the resistors are effectively disconnected.

A voltage regulator provides a precisely controlled collector current that develops Vref with respect to the +12V supply. In addition, this potential is compensated at the rate of −2.5V/°C, which alters the read and write currents at a rate of −0.5mA/°C. A second temperature-compensated reference current is developed across a resistor on the inhibit board to control the amplitudes of the inhibit currents.

4.24 ***Sense-Amplifier Strobe Generator.*** A dual monostable multivibrator generates the SAST signal, which is used to generate $\overline{\text{STRA}}$ or $\overline{\text{STRB}}$, depending on the address. The first section provides a delay from the leading edge of $\overline{\text{READ1} \bullet \text{MOSL}}$ to the peak of the core outputs, at which time it triggers the second section to generate an 80 ns pulse.

4.25 ***Bias Generator.*** Diodes are used in the X- and Y-sections of the stack to provide 128 independent bidirectional paths through the stack in each section. A dynamic bias (DB) signal is used to switch the diodes. The bias generator pulls the DB line up during read and down during write. The transitions occur at the ends of READ1 and INH. When the CPU is halted, as indicated by RUN being low, the DB line is pulled down.

4.26 **Inhibit Board.** Sixteen identical groups of circuits with separate data inputs and common controls make up this board. Those circuits associated with data bit 0 are shown in Figure 4-7.

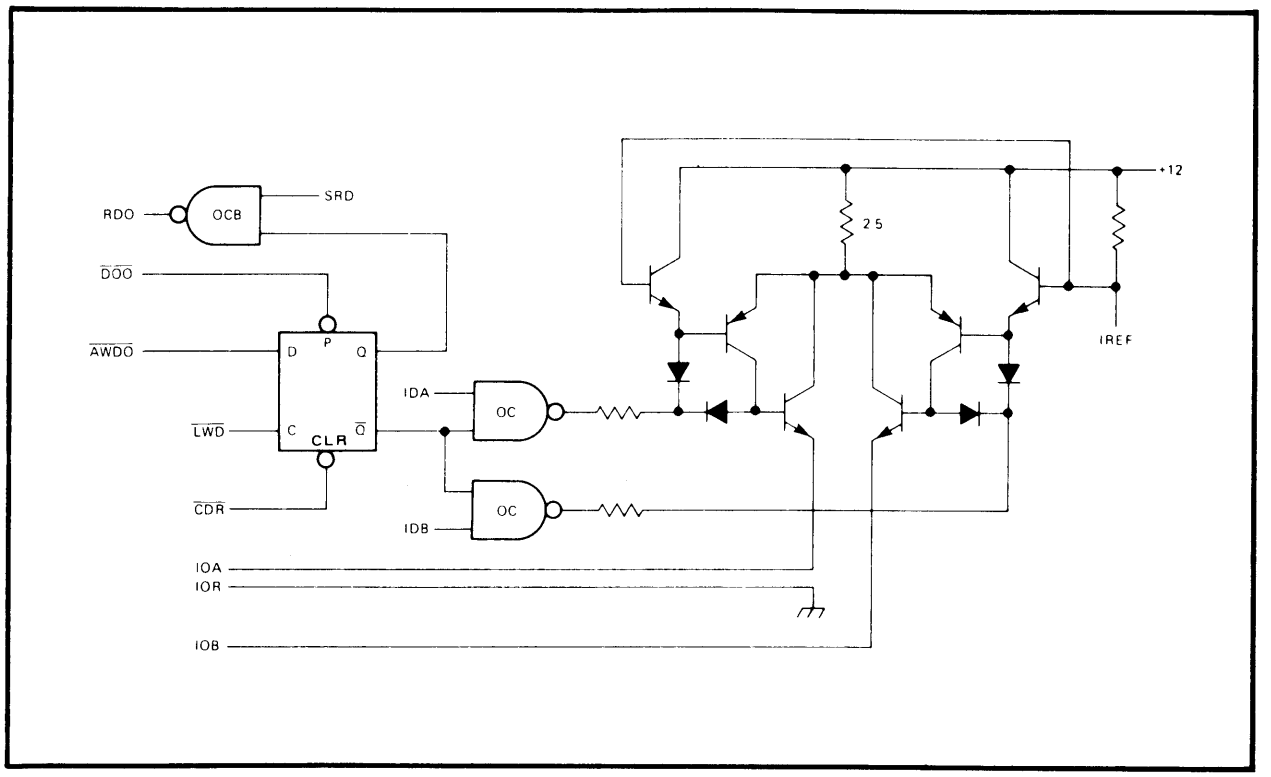


Figure 4-7. Data-Inhibit Circuits, Bit 0

The relationships between memory and CPU data signals are as follows. Data inputs from the CPU are negative-true; i.e., a low level on the AWD0 line is a CPU 1. Outputs from the data register to the CPU are positive-true. A high level on AWD0 (a CPU 0), when clocked into the flip-flop, causes the Q output to go high. When SRD goes high, the RD0 line goes low, placing a low (CPU 0) level on the read data bus to the CPU. Finally, CPU 1's are stored as 0's in the core memory to minimize memory power, since the average instruction contains a majority of CPU 0's. A CPU 0 in the data register causes the Q output to go low. This leaves the associated inhibit driver off during the write cycle, and a 1 is written into core. A subsequent read operation produces a high output on the DO0 line, a low input to the present input at SAST time, and a high level at the Q output. In the following discussion, a 1 means a memory 1 unless specifically denoted as a CPU 1.

4.27 ***Data Register.*** Data-inhibit circuit functions are related to the time sequence of events in a Read-Modify-Write cycle. These functions and events are related as follows:

1. $\overline{\text{MAST}}$ loads the address register. MOSL is generated on the address board and gates the control signals to the inhibit board.
2. Read currents are turned on. All data register bits are cleared (set to the zero state) by the $\overline{\text{CDR}}$ pulse immediately following the start of $\overline{\text{READ2}}$ and prior to receiving outputs from the stack.

3. Those cores switched from the one state produce sense-amplifier outputs (DOX), which (when gated by SAST) set their associated data register bits to the one state (Q high).
4. SRD places the word retrieved from memory on the read data bus.
5. Modified data from the CPU are placed on the $\overline{\text{AWD}}$ bus and loaded into the register at the trailing edge of $\overline{\text{LWD}}$.
6. Write currents are turned on. IDA or IDB turns on those inhibit drivers with 0's stored in their associated data register bits.

4.28 ***Inhibit Drivers.*** Dual current sources are used to inhibit lines. IDA or IDB turns on one side or the other, sending a current out the IXA or IXB line. A common return line is used since only one can be on at a time.

Inspection of **Figure 4-7** shows that these current source configurations are the same as those of the Read and Write current generators, and they operate in the same way. Turn-on transients are controlled by terminations at the stack end rather than with the snubber circuits of the read-write current generators.

4.29 Core Module (Stack). The stack contains sense-inhibit lines, sense amplifiers, X-drive and Y-drive lines, diode decoding, and resistive terminations.

4.30 ***X and Y Circuits.*** Each of 16 XS lines (XS0–XS15) connects directly to 8 drive lines. The other ends of these drive lines are diode-connected to the XA and XC lines.

Line selection and current routing is best illustrated by a specific example. Suppose that XS15 and the XA7/XC7 pair are specified in the X address. During the read half-cycle, the read current pulse is sent down the XA7 line and XS15 is returned to ground by a sink switch. Also, recall that the DB line is pulled up during read. Since XA7 is driven positive (the read and write currents are developed from the + 12V supply) and XS15 is pulled down, the diode connecting XA7 to the desired line is forward biased. All others are back biased. Consider the SC lines. During the read half-cycle, all of the sink switches connected to the XC lines are turned off. Thus, all SC lines are pulled up to 12V by the HSB input. DB is high but at a potential less than 12V. Therefore, all diodes connected to SC lines are back biased. Similarly, the only source switch that is on is the one driving XA7, so all diodes connected to XA0–XA6 are back biased by the DB and LSB lines. Finally, DB is more positive than the driven XA line, so all diodes connected to XA7 are back biased except the one pulled down by XS15. In a similar manner, a write current injected into XS15 flows through the desired line and out through the SC7 line. Y-drive operation is the same.

4.31 ***Sense and Inhibit Circuits.*** One of the sense amplifier and sense-inhibit circuits is shown in Figure 4-8. This circuit is repeated 16 times.

The geometry of the sense-inhibit line is described as follows. SOA and $\overline{SOA}$ are the ends of the line, and IOA is connected to the center tap. The cores strung between SOA and IOA are threaded in such a fashion as to give a certain output polarity, say positive. The cores on the other half, which are strung between $\overline{SOA}$ and IOA, given a negative output. This is done to cause cancellation of the low-level responses from half-selected cores during a read operation.

The following occurs during the read half-cycle. IOA is open and IOR is at ground potential. SOA and $\overline{SOA}$ are connected to the inputs of a bipolar comparator. Whenever the magnitude of the potential difference between SOA and $\overline{SOA}$ exceeds the reference voltage (14mV), DO0 goes to a logical 0 level. Thus, the selected core gives the desired signal out regardless of thich polarity it induces in the sense line. Note that any perturbations on the IOA or IOR lines are common-mode inputs and should have little effect on the desired response. The DO0 output is gated by STRA so the only outputs of significance are those that occur at the expected core peaking time.

The sense amplifier plays no part in the write operation since its output is ignored and its input impedance is high. Should bit 0 be programmed to store a 0, an inhibit current equal to Isw is injected at IOA, which splits to send Isw/2 through each half of the sense winding. These currents are summed by the diodes at the IOR node and returned to the inhibit driver.

4.32 CONTROL PANEL

The control panel is the operator interface to the 1602B Processor. It provides for manual control and data entry to the processor, and contains displays for status information and data from the processor. Note that the control panel is used only for troubleshooting and maintenance, and is not part of the operational computer system.

The operational functions of the control panel are discussed in Section III. Physically, the control panel contains four electronic subassemblies: The power supply;the switch board, which contains the 16 SPST data switches and 10 SPDT momentary control switches; the display board contains the 11 discrete LED (light-emitting diode) status indicators and the two 6-digit octal LED displays and decoding; the Logic board contains line drivers and receivers, control switch encoding logic, and breakpoint logic.

Refer to schematic 00-107280 for this discussion of the Model 1638 Control Panel.

4.33 Interface Signals

The interface to the Model 1602B Processor consists of 28 signals. A single bidirectional 16-bit data bus (PB) is the basic data path between the processor and the control panel. The bidirectional PB bus is buffered by drivers and receivers on 64K.

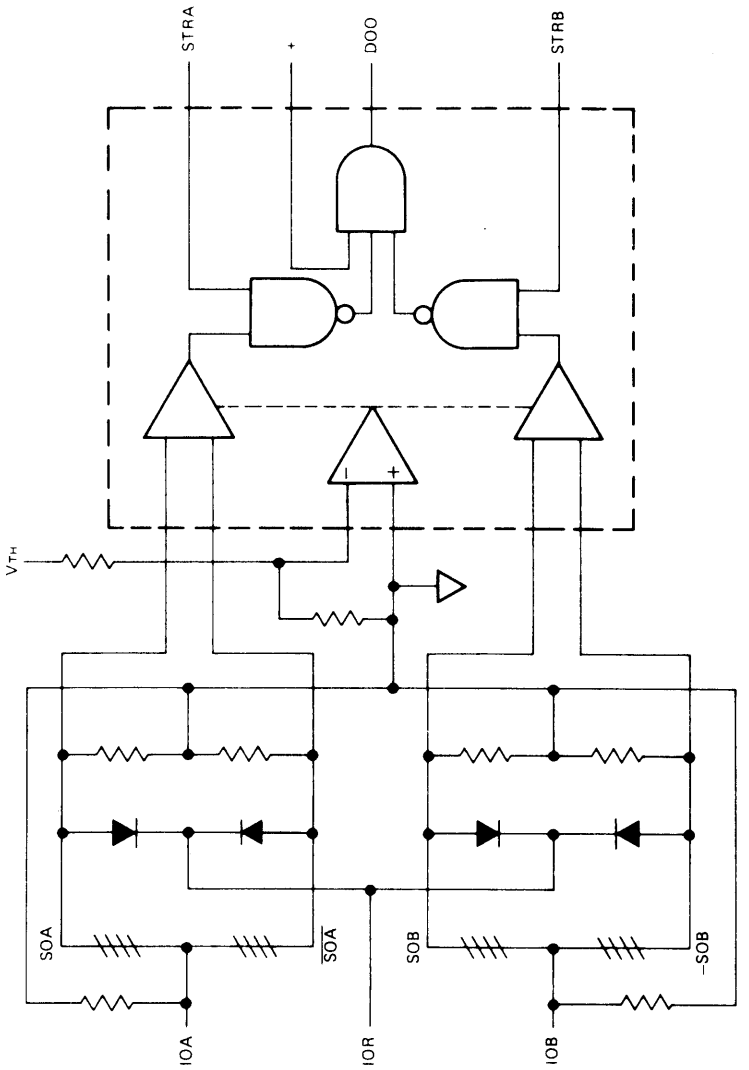
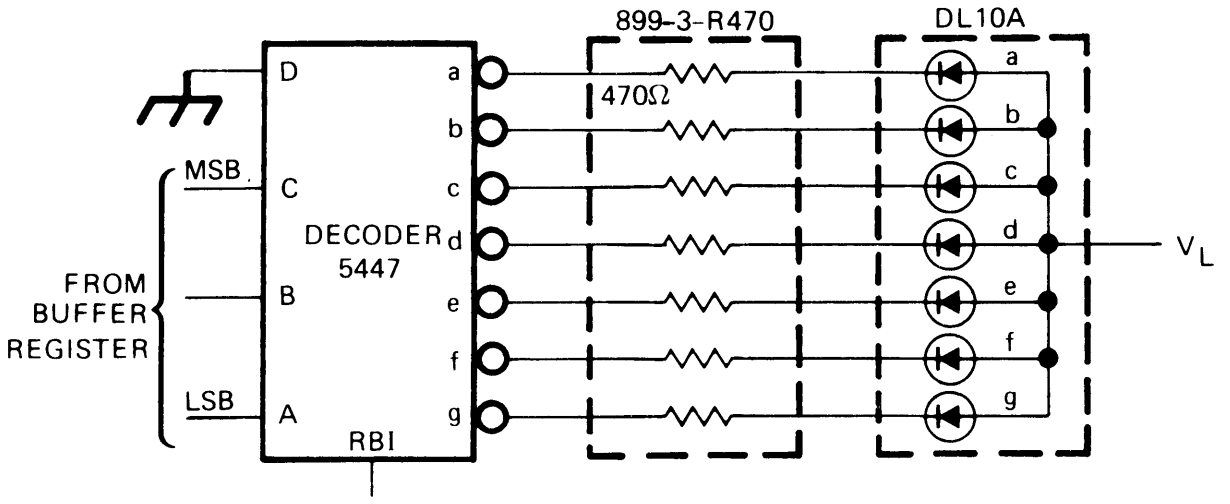


Figure 4-8. Sense Amplifier Circuit

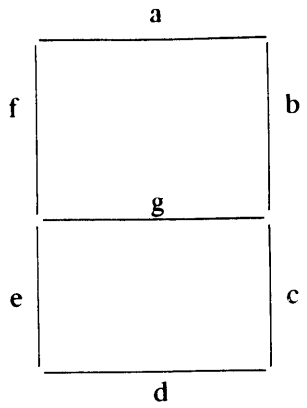
In addition to the data busses, there are 12 control and status signals in the interface. $\overline{\text{PINT}}$ (Panel Interrupt), PDMA (Panel DMA), PANF (Panel Fetch), and PRUN are status signals from the CPU which directly drive the PI, DCH, FETCH (and EXECUTE), and RUN indicators, respectively. $\overline{\text{PSEL0}}$ (Panel Select 0) and $\overline{\text{PSEL1}}$ (Panel Select 1) are control signals generated by the CPU which gate the data switches or encoded control switches, respectively, onto the PIB lines. $\overline{\text{PMAST}}$ (Panel Memory Address Strobe) and PDST (Panel Data Strobe) are strobes generated by the CPU which cause the Address display (conditionally) or Data display buffer register, respectively, to be loaded with the data present on the PB lines. PCLR (Panel Clear) is a pulse generated by the CPU which causes the Data display to be blanked. $\overline{\text{PRQ}}$ (Panel Request) is a pulse generated by the control panel whenever the processor is stopped and a control switch other than START or RESET is pressed. $\overline{\text{PSTOP}}$ and $\overline{\text{PRST}}$ are generated by pressing the STOP or RESET switch (unless the on-off switch is in LOCK position) and cause the CPU to halt at the end of the current instruction or memory cycle, respectively.

4.34 Address Display

The six-digit octal address display is comprised of six seven-segment LED display units, together with a buffer register and decoding logic. Shown below is the circuit for each octal character on the display board.



The decoder (5447) pulls down appropriate open-collector outputs a–g to turn on the LED segments corresponding to the octal character present at inputs C, B, A of the decoder. If C, B, A are all logical zeros (low) and RBI is low, decoder outputs a–g are all high, and the display is blank (blanking is used only on the data display).



The buffer register for the address display consists of two 9308 latches (logic U2, U4) which load from the inverted $\overline{PB}$ lines whenever the PMAST pulse occurs, depending on the address display mode flip-flop U5–6.

4.35 Data Display

The 6-digit octal data display uses exactly the same display circuits as described in Paragraph 4.44 for the address display. The buffer register for the data display consists of two 9308 latches (logic U1, U3), which load from the inverted PB lines when the PDST pulse occurs. Blanking is controlled by PCLR and an R-S flip-flop (U18-6, 8). PCLR resets the buffer register to all logical zeros and also sets the blanking flip-flop, grounding RBI on the decoders, which blanks the display. The PDST pulse clears the flip-flop, blanking the display.

4.36 Status Display

On the display board are 11 discrete light emitting diodes (DS1–DS11) for display of status information. The driver circuit is an open-collector TTL gate (U11, 43, 46) and current limiting resistor. Five of the diodes (PI, DCH, FETCH, EXECUTE, RUN) continuously display the status conditions within the CPU (FETCH and EXECUTE are derived from the two polarities of PANF). The other six diodes display the state of PB0–PB5 whenever RUN is off (PRUN low, U5-8). In all shut-down sequences the microprocessor gates the status word onto the PB lines before halting, so that ION, OVF, etc., are correctly displayed.

4.37 Data Switches

The 16 SPST data switches (S1–S16) are gated onto the PIB lines through open-collector NAND gates U31, 32, 33, 34 when $\overline{PSEL0}$ is low. The data is active-high on the PIB lines, with a logical one generated by a switch closure to ground.

4.38 Control Switches

The 10 control switches S17–S16 actually generate 20 control signals, since each switch is a double-throw momentary action with center off. All switch closures except STOP/RESET are encoded by U16, 21, 25, 26 to an 8-bit control code, which is placed on PIB0–PIB7 through open collector gates U22, 24 when $\overline{\text{PSEL1}}$ is low. One pole of the ON-OFF-LOCK switch on the panel is also encoded for the autorestart condition. U21, 25, 26 are type 9318 priority encoders, which accept active-low data from eight inputs, 0–7, and provide a binary representation of the highest priority input on the three active-low outputs, A2–A0. Input 7 has the highest priority. Output $\overline{\text{GS}}$ is low if any input is low; $\overline{\text{E0}}$ is low when all inputs are high. If E1 is high, all outputs, including GS and $\overline{\text{E0}}$, are high. Refer to Table 4-1 for switch encodings.

Table 4-1. Truth Tables (J) Panel Control Switches

Control Switch	Request Line	Contents of RD Bus during Switch Interrogation						I/O Data Bus Bit				
								2	8	9	3	4
EXAM	PRQ	0	7	4	3	7	7	1	1	0	0	0
DEP	PRQ	0	7	4	7	7	7	1	1	0	1	0
EXAM NEXT	PRQ	0	7	5	3	7	7	1	1	0	0	1
DEP NEXT	PRQ	0	7	5	7	7	7	1	1	0	1	1
START	PRQ	0	7	6	3	7	7	1	1	1	0	0
PANEL INST	PRQ	0	7	6	7	7	7	1	1	1	1	0
BREAKPOINT	PRQ	0	7	7	3	7	7					
(SPARE CODE)	—	(0	7	7	7	7	7)					
EXAM AC0	PRQ	1	0	0	3	7	7	1	0	1	0	0
EXAM AC1	PRQ	1	2	4	3	7	7	1	0	1	0	1
EXAM AC2	PRQ	1	5	0	3	7	7	1	0	1	1	0
EXAM AC3	PRQ	1	7	4	3	7	7	1	0	1	1	1
DEP AC0	PRQ	1	0	0	7	7	7	1	0	0	0	0
DEP AC1	PRQ	1	2	4	7	7	7	1	0	0	0	1
DEP AC2	PRQ	1	5	0	7	7	7	1	0	0	1	0
DEP AC3	PRQ	1	7	4	7	7	7	1	0	0	1	1
MEM STEP	PRQ	1	7	5	3	7	7					
INST STEP	PRQ	1	7	5	7	7	7	1	1	1	1	1
CONT	PRQ	1	7	6	3	7	7	1	1	1	0	1
(SPARE CODE)	—	(1	7	6	7	7	7)					
NONE OF ABOVE:												
PANEL UNLOCKED	—	1	7	7	3	7	7					
PANEL LOCKED	—	1	7	7	7	7	7	0	X	X	X	X
STOP	PSTP				—							
RESET	PRST				—							

When PRUN is low (processor is stopped) and no control switch is depressed, U21-15 is low. Depressing any control switch (other than STOP/RESET) causes U21-15 to go high, triggering one-shot U7-9, 44 ms (for debouncing). When the one-shot times out, U7-9 going high triggers one-shot U7-6 (350 ns), which directly generates the PRQ pulse to initiate a control panel function sequence in the CPU.

As long as the on-off switch is not in the LOCK position, pressing STOP or RESET grounds $\overline{\text{PSTOP}}$ or $\overline{\text{PRST}}$, respectively, to halt the processor.

4.39 Break Point Logic

When the PRQ pulse occurs, flip-flop U19-9 is cleared (U19-8 high) if the BREAKPOINT switch is being depressed. This provides an enable input to U13-11, permitting breakpoint halts. Comparison logic U8, 9, 10, 11, 15, 17, 18, 20 provides a low output at U18-3 any time the contents of the Address buffer register (U2, U4) matches logically with the pattern in the panel data switches. Each time the PMAST pulse occurs, one-shot U6 triggers, allowing 125 ns for the buffer register and comparison logic to settle. If a match is present, then U6-7 going high clocks U19, causing U19-6 to be high, pulling down PSTOP (U13-11) if enabled. The processor will then halt after completing the current instruction. When the processor is halted, PRUN being low asynchronously presets U19, clearing the breakpoint match condition.

4.40 Power Supply

The Model 1638 Control Panel operates from 28 Vdc. The power supply is chopper-regulated to provide a single 5 Vdc output, which powers the LED displays and the digital logic (reference schematic 00-107280). An SG3524 pulse-width modulator (U1) drives a push-pull chopper consisting of Q1, Q2, and transformer T1. The output of T1 is rectified and filtered by CR10, L1, and C2 to provide 5 Vdc, which is sensed by an error amplifier consisting of VR1 and its associated passive components. Optical isolator U2 couples the error signal to the pulse-width modulator, which then varies the duty factor of the drive signals to T1 to effect a constant 5 Vdc output as the primary power input (28 Vdc) varies.

4.41 CPU THEORY OF OPERATION

Figure 4-9, central processor block diagram, divides the CPU physically and functionally into two major blocks, the data loop and the control loop. The data loop is located on the "A" board (front). The control loop is located on the "B" board (rear).

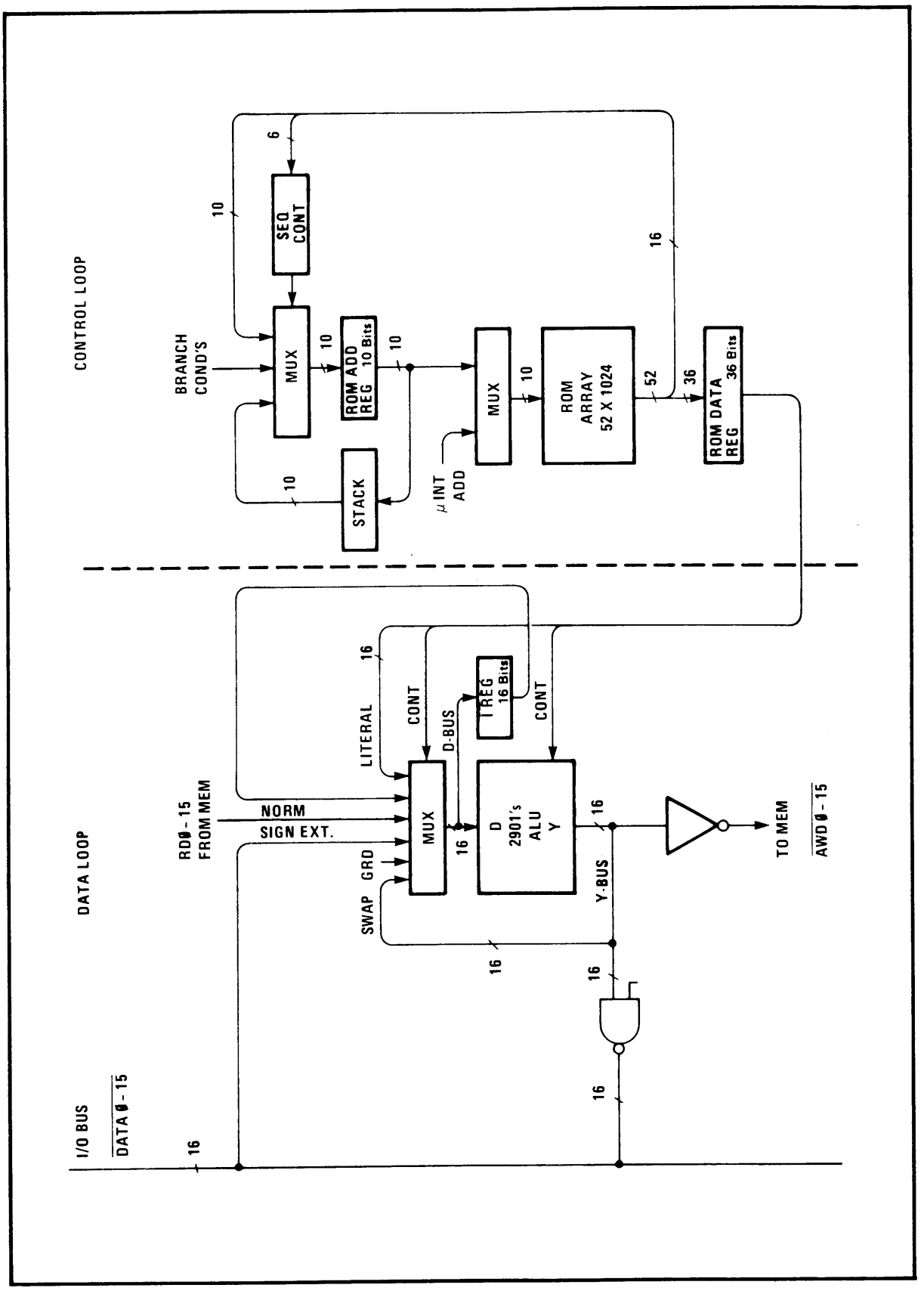


Figure 4-9. Block Diagram of 5605 CPU

4.42 Data Loop

The heart of the data loop is the 2901, which is a 4-bit bipolar microprocessor. Four 2901's are cascaded together to form a 16-bit register-arithmetic and logic unit. A D bus and a Y bus interface with the 2901's for input and output, respectively. The Y bus (output) drives the I/O bus ($\overline{\text{DATA0-15}}$) and the Address and Write Data to Memory Bus ($\overline{\text{AWD0-15}}$). The D bus (input) is multiplexed from several sources: the I/O bus ($\overline{\text{DATA0-15}}$), data from memory bus (RD0-15), a 16-bit literal from the control loop, the 8 least significant bits of the Instruction Register (I REG) signs extended to 16 bits, and the Y bus with the most significant and least significant bytes exchanged.

The only significant system register that is not contained in the 2901's, but is implemented externally, is the Instruction Register (I REG). All other system registers, including all those accessible by software (AC0-3, program counter, and stack pointer), are in the 2901's.

4.43 Control Loop

The control loop provides the control signals for the data loop. The architecture of the control loop is basically that of a pipe-lined microcontroller. While a microstep is being executed out of the ROM DATA REG, the next microstep is being fetched from the ROM ARRAY. Thus, the microstep execution time and the ROM access time are overlapped rather than sequenced, reducing the cycle time of the microstep.

The microcontrol word is 52 bits in width. Of these, 36 bits control the operations to be performed during the microstep, and the remaining 16 are used for sequence control; i.e., to generate the address of the next microcontrol word. The maximum size of the control store is 1024 words. This requires a 10-bit address which is generated by a MUX. This multiplexer has two inputs, the ROM ADD REG and a hardwired microinterrupt address (μINT ADD). Thus, the normal sequencing of microsteps can be interrupted and a routine executed that begins at the hardwired address. When a microinterrupt occurs, the address of the next microstep that would have been accessed is in the ROM ADD REG and it is pushed onto the STACK. The STACK is a four-level pushdown stack. To return from a microinterrupt, the address is popped off the stack (through a multiplexer) and back into the ROM ADD REG. The STACK also permits microsubroutines to the executed. The calling sequence for a microsubroutine pushes the address that is in the ROM ADD REG onto the stack at the same time that it is gated through the MUX to address the ROM ARRAY. When returning from the subroutine, the address is popped from the STACK and the least significant bits are modified while passing through the MUX to the ROM ADD REG.

In addition to sequencing functions previously mentioned, there are available various kinds of multiway branching based on the contents of the I REG, various status conditions, and status registers in the CPU.

SECTION V
MAINTENANCE

5.1 INTRODUCTION

This section discusses maintenance procedures for the processor, core memory, power supply, and control panel. Maintenance discussions for system options or I/O are included in the appropriate sections of Appendices B and C.

CAUTION

Never remove or replace electronic assemblies or cables with power on.

5.2 GENERAL MAINTENANCE CONCEPTS

The Model 1602B Processor is a sophisticated and complex piece of electronic equipment. Isolation of failures to the circuit component level generally requires thoroughly trained technical personnel; however, the modular construction of the processor allows straightforward isolation of failures and easy replacement at the module level.

There are three basic approaches to maintenance planning, the optimum approach depending on the specific requirements of each application.

1. *Chassis Replacement.* In the event of a failure an entire chassis is replaced with a spare unit. This method minimizes mean time to repair, which can be a matter of seconds. The failed chassis is returned to a depot or the factory for repair. This approach is especially attractive for installations with several identical processors or installations with spare chassis.

2. *Module Replacement.* In the event of a failure, the fault is isolated to a replaceable module, and a spare module is installed. Mean time to repair with this method is less than one hour, and this approach is economically preferable to "1" in those installations with several chassis of differing configurations. The failed module is returned to a depot or the factory for repair.

3. *Component Replacement.* In the event of a failure, the fault is isolated to the failed component, which is then replaced. This approach should not be attempted except at

the depot level, since it requires considerable technical skill, sparing or a large number of component types, and can require hours of troubleshooting and repair time.

ROLM maintains an extensive spare parts inventory and a highly trained repair staff. Processors, chassis, or modules returned for repair can be turned around in a matter of days. When returning equipment for factory repair, following the steps listed below will speed repairs and minimize downtime.

1. Contact the Customer Service Department at the factory prior to shipping equipment and obtain a Return Authorization number. This will greatly enhance turnaround time.

2. Ship with the equipment a report on failure conditions and symptoms, e.g., operating temperature, failing programs, intermittent or solid. Also include the Return Authorization number and the name and telephone number of technical personnel to contact.

3. Include an authorization to repair or replace and an accurate packing list to ensure return of all parts.

4. Include a purchase order (P.O.) number. This P.O. number will be used for control purposes if the equipment is under warranty and for invoicing if the equipment is out of warranty.

5. When returning equipment, include any associated equipment which could be affecting the failure mode (control panel, peripherals, etc.) as advised by the ROLM Customer Service Department.

5.3 INSPECTIONS AND PREVENTIVE MAINTENANCE

The Model 1602B Processor is designed to require a minimum amount of periodic inspection/maintenance.

If the processor operates in a vibration environment (such as a moving vehicle), an occasional check of external screw tightness is desirable. In particular, the screws holding the side rails on the PC board conductive heat path should be tightened. Additional information on these screws is contained in Paragraph 5.22. A visual inspection of the system cables and connectors may also be made prior to each deployment.

When the processor has not been operated for some time, it should be checked out with an operational system program before use. This may be done as follows:

1. Turn on processor and check for proper operation of all control panel switches. (Refer to Paragraph 2.12.)

2. Load the CPU Logic Test and run for two minutes.
3. Load and run the other applicable diagnostic routines.
4. Restore operational program.

In general, the checkout schedule should be more responsive to upcoming events than to passage of calendar time. An effective checkout procedure in many cases is to run the operational program with known data, and obtain the correct results before proceeding with the operational usage. This approach in effect runs the most important diagnostic every time the processor is turned on. "Most important diagnostic" denotes the one most closely duplicating the requirements of a particular system.

5.4 FAULT ISOLATION

This section discusses procedures for determining which replaceable module has failed in a system that is not operating properly. Replaceable modules are the power supply, the EMI input filter, each 16K core memory increment (three modules). the CPI, and the CPU. Although the memory has three circuit modules, they are not interchangeable and should be replaced as a unit.

Whenever an apparent malfunction occurs with a processor it is always wise to spend a few minutes eliminating the possibility of operator error (program not properly loaded, peripheral chassis not connected, etc.) or programming bugs in unproved software. If hardware failures seem probable, then there are two basic tools in fault isolation: control panel checks and diagnostic programs.

Control panel checks allow one to manually check a significant portion of the computer hardware. These will generally lead one quickly to diagnose a failure in the power supply, memory, control panel, or the CPU. If the control panel checks work perfectly, then the diagnostic programs should be run. The diagnostic programs are useful in two ways: first, they often simplify identification of the failed module; second, they are a thorough verification of correct hardware operation. It should be noted that since there are only a few easily replaceable units in the processor, the brute force trial-and-error substitution method is viable. When using this approach, first test all power supply voltages and level detectors (+5 OK, MEM OK). If they are incorrect, replace the power supply. If they are correct, then the fault is probably not in the power supply.

5.5 Control Panel Checks

Much of the hardware can easily be checked manually using the control panel. As a first step in fault isolation, perform the procedures given below with the control panel. Gross problems will usually be identified using these procedures; more subtle failures require the use of the diagnostic programs.

Try some manual functions from the control panel. If operation of switches does not cause the display (status, address, data) to change, then the program is probably malfunctioning in one of the following: the +5 Vdc supply, the 20 MHz master oscillator, or the control panel.

Try depositing and examining various data patterns in the accumulators. If the processor hangs up with the RUN indicator on or if the data examined differs from that deposited, the problem is most likely in the CPU.

Try the EXAMINE and DEPOSIT functions. If the memory location appears to always contain all 1's or 0's regardless of what is deposited, the most likely cause is malfunctioning + 12 Vdc or − 5 Vdc regulators in the power supply. If only one or a few bits of the data are wrong or if only certain addresses malfunction, the problem is probably in the 16K memory module (particularly if the other 16K module behaves properly).

Try filling a block of memory with specific data patterns using DEPOSIT NEXT, and examine with EXAMINE NEXT. Put in a two-instruction loop, such as SUB 0,0,JMP. − 1. Check the operation of START, STOP, CONTINUE, and RESET.

If control panel functions cause display changes with RUN off, and it appears the wrong function is being performed (i.e., EXAM NEXT when you pressed DEP), then the problem is most likely in the control panel, CPI, or CPU.

If diagnostics are supplied on paper tape, load the Memory Address Test by doing a bootload with device 77 selected. If the program runs correctly, proceed with other diagnostic programs. If programmed halts occur, verify that the program is loaded correctly. If the program is correct, the memory is most likely faulty. If the control panel display is unchanging but the RUN light is on, check the instructions to see whether bits have been picked up or dropped. If so, the memory is probably faulty. Otherwise there is probably a CPU problem. Instruction stepping through the program may prove helpful.

If diagnostics are supplied on an IDMS media, boot the media. IDMS will perform a memory address test and output an error message if any faulty memory has been detected. If unable to boot IDMS, check the I/O interface by the method described in Paragraph 5.7.

5.6 Diagnostic Programs

The diagnostic programs perform systematic testing of the processor. Besides standard routines for the basic processor, others are available which apply to I/O interfaces and other options; they are noted in the appendix which describes the particular option.

To perform any diagnostic test, the following two items are required:

1. *Binary Program Tape.* This is a punched paper tape containing the diagnostic program. It is loaded into the processor in the same manner as any program tape.

   OR

   Integrated Diagnostic Management System Media. This is a magnetic tape, cartridge disk, or floppy disk, containing the diagnostics for the processor and peripherals. It is booted using the standard bootstrap for the device.

2. *Program Operating Instructions and Listing.* A set of instructions and a program listing are provided for each diagnostic program. The instructions tell how to start the program, define different operation modes (if applicable), and describe the error indications.

If no indications are available which limit the problem, the diagnostics should be run in the following order:

Memory Address Test (if using paper tape)
Instruction Test
Checkerboard Data Test
Stack and Interrupt Test
Random Arithmetic Test
Teletype Test
Exerciser

The diagnostics are written to output an error message if a problem is detected and either halt or continue, based on operator selection. The listing can then be consulted to determine the problem symptom. If the program finds no problem, it either runs continually or runs to a specified number of passes if under IDMS, displaying an iteration count in the control panel data lights. Some problems will cause the program to "blow up," rather than to halt. By this is meant going into a strange instruction loop or "locking up," in which the control panel display is unchanging but the RUN light is on.

The module replacement sequence to follow depends on which diagnostic failed and what the failure symptom was. Due to the large number of possible failures, it is not practical to list them together with each optional replacement sequence. However, since there are basically only a few modules, each of which is easily replaced, there is little variation in total repair time no matter what replacement sequence is followed. Discussed below are some general guidelines which, in most cases, will lead to a short replacement sequence.

Assuming the control panel checks and memory address test operated error-free, a problem encountered with the diagnostics is most likely a marginal memory or a failure in the CPU. If the Checkerboard Data Test runs error-free, the memory is probably operating normally. If halts occur, a faulty memory is almost certainly the problem. Halts in the Teletype Test would indicate a faulty CPU or a failed I/O option.

5.7 Loading Problems

Sometimes it may be impossible to load the diagnostics. Assuming no gross fault has been detected by the control panel checks, the problem should still be easy to find. If the processor stops in the process of loading a paper tape because of a checksum error, back the tape up to the beginning of the block and raise the START switch (not CONT).

NOTE

Never try to restart the processor before backing up the tape.

Check the Binary Loader. A possible problem is that the Binary Loader has been inadvertently altered. If the Binary Loader will not load, try another input device if one is available. If not, key in a simple input routine, such as:

```
0601XX      NIOS      DEV (XX)
0636XX      SKPDN     DEV (XX)
000777      JMP       .-1
0605XX      DIAS      0,DEV (XX)
063077
```

If this routine does not complete (i.e., execute and halt), it is probably best to begin troubleshooting at the I/O interface. If the short routine does complete, check AC0 for the proper data. If no problem in the data is observed, instruction-step through the Bootstrap Loader routine until you detect the problem.

5.8 Power Supply Shutdown

Because overcurrent, overvoltage, and overtemperature sensors protect the supply from externally caused failures, actual supply failure should be rare. However, many problems will at first be diagnosed as power supply failures since the supply reaction to an overstressed condition, whether it be temperature, voltage, or current, is to set a latch which electronically shuts down all outputs. The following subparagraphs outline techniques for separating actual supply failures from apparent supply failures. Should an actual supply failure be diagnosed, it is strongly recommended that the supply, or preferably the whole system, be returned to the factory for repair. Field troubleshooting and repair of supplies should never be attempted except by factory-trained personnel, and then only with extreme caution because of the high voltages involved.

5.9 Overcurrent Shutdown. A current-sensing resistor in series with the emitters of the chopper transistors is used to monitor the total load current. A short on either the +5 or +12 Vdc output (e.g., due to a shorted tantalum capacitor) will cause this current to exceed a preset threshold and cause the chopper to shut down. A short on either the −5 or −12 Vdc output will probably not cause the threshold to be exceeded; however, both of these outputs are current-limited so that a short on either will affect only that output — not the others.

To isolate a circuit module that is overloading one of the outputs, remove the modules one at a time. If the short is on the −5 or −12 Vdc line, the voltage will return to the proper value when the faulty module is removed. If the short is on the +5 or +12 Vdc line, the latch must be reset by turning the power off and back on each time a module is pulled. When the faulty module is pulled, the supply will come on and stay on.

5.10 Overvoltage Shutdown. The shutdown latch will also be set if a transient on the input approaches a level that could damage the supply, or if either the +5 or +12 Vdc output should rise to a level that could damage circuit modules. The latter condition could be caused by a regulator loop failure or instability which would necessitate repair of the power supply. It could also be caused by a wiring or connector problem that would open one of the remote sense connections. If the latch is tripping and no shorts can be found, the sense line for the +5 or +12 Vdc output should be checked for continuity.

5.11 Overtemperature Shutdown. A thermistor inside the supply is used to monitor the internal supply temperature and shut the supply down at about 100°C. If an operator is present when shutdown occurs, the problem will be obvious. The operator need only touch the machine to identify the problem. Should the shutdown occur on an unattended machine, it may cool down before the problem is noticed. Upon restarting a machine that has had an unexplained shutdown, the operator should always check to be sure that the fan is operating and that the air intake port is not blocked.

5.12 Obvious Supply Failures. Since the electronic shutdown circuits protect the system electronics and most of the power supply components, a blown fuse generally means that there has been a hard failure in the input circuitry or in the control section of the supply. It is possible, particularly in heavily loaded systems in high-vibration or high-temperature environments, for a fuse to fatigue and fail spontaneously. Such a failure will generally not discolor the fuse appreciably. If the fuse is replaced and does not blow again, it was probably a random fuse failure. Certain failures, such as the input bridge or one of the chopper transistors, draw such high surge currents that the fuse element will virtually vaporize, and the fuse will be noticeably blackened. When this happens, the supply is almost certainly defective and must be repaired. Repeated replacement and blowing of fuses can only increase the damage to the supply.

A malfunctioning input filter may be isolated by first verifying primary power input, then checking power output at filter connector P2 (see Figure 5-6 and Table 5-4).

5.13 TROUBLESHOOTING AND REPAIR

This section discusses guidelines for troubleshooting and repair of failed modules at the circuit component level. Component level repair should be attempted only by trained personnel who are thoroughly familiar with the theory of operation contained in Section IV and with military specifications and standards for replacement of components.

5.14 Power Supply

The EMI filter and the power input fuses should be checked before troubleshooting the power supply. A blown fuse indicates a probable fault in the EMI filter or in the power supply. If power is present at the output of the EMI filter, proceed with troubleshooting the power supply.

NOTE

Separate connector pins are used for ac and dc power, and power system continuity is maintained only when the power supply and the EMI filter are both ac or both dc, as required.

Since the power supply contains protective circuitry for overvoltage, overcurrent, and overtemperature protection from externally caused failures, actual supply failures should be rare. To determine whether a power supply failure has occurred, refer to Paragraph 5.8.

Should an actual supply failure be diagnosed, it is strongly recommended that the supply or preferably the processor system be returned to the factory. Because of the high voltages used in the supply, field repair should never be attempted except by factory-trained personnel.

5.15 Core Memory

The three circuit modules comprising a core memory are calibrated as a unit at the factory. Although the memory will generally operate at room temperature with interchanged boards, its margins may be poor, and malfunctions at extremes of temperature can be expected.

CAUTION

Use extreme care when handling the core module. It has exposed fine magnet wire which is easily cut. Never remove the core cover. In the event of a core module failure, it is strongly recommended that it be returned to the factory for repair.

The following procedures for troubleshooting of the memory are recommended:

1. Isolate the fault to a given memory module. If this cannot be done, the defect is probably elsewhere — memory controller signals, power supply problems, another device on the RD lines at the wrong time, noise on interface lines, etc.

2. With the control program resident in another module, loop on a failing instruction sequence.

3. Trace the problem to one of the three circuit boards. Place the suspected board on an extender and probe for anomalies. Several facts complicate this procedure. First, if the data inhibit board is removed from the chassis and its stiffener removed, it will overheat unless the inhibit duty factor is very low. Second, the noise environment is much different on an extender and there is no assurance that even a good memory will work with one of the cards on an extender. Finally, since the stack is a current-controller device, voltage waveforms are unusual to say the least and are difficult for the untrained eye to interpret.

The best advice is to make use of the high degree of parallelism in the system by comparing waveforms in like circuits and looking for deviations.

5.16 CPU

CPU repair should not be attempted in the field. Failed CPUs should be returned to the factory for repair.

5.17 Control Panel

Troubleshooting the control panel is very straightforward and can be accomplished with the panel completely disconnected from the processor. The following procedures are recommended.

1. Disconnect the panel from the processor, apply power, and turn switch to ON. If no displays are illuminated, troubleshoot the power supply. First check the fuses.

2. To check data switches, ground PSEL0 and look at PIB lines to see if they follow the switch closure. Note: The PIB lines are driven by open-collector gates. On remote panels they are tied to the PB lines which have resistive terminators. However, on a local panel a pullup resistor should be connected for measurement.

3. To check the control switch coding, ground PSEL1 and look for correct patterns on PIB lines for the various control switches.

4. If the panel could perform no functions when attached to the CPU, ground PRUN, then scope PRQ for a pulse whenever a control switch is pressed.

5. To check the data display, ground PCLR and insert data patterns by grounding appropriate PB lines. Then check blanking by grounding PDST and ungrounding PCLR.

6. To check the address display, ground PMAST and insert data patterns by grounding appropriate PB lines.

7. Check status display LEDs by grounding PRUN and appropriate PB or other lines.

5.18 IC Replacement

IC removal and replacement should be performed only by a technician skilled in working with semiconductor devices. When removing an IC, certain steps make the procedure easier. First, remove the HumiSeal® coating by applying trichloroethane liberally to both sides of the board in the vicinity of the IC to be removed. Next cut all the leads to the IC as far off the board as possible. Then the individual leads may be unsoldered and easily removed from the board. Remove excess solder and clean the area with more trichloroethane. Make sure no traces are shorted to heat frame.

The new IC should have Wakefield Engineering Corporation Thermal Compound applied to its underwide before installing. After inserting the IC, press it very tightly against the thermal frame and solder two or three pins. This will hold it in while the other pins are soldered. Recoat the area with HumiSeal.

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5.19 ACCESS

This section covers physical access to the Model 1602B Processor, memory and control panel. The processor consists of a chassis with numerous slots for plug-in circuit modules. The circuit modules make electrical connection to a motherboard in the bottom of the chassis, which provides electrical interconnections between circuit modules. The power supply and EMI filter are removable assemblies.

Figure 5-1 shows replaceable components and circuit module locations in the chassis. Subassembly locations are designed by A1, A2, etc.

At the replacement module level, access to any assembly in the processor and control panel is achievable by means of three scewdrivers and a special circuit module extractor.

Hex Wrench, 3/32 in.
Screwdriver, No. 1 Phillips Head
Screwdriver, No. 2 Phillips Head
Screwdriver, 1/8 in. blade, 3 in. long
Card Extractor, ROLM Model 5625

5.20 Top Cover

Access to all circuit modules for insertion or removal is achieved by removing the top cover of the chassis. The top cover is attached by 16 captive screws.

5.21 Bottom Cover

Removal of the bottom cover permits access to all motherboard connections. This cover is attached by captive screws.

5.22 Circuit Modules

The plug-in circuit modules can be removed by the following procedure:

1. Remove top cover (Paragraph 5.20).

2. With a 3/32 in. hex wrench, loosen (about two turns) the two screws holding the two vertical clamping wedges. The screws should not be removed from the wedge.

3. Attach the card extractor as shown in Figure 5-2. The handle edges are grooved to fit on the top of the main frame box side plates. Two pins in the extractor fit into small mating holes on the top edge of the circuit module stiffener. The extractor pins should be inserted from the aluminum stiffener side of the module because that side provides greater mechanical strength.

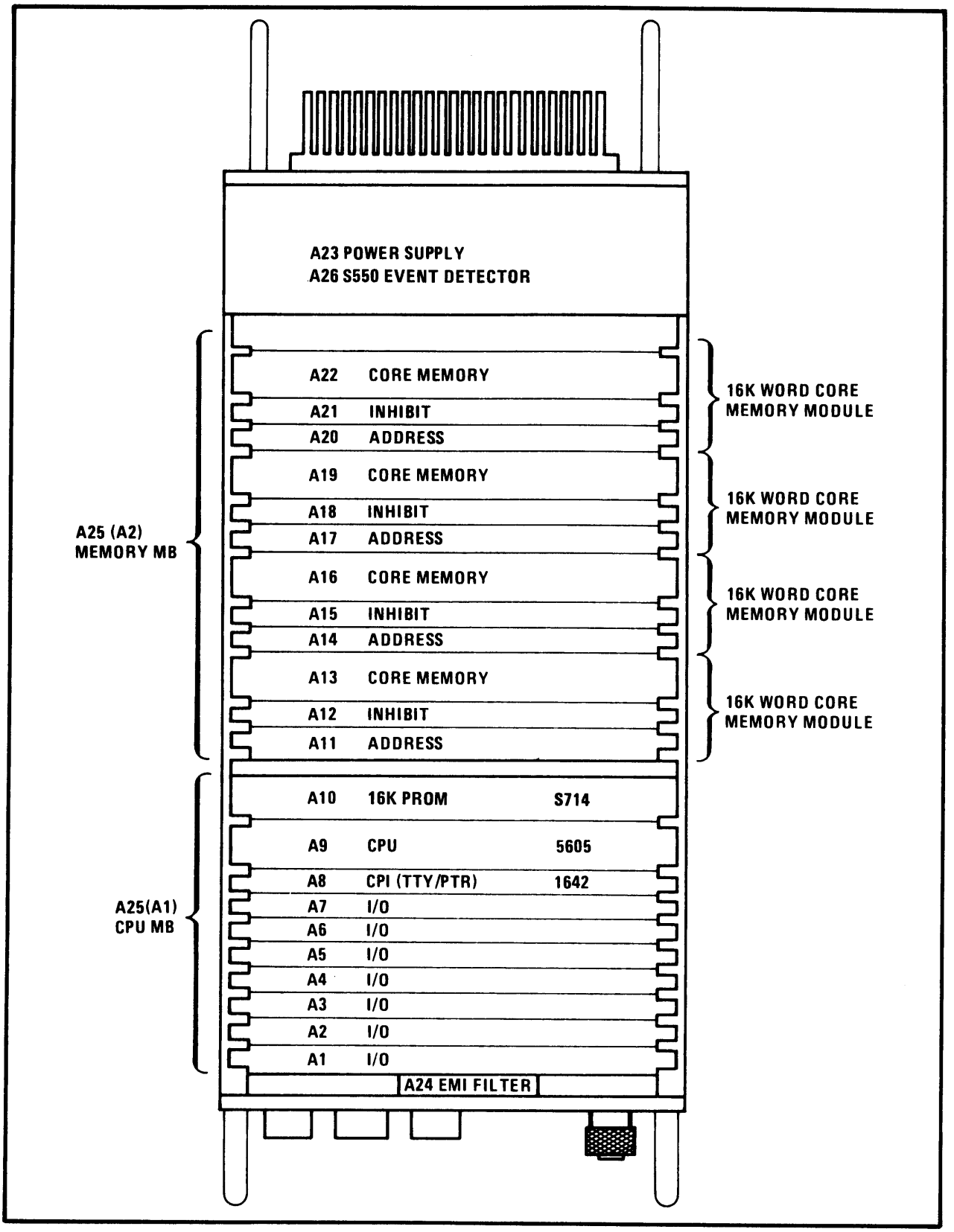

Figure 5-1. Circuit Board Configuration

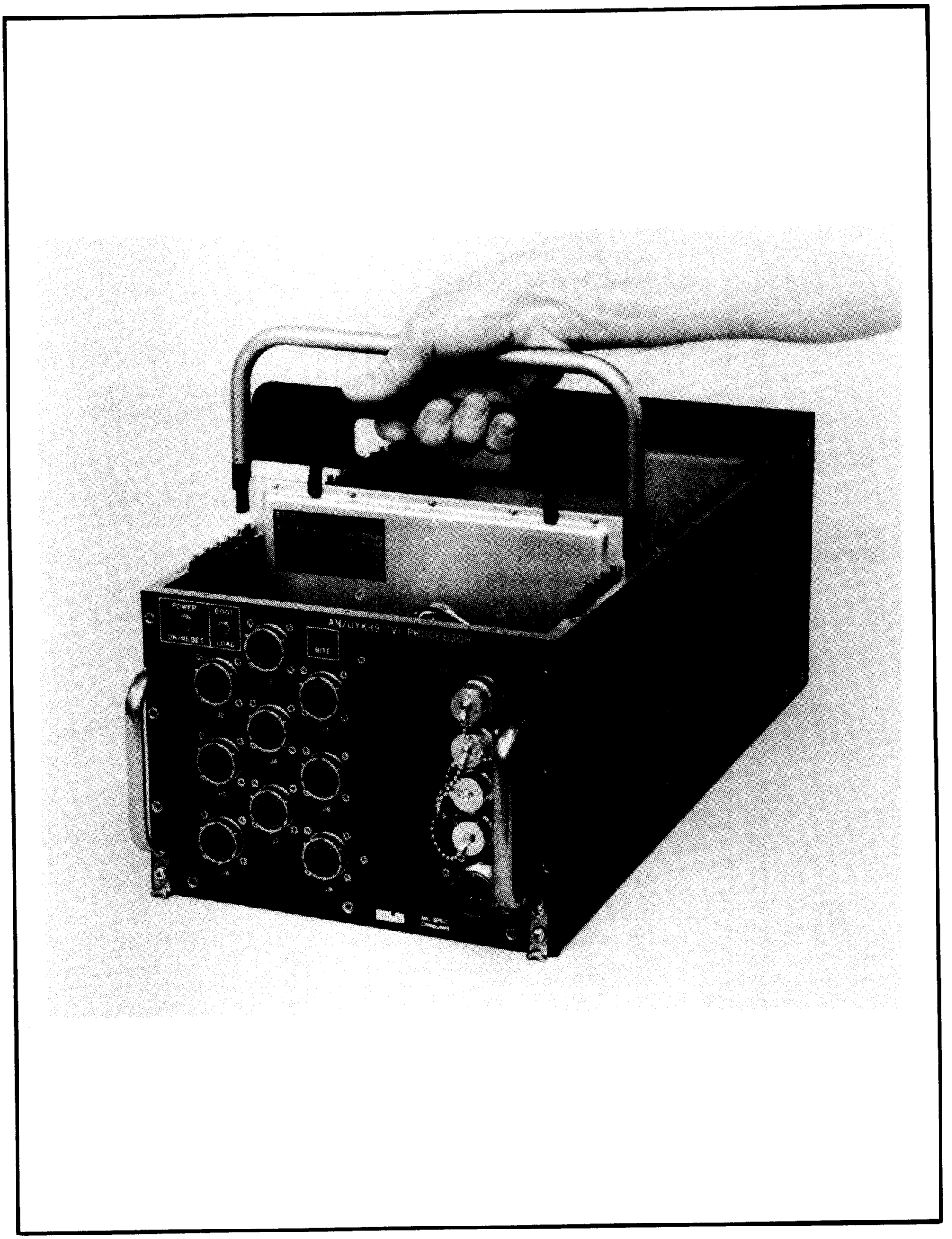

Figure 5-2. Circuit Module Removal

4. By squeezing slowly with the card extractor, the circuit module will be pulled loose from the two connectors on the motherboard.

Replacement of a module is accomplished by manually inserting the board into the proper slot, using the palm of the hand to push the board firmly into place. After the board is in place, both side wedges must be fully tightened. Cooling of the integrated circuits is accomplished by conducting the heat out through the card edge to the processor box side plate, and continuity of the cooling path requires that the wedges be kept tight.

Once the module is removed, access to the components requires removal of the aluminum stiffener. Applicable assembly drawings are included in Section VII.

5.23 Memory

Access to the circuit modules comprising core memory is the same as for other circuit modules. There are, however, two cautions with respect to the memory. First, use extreme care when handling the core module. There are very fine magnet wires on the exposed component side which can easily be broken. Second, each memory increment (three modules) is in itself a replaceable unit. When failures occur, always replace a complete set. Replacing a single circuit module will change memory alignment and may result in improper operation, particularly at extremes of temperature.

5.24 Power Supply

Access to power supply voltage monitoring points can be obtained by removing the bottom cover to gain access to the motherboard connections.

Removal of the power supply is accomplished by the following steps:

1. Use a Phillips screwdriver to loosen the eight captive screws attaching the power supply to the chassis. Back the screws out until they disengage.

CAUTION

To prevent damage to power supply connector pins, do not rock the power supply during removal or replacement. To prevent arcing and spike transients, never remove (or insert) the power supply with power on. To prevent damage to exposed components, exercise care to avoid scraping the power supply against any part of the processor chassis.

2. Grasp the power supply with both hands and pull it straight out until the power supply connectors just clear the two connector alignment pins. At this point the power supply is resting on rails at the sides of the chassis, and one or both hands may be shifted to permit a more secure hold (Figure 5-3) prior to lifting the power supply free of the chassis.

Replacement of the power supply follows the above procedure in reverse order.

5.25 Front Panel Wiring and EMI Filter

Access to front panel wiring and to the EMI filter is gained by loosening nine captive screws in the connector (front) panel, then hinging the panel down. The EMI filter is attached to the back side of the connector panel by four screws, which are accessed from the front of the connector panel.

5.26 Control Panel

Access to all parts of the control panel can be gained by first removing the rear cover (Figure 5-4). Then, in any order, the Power Supply Assembly, Power Entry Assembly, and bottom cover can be unscrwed from the front panel. A 3 in. screwdriver with a 1/8 in. blade is required to remove the side plates. Assembly and disassembly operations can more easily be made with the control panel resting on its front on a clean table or work bench.

Voltages and waveforms on the logic board can be measured with only the rear cover removed; however, to replace parts on the logic or display boards they should first be removed from the front panel. It is not necessary to disconnect the flat cable jumpers connecting the two assemblies. Unscrew the logic board from the side plate bars.

Remove the control panel power supply and power entry assemblies from the front panel without disconnecting the wiring. Remove the bottom cover, unplug the logic board from the switch board and move it toward the bottom of the control panel giving access to the screws holding the display board. After removing the 12 screws holding the display board, lift it up until the LEDs clear the panel before removing it toward the top of the control panel to clear the switch board.

To remove the switch board it is necessary to loosen the switch mounting nuts on the rear side of the panel, remove the decorative nuts from the switches on the front of the panel, and then lift off the board with the switches still soldered to it.

Reassembly is accomplished by the following previously mentioned steps in the reverse order. Be sure to reinstall the display board with all of its mounting screws because a tight fit between the heat sink board and the front panel is required for maximum heat transfer.

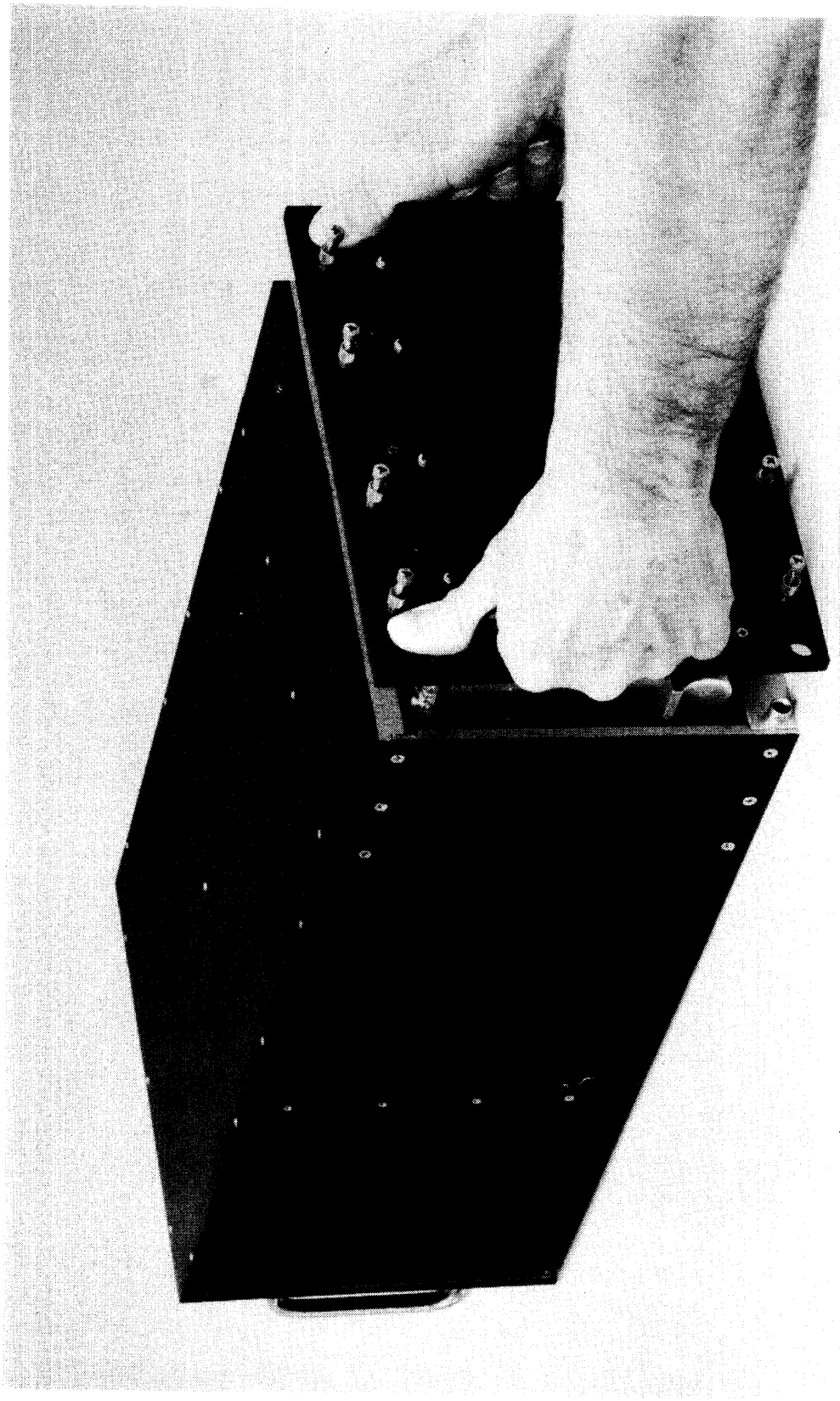

Figure 5-3. Power Supply Removal

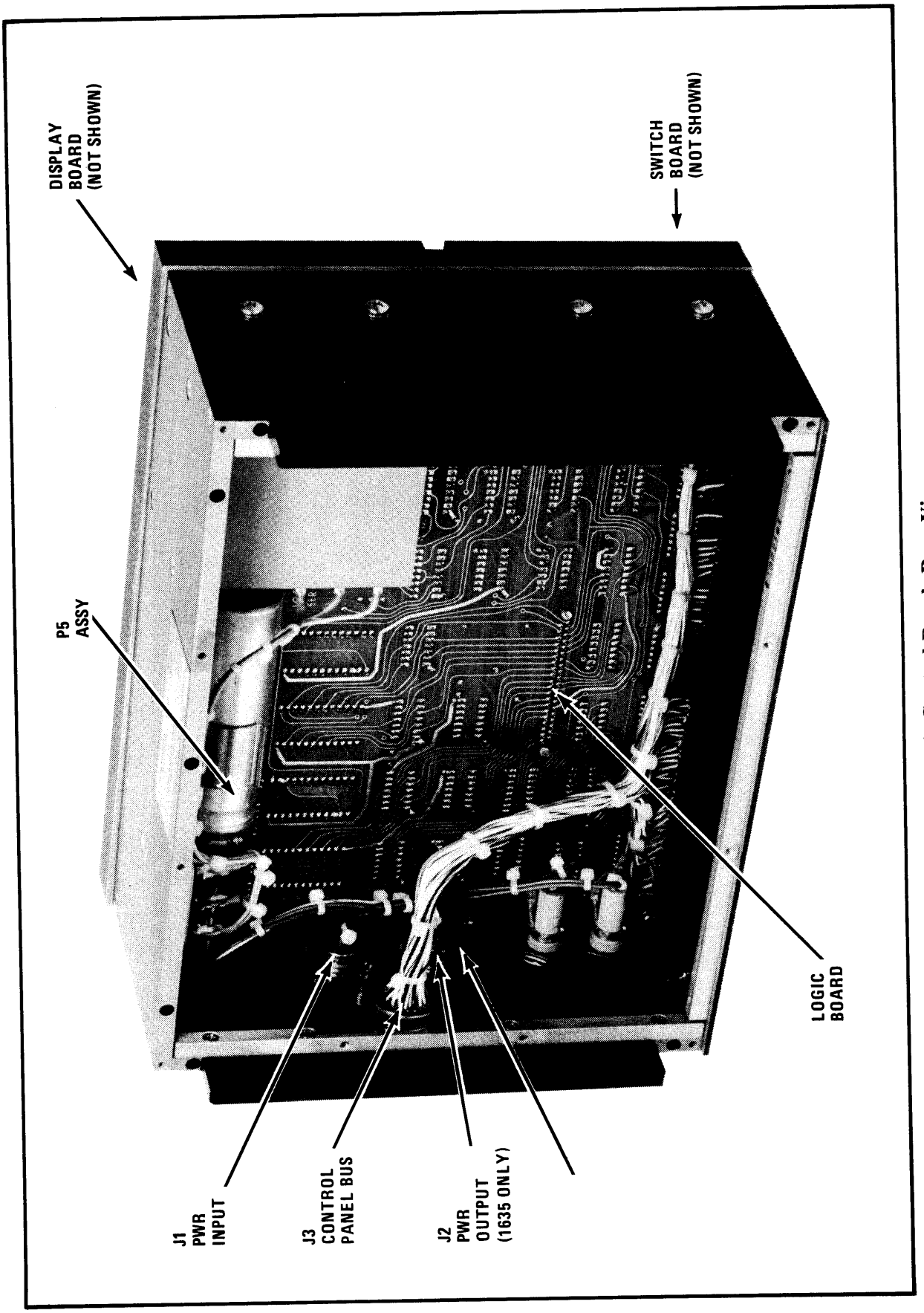

Figure 5-4. Control Panel, Rear View

5.27 INTERNAL ELECTRICAL CONNECTIONS

5.28 Motherboard Wiring

Motherboards (MB) are multilayer printed circuit boards containing the interconnections between plug-in circuit modules. Each circuit module has two VARICON™ type connectors, P1 and P2, for making electrical connections to corresponding J1 and J2 connectors on the motherboard, as shown in Figure 5-5. Motherboard connectors are thus designated by location as A1J1, A1J2, A2J1, etc., and the reference designations are in sequential order throughout the assembly. The two MBs, identified in Figure 5-1, are hardwired together. Wiring of the MBs can be considered in three functional elements: I/O, memory, and CPU.

Memory bus signals are connected to the memory MB and the CPU, and interconnections between the memory modules are contained in the MB. Memory addresses are controlled by MB wiring; i.e., if a memory module is moved from one location to another, it will respond to the address of the new location.

Motherboard wiring connections for the CPU, I/O bus, and memory bus are shown in Table 5-1, and MB wiring connections for Model 2011 Core Memory 16K modules are shown in Table 5-2.

5.29 Front Panel Connectors

Wiring lists for connectors J1 through J8 are given in Section I. Control panel connector (J9) wiring is given in Table 5-3. Power supply connector (J10) wiring is given in Paragraph 2.8. For nuclear event detection, S1 and J4 on the front panel are wired to the motherboard and to J21 (Figure 5-7). (Operation of the optoisolator in the S1 switch assembly to reset the power supply is explained in Appendix D.20.)

5.30 EMI Filter

The EMI filter input connector (P1) plugs into chassis connector J14 and the filter output connector (P2) plugs into chassis connector J13. These connectors are shown in Figure 5-6, and the wiring list for the EMI filter connector is contained in Table 5-6.

5.31 Power Supply Internal Connections

Power is delivered to the chassis via front panel connector J10, which is wired (via J14, the EMI filter, and J13) to connector J12 (Figure 5-7), located on the rear bulkhead. Power supply connector P2 (Figure 5-8) plugs into J12 to receive primary power input, and regulated output voltages are delivered to the motherboard via power supply connector P1, which plugs into chassis connector J11. Wiring lists for power supply connectors P1 and P2 are contained in Tables 5-5 and 5-6. When the processor is equipped with a heat exchanger, power for the blower is provided at J17 (Figure 5-7).

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5.32 ALIGNMENT AND TESTING

In general, no alignment is required following replacement of a part. After any component (or module) has been replaced, all diagnostics should be run. This is to ensure that the replacement is not defective in another area.

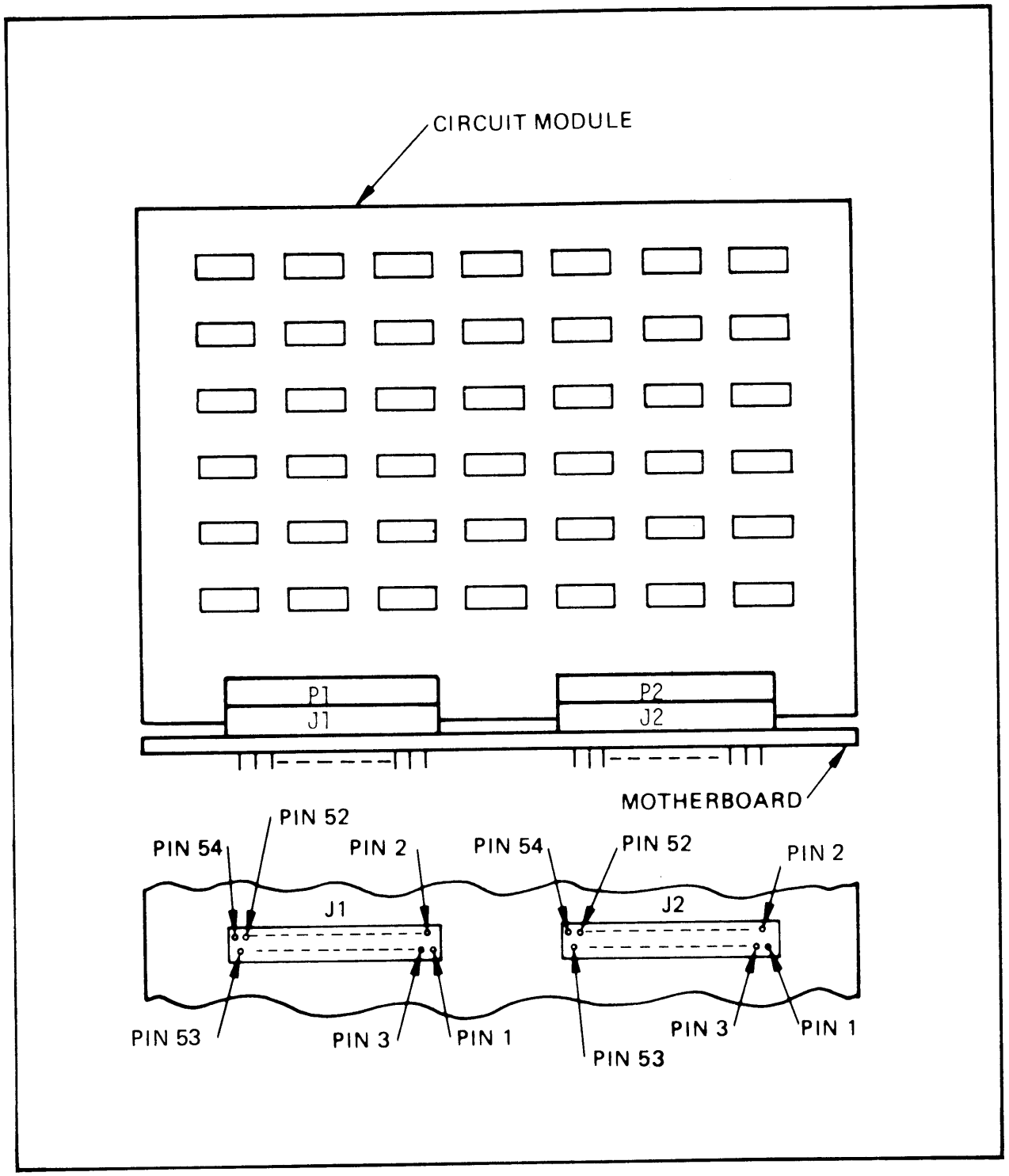

Figure 5-5. Motherboard Connector Layout

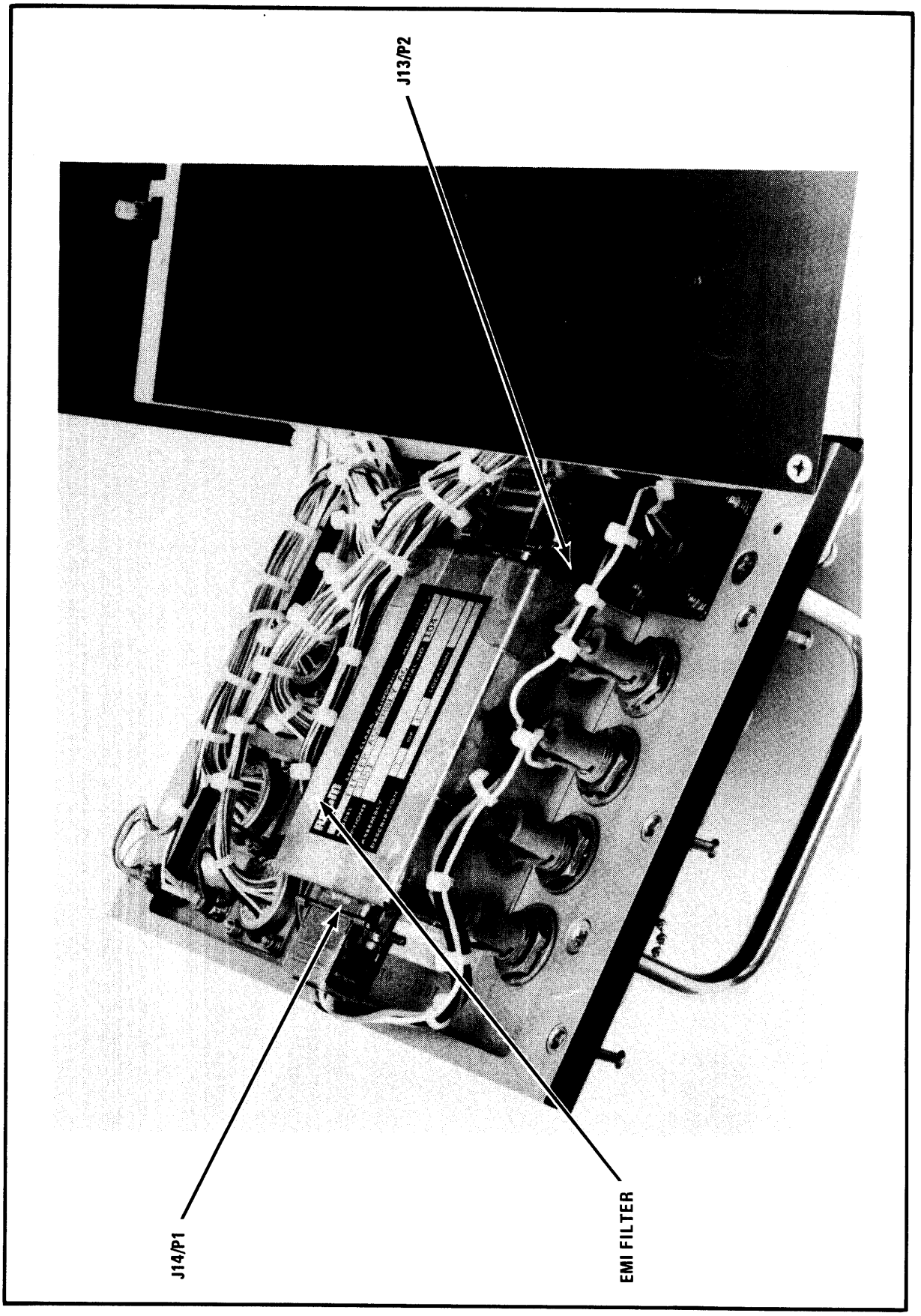

Figure 5-6. EMI Filter and Connectors

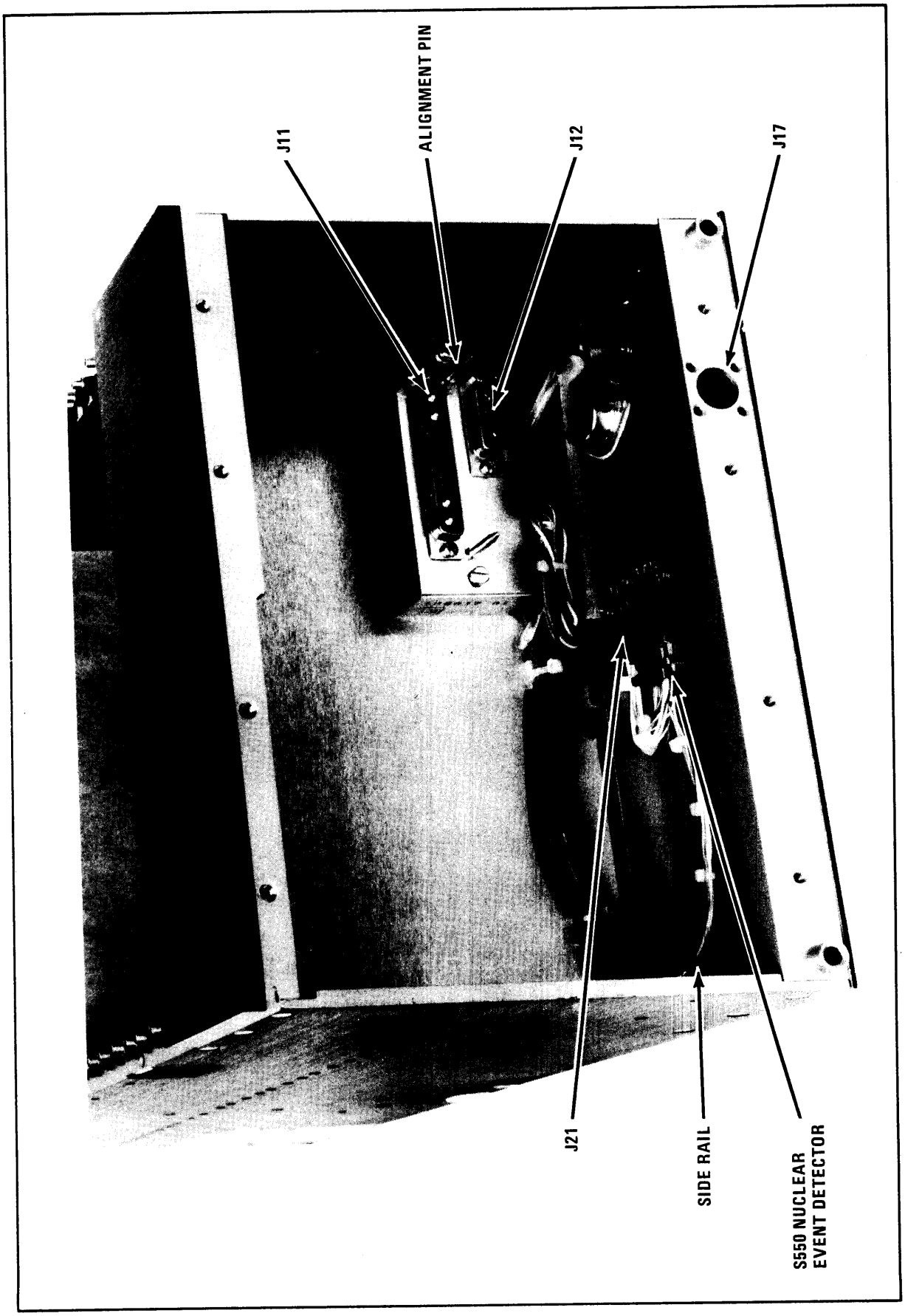

Figure 5-7. Chassis Connectors for Power Supply

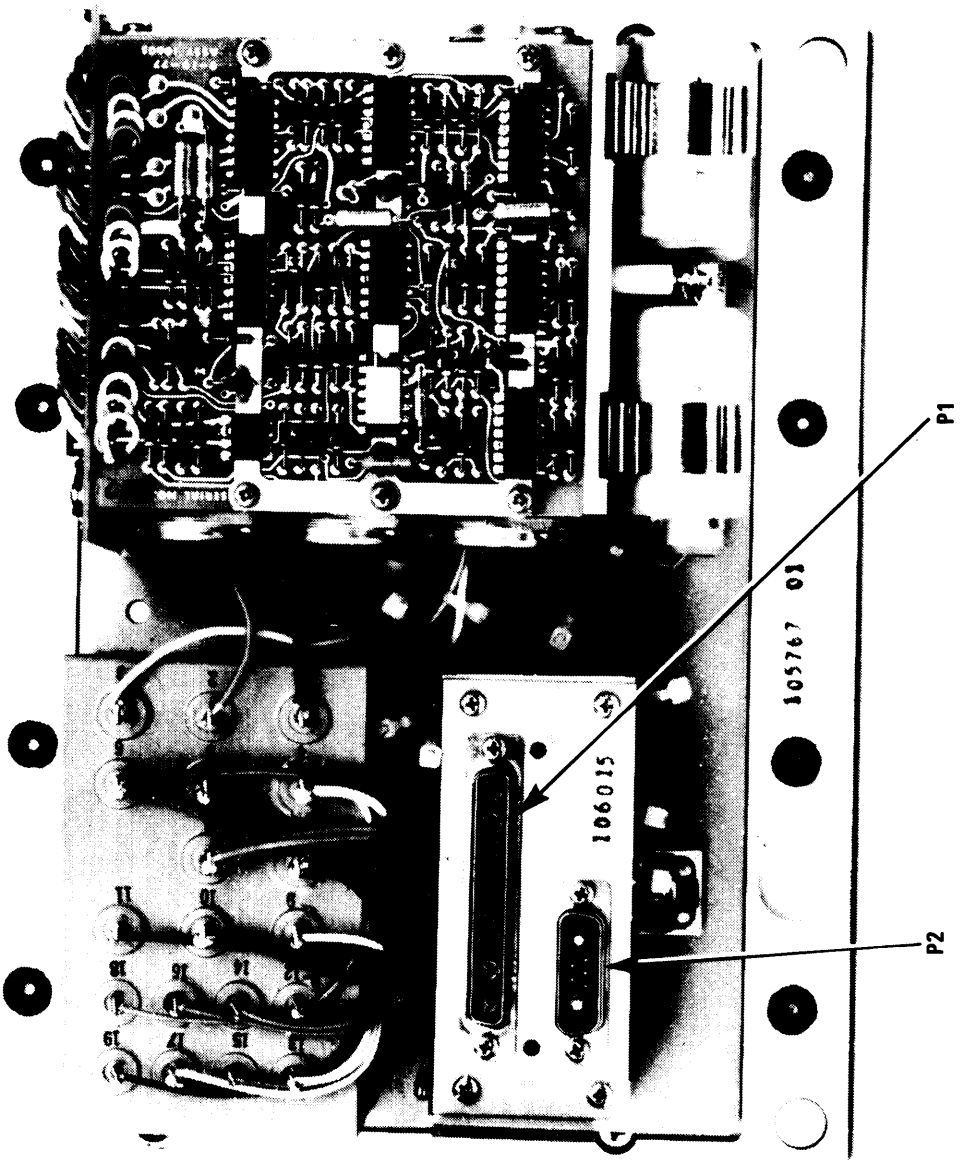

Figure 5-8. Model S665 Power Supply, Rear View

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Table 5-1. 1602B Motherboard A1 (CPU) Interconnection List

FUNCTION	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	E27	E28	E29	E30	E31	Power Supply Pads
	I/O	I/O	I/O	I/O	I/O	I/O	I/O	CPI	CPU	MEM OPT	I/O BUS		CONT PANEL	MEM	MEM	
AWD0*								1-11	1-11	2-28				1-39		
AWD1*								1-13	1-13	2-26				1-38		
AWD2*								1-15	1-15	2-24				1-37		
AWD3*								1-17	1-17	2-20				1-36		
AWD4*								1-19	1-19	2-16				1-35		
AWD5*								1-21	1-21	1-51				1-34		
AWD6*								1-23	1-23	1-50				1-33		
AWD7*								1-25	1-25	1-48				1-32		
AWD8*								1-27	1-27	1-30				1-31		
AWD9*								1-29	1-29	1-29				1-30		
AWD10*								1-31	1-31	1-27				1-29		
AWD11*								1-33	1-33	1-18				1-28		
AWD12*								1-35	1-35	1-16				1-27		
AWD13*								1-37	1-37	1-11				1-26		
AWD14*								1-39	1-39	1-9				1-11		
AWD15*								1-41	1-41	1-7				1-12		
RD0									1-32	2-38					2-25	
RD1									1-30	2-36					2-26	
RD2									1-12	2-13					2-35	
RD3									1-10	2-11					2-36	
RD4									1-6	2-7					2-38	
RD5									1-8	2-9					2-37	
RD6									1-20	2-21					2-31	
RD7									1-18	2-19					2-32	
RD8									1-26	2-27					2-28	
RD9									1-28	2-33					2-27	
RD10									1-14	2-15					2-34	
RD11									1-16	2-17					2-33	
RD12									1-2	2-3					2-40	
RD13									1-4	2-5					2-39	
RD14									1-22	2-23					2-30	
RD15									1-24	2-25					2-29	
READ									1-49						2-10	

NOTES:
1. An asterisk (*) following the function name means signal is true when voltage is low.
2. Table entry n-mp means signal is found on Jn, pin mp of the location given in the heading.
3. A dagger (†) following an entry means the signal originates on the circuit module at that location.

Table 5-1. 1602B Motherboard A1 (CPU) Interconnection List (Continued)

FUNCTION	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	E27	E28	E29	E30	E31	Power Supply Pads
	I/O	I/O	I/O	I/O	I/O	I/O	I/O	CPI	CPU	MEM OPT	I/O BUS		CONT PANEL	MEM	MEM	
READ1*									1-44					1-16		
READ2*									1-40					1-15		
RMODE*								1-58	1-58							
WMODE*								1-61	1-61							
SC*									1-56	2-22					2-17	
HS*									1-57	2-42						
MSEL*									1-45	2-18					2-15	
CLEAR*									1-43	2-40					2-13	
WRITE*									1-42					1-13		
INH*									1-46	1-39					2-14	
STACK BIAS									1-47	1-49					2-11	
MAST*								1-52	1-52	1-1				1-12		
MDST*								1-48	1-48	1-5					2-12	
FETCH*								1-63	1-63							
EXTS								1-65	1-65							
EXT CLK								1-70	1-70							
DATA0*	2-9	2-9	2-9	2-9	2-9	2-9	2-9	2-9	2-9		2-9					
DATA1*	2-11	2-11	2-11	2-11	2-11	2-11	2-11	2-12	2-12		2-11					
DATA2*	2-13	2-13	2-13	2-13	2-13	2-13	2-13	2-14	2-14		2-13					
DATA3*	2-15	2-15	2-15	2-15	2-15	2-15	2-15	2-17	2-17		2-15					
DATA4*	2-17	2-17	2-17	2-17	2-17	2-17	2-17	2-20	2-20		2-17					
DATA5*	2-19	2-19	2-19	2-19	2-19	2-19	2-19	2-22	2-22		2-19					
DATA6*	2-21	2-21	2-21	2-21	2-21	2-21	2-21	2-25	2-25		2-21					
DATA7*	2-23	2-23	2-23	2-23	2-23	2-23	2-23	2-28	2-28		2-23					
DATA8*	2-10	2-10	2-10	2-10	2-10	2-10	2-10	2-10	2-10			2-10				
DATA9*	2-12	2-12	2-12	2-12	2-12	2-12	2-12	2-13	2-13			2-12				
DATA10*	2-6	2-6	2-6	2-6	2-6	2-6	2-6	2-6	2-6			2-6				
DATA11*	2-8	2-8	2-8	2-8	2-8	2-8	2-8	2-8	2-8			2-8				
DATA12*	2-18	2-18	2-18	2-18	2-18	2-18	2-18	2-21	2-21			2-18				
DATA13*	2-16	2-16	2-16	2-16	2-16	2-16	2-16	2-18	2-18			2-16				
DATA14*	2-14	2-14	2-14	2-14	2-14	2-14	2-14	2-16	2-16			2-14				
DATA15*	2-20	2-20	2-20	2-20	2-20	2-20	2-20	2-24	2-24			2-20				
DATIA	2-53	2-53	2-53	2-53	2-53	2-53	2-53	2-66	2-66		2-53					

NOTES:
1. An asterisk (*) following the function name means signal is true when voltage is low.
2. Table entry n-mp means signal is found on Jn, pin mp of the location given in the heading.
3. A dagger (†) following an entry means the signal originates on the circuit module at that location.

Table 5-1. 1602B Motherboard A1 (CPU) Interconnection List (Continued)

FUNCTION	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	E27	E28	E29	E30	E31	Power Supply Pads
	I/O	I/O	I/O	I/O	I/O	I/O	I/O	CPI	CPU	MEM OPT	I/O BUS		CONT PANEL	MEM	MEM	
DATIB	2-37	2-37	2-37	2-37	2-37	2-37	2-37	2-46	2-46		2-37					
DATIC	2-39	2-39	2-39	2-39	2-39	2-39	2-39	2-49	2-49		2-39					
DATOA	2-44	2-44	2-44	2-44	2-44	2-44	2-44	2-54	2-54			2-44				
DATOB	2-38	2-38	2-38	2-38	2-38	2-38	2-38	2-48	2-48			2-38				
DATOC	2-41	2-41	2-41	2-41	2-41	2-41	2-41	2-52	2-52		2-41					
STRT	2-22	2-22	2-22	2-22	2-22	2-22	2-22	2-26	2-26			2-22				
CLR	2-50	2-50	2-50	2-50	2-50	2-50	2-50	2-62	2-62			2-50				
IORST	2-46	2-46	2-46	2-46	2-46	2-46	2-46	2-57	2-57			2-46				
INTA	2-40	2-40	2-40	2-40	2-40	2-40	2-40	2-50	2-50			2-40				
INTR*	2-49	2-49	2-49	2-49	2-49	2-49	2-49	2-61	2-61		2-49					
MSKO*	2-52	2-52	2-52	2-52	2-52	2-52	2-52	2-65	2-65			2-52				
SELB*	2-43	2-43	2-43	2-43	2-43	2-43	2-43	2-53	2-52		2-43					
SELD*	2-45	2-45	2-45	2-45	2-45	2-45	2-45	2-56	2-56		2-45					
DCHR*	2-51	2-51	2-51	2-51	2-51	2-51	2-51	2-64	2-64		2-51					
DCHA*	2-33	2-33	2-33	2-33	2-33	2-33	2-33	2-41	2-41		2-33					
DCHI	2-36	2-36	2-36	2-36	2-36	2-36	2-36	2-45	2-45			2-36				
DCHO	2-35	2-35	2-35	2-35	2-35	2-35	2-35	2-44	2-44		2-35					
DCHM0*	2-1	2-1	2-1	2-1	2-1	2-1	2-1	2-1	2-1		2-1					
RQENB*	2-54	2-54	2-54	2-54	2-54	2-54	2-54	2-68	2-68			2-54				
PRUN*								2-4	2-4							
PRQ*								2-5	2-5							
DS0*	2-32	2-32	2-32	2-32	2-32	2-32	2-32	2-40	2-40			2-32				
DS1*	2-28	2-28	2-28	2-28	2-28	2-28	2-28	2-34	2-34			2-28				
DS2*	2-30	2-30	2-30	2-30	2-30	2-30	2-30	2-37	2-37			2-30				
DS3*	2-26	2-26	2-26	2-26	2-26	2-26	2-26	2-32	2-32			2-26				
DS4*	2-24	2-24	2-24	2-24	2-24	2-24	2-24	2-29	2-29			2-24				
DS5*	2-34	2-34	2-34	2-34	2-34	2-34	2-34	2-42	2-42			2-34				
PBOOT*									2-38							E19
IOPLS	2-29	2-29	2-29	2-29	2-29	2-29	2-29	2-36	2-36		2-29					
FF7*(BITE*)									2-69	2-6						E21
OVFLO	2-47	2-47	2-47	2-47	2-47	2-47	2-47		2-58		2-47					
DCHM1*	2-2	2-2	2-2	2-2	2-2	2-2	2-2		2-2			2-2				
PB0								1-22					2A			

NOTES:
1. An asterisk (*) following the function name means signal is true when voltage is low.
2. Table entry n-mp means signal is found on Jn, pin mp of the location given in the heading.
3. A dagger (†) following an entry means the signal originates on the circuit module at that location.

Table 5-1. 1602B Motherboard A1 (CPU) Interconnection List (Continued)

FUNCTION	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	E27	E28	E29	E30	E31	Power Supply Pads
	I/O	I/O	I/O	I/O	I/O	I/O	I/O	CPI	CPU	MEM OPT	I/O BUS		CONT PANEL	MEM	MEM	
PB1								1-26					2C			
PB2								1-28					3A			
PB3								1-30					3C			
PB4								1-32					4A			
PB5								1-34					4C			
PB6								1-38					5A			
PB7								1-40					5C			
PB8								1-42					6A			
PB9								1-43					6C			
PB10								1-44					7A			
PB11								1-45					7C			
PB12								1-46					8A			
PB13								1-47					8C			
PB14								1-49					9A			
PB15								1-51					9C			
PMAST*								1-53					10A			
PDST								1-56					10C			
PSEL1*								1-57					11A			
PSEL0*								1-59					11C			
PCLR								1-60					12A			
PRUN								1-62					12C			
PPRQ*								1-66					13A			
PINT*								1-67					13C			
PDMA*								1-68					14A			
PANF								1-69					14C			
PRST*									2-30				1A			
PSTOP*									2-33				1C			
MEMOK									1-3							E13
+5OK									1-5	1-4						E12
PWR FAIL*									1-1							E14
GND	2-3	2-3	2-3	2-3	2-3	2-3	2-3	1-8	1-7	1-2	2-2	2-1	1B	1-16		E16
			1-1	1-53		1-53		1-24	1-9	1-54	2-4	2-3	1D	1-17		E18
			1-13					1-36	1-51	2-2	2-6	2-5	2B	1-18		E20

NOTES:
1. An asterisk (*) following the function name means signal is true when voltage is low.
2. Table entry n-mp means signal is found on Jn, pin mp of the location given in the heading.
3. A dagger (†) following an entry means the signal originates on the circuit module at that location.

Table 5-1. 1602B Motherboard A1 (CPU) Interconnection List (Continued)

FUNCTION	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	E27	E28	E29	E30	E3[1]	Power Supply Pads
	I/O	I/O	I/O	I/O	I/O	I/O	I/O	CPI	CPU	MEM OPT	I/O BUS		CONT PANEL	MEM	MEM	
GND			1-34					1-50	1-53	2-54	2-8	2-7	2D	1-19		
			1-53					1-64	1-55		2-10	2-9	3B		2-1	
								2-3	1-59		2-12	2-11	3D		2-2	
								2-15	2-3		2-14	2-13	4B		2-20	
								2-27	2-7		2-16	2-15	4D		2-21	
								2-39	2-11		2-18	2-17	5B			
								2-51	2-15		2-20	2-19	5D			
								2-63	2-19		2-22	2-21	6B			
									2-23		2-24	2-23	6D			
									2-27		2-26	2-25	7B			
									2-31		2-28	2-27	7D			
									2-35		2-30	2-29	8B			
									2-39		2-32	2-31	8D			
									2-43		2-34	2-33	9B			
									2-47		2-36	2-35	9D			
									2-51		2-38	2-37	10B			
									2-55		2-40	2-39	10D			
									2-59		2-42	2-41	11B			
									2-63		2-44	2-43	11D			
									2-67		2-46	2-45	12B			
											2-48	2-47	12D			
											2-50	2-49	13B			
											2-52	2-51	13D			
											2-54	2-53	14B			
													14D			
+12V	2-27	2-27	2-27	2-27	2-27	2-27	2-27	2-35		2-4				1-8		E2
														1-20		
														1-21		
														1-22		
+5V	2-7	2-7	2-7	2-7	2-7	2-7	2-7	2-2	1-34	1-53					2-11	E15
								2-70	1-36	2-1					2-12	E17
									1-38							E22

NOTES:
1. An asterisk (*) following the function name means signal is true when voltage is low.
2. Table entry n-mp means signal is found on Jn, pin mp of the location given in the heading.
3. A dagger (†) following an entry means the signal originates on the circuit module at that location.

Table 5-1. 1602B Motherboard A1 (CPU) Interconnection List (Continued)

FUNCTION	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	E27	E28	E29	E30	E31	Power Supply Pads
	I/O	I/O	I/O	I/O	I/O	I/O	I/O	CPI	CPU	MEM OPT	I/O BUS		CONT PANEL	MEM	MEM	
+5V									1-50							
									1-60							
									1-62							
									1-64							
									1-66							
									1-67							
									1-68							
									1-69							
-12V	2-25	2-25	2-25	2-25	2-25	2-25	2-25	2-33						1-7		E11
-5V														1-37		E3
HAR +5V										1-40						
DETF*										2-50						
DNDATA			1-15													
DNDATA*			1-16													
EFRST										2-10						
ENB			1-6													
ENB*			1-7													
NRST*									1-5							
PBUS*				1-12		1-12										
SBUS*				1-14		1-14										
SEL0			1-43													
			1-44													
SEL2			1-45													
			1-46													
SEL4			1-49													
			1-50													
SL1*, SL2*				1-3		1-3										
				1-4		1-4										
				1-5		1-5										
SL4*				1-15		1-15										
				1-16		1-16										
SL5*						1-17										
						1-18										

NOTES:
1. An asterisk (*) following the function name means signal is true when voltage is low.
2. Table entry n-mp means signal if found on Jn, pin mp of the location given in the heading.
3. A dagger (†) following an entry means the signal originates on the circuit module at that location.

Table 5-1. 1602B Motherboard A1 (CPU) Interconnection List (Continued)

FUNCTION	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	E27	E28	E29	E30	E31	Power Supply Pads
	I/O	I/O	I/O	I/O	I/O	I/O	I/O	CPI	CPU	MEM OPT	I/O BUS		CONT PANEL	MEM	MEM	
UPCLC			1-10													
UPCLC*			1-11													
UPDATA*			1-2													
UPDATA			1-3													

NOTES:
1. An asterisk (*) following the function name means signal is true when voltage is low.
2. Table entry n-mp means signal is found on Jn, pin mp of the location given in the heading.
3. A dagger (†) following an entry means the signal originates on the circuit module at that location.

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Table 5-2. 1602B Motherboard A2 (Memory) Interconnection List

FUNCTION	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	PAD E36	PAD E37	TERMINATOR OR PAD
BAWD 0*	1-1	1-2		1-1	1-2		1-1	1-2		1-1	1-2		1-39		U1-3
BAWD 1*	1-3	1-4		1-3	1-4		1-3	1-4		1-3	1-4		1-38		U1-4
BAWD 2*	1-5	1-6		1-5	1-6		1-5	1-6		1-5	1-6		1-37		U1-12
BAWD 3*	1-7	1-8		1-7	1-8		1-7	1-8		1-7	1-8		1-36		U1-11
BAWD 4*	1-9	1-10		1-9	1-10		1-9	1-10		1-9	1-10		1-35		U1-10
BAWD 5*	1-11	1-12		1-11	1-12		1-11	1-12		1-11	1-12		1-34		U1-9
BAWD 6*	1-13	1-14		1-13	1-14		1-13	1-14		1-13	1-14		1-33		U1-5
BAWD 7*	1-15	1-16		1-15	1-16		1-15	1-16		1-15	1-16		1-32		U1-6
BAWD 8*	1-17	1-18		1-17	1-18		1-17	1-18		1-17	1-18		1-31		U2-3
BAWD 9*	1-19	1-20		1-19	1-20		1-19	1-20		1-19	1-20		1-30		U2-4
BAWD 10*	1-21	1-22		1-21	1-22		1-21	1-22		1-21	1-22		1-29		U2-12
BAWD 11*	1-23	1-24		1-23	1-24		1-23	1-24		1-23	1-24		1-28		U2-11
BAWD 12*	1-25	1-26		1-25	1-26		1-25	1-26		1-25	1-26		1-27		U2-10
BAWD 13*	1-27	1-28		1-27	1-28		1-27	1-28		1-27	1-28		1-26		U2-9
BAWD 14*	1-29	1-30		1-29	1-30		1-29	1-30		1-29	1-30		1-11		U2-5
BAWD 15*	1-31	1-32		1-31	1-32		1-31	1-32		1-31	1-32		1-17		U2-6
RD 0		2-34			2-34			2-34			2-34			2-25	
RD 1		2-32			2-32			2-32			2-32			2-26	
RD 2		2-14			2-14			2-14			2-14			2-35	
RD 3		2-12			2-12			2-12			2-12			2-36	
RD 4		2-8			2-8			2-8			2-8			2-38	
RD 5		2-10			2-10			2-10			2-10			2-37	
RD 6		2-22			2-22			2-22			2-22			2-31	
RD 7		2-20			2-20			2-20			2-20			2-32	
RD 8		2-28			2-28			2-28			2-28			2-28	
RD 9		2-30			2-30			2-30			2-30			2-27	
RD 10		2-16			2-16			2-16			2-16			2-34	
RD 11		2-18			2-18			2-18			2-18			2-33	
RD 12		2-4			2-4			2-4			2-4			2-40	
RD 13		2-6			2-6			2-6			2-6			2-39	
RD 14		2-24			2-24			2-24			2-24			2-30	
RD 15		2-26			2-26			2-26			2-26			2-29	
READ1*	1-32			1-32			1-32			1-32			1-16		
READ2*	1-34			1-34			1-34			1-34			1-15		
READ	1-40			1-40			1-40			1-40				2-10	
WRITE*	1-36			1-36			1-36			1-36			1-14		
INH*	1-48			1-48			1-48			1-48				2-14	
RUN	1-42			1-42			1-42			1-42				2-11	
SC*	1-54			1-54			1-54			1-54				2-17	
MDST*	1-44			1-44			1-44			1-44				2-12	
CLEAR*	1-46			1-46			1-46			1-46				2-13	
MSEL*	1-50			1-50			1-50			1-50				2-15	
WPR*	1-52			1-52			1-52			1-52				2-16	
MAST*	1-38			1-38			1-38			1-38			1-13		
D0*		(1-1	1-6†)		(1-1	1-6†)		(1-1	1-6†)		(1-1	1-6†)			
D1*		(1-3	1-10†)		(1-3	1-10†)		(1-3	1-10†)		(1-3	1-10†)			
D2*		(1-5	1-14†)		(1-5	1-14†)		(1-5	1-14†)		(1-5	1-14†)			

Notes:
1. An asterisk (*) following the function name means signal is true when voltage is low.
2. Table entry n-mp means signal is found on Jn, pin mp of the location given in the heading.
3. ( ) around an entry in the memory column means that signal appears only on that memory.
4. A dagger (†) following an entry means that the signal originates on the circuit module at that location.

Table 5-2. 1602B Motherboard A2 (Memory) Interconnection List (Continued)

FUNCTION	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	PAD E36	PAD E37	TERMINATOR OR PAD
D3*		(1-7	1-18†)		(1-7	1-18†)		(1-7	1-18†)		(1-7	1-18†)			
D4*		(1-9	1-22†)		(1-9	1-22†)		(1-9	1-22†)		(1-9	1-22†)			
D5*		(1-11	1-26†)		(1-11	1-26†)		(1-11	1-26†)		(1-11	1-26†)			
D6*		(1-13	1-30†)		(1-13	1-30†)		(1-13	1-30†)		(1-13	1-30†)			
D7*		(1-15	1-36†)		(1-15	1-36†)		(1-15	1-36†)		(1-15	1-36†)			
D8*		(1-17	1-40†)		(1-17	1-40†)		(1-17	1-40†)		(1-17	1-40†)			
D9*		(1-19	1-44†)		(1-19	1-44†)		(1-19	1-44†)		(1-19	1-44†)			
D10*		(1-21	1-48†)		(1-21	1-48†)		(1-21	1-48†)		(1-21	1-48†)			
D11*		(1-23	1-52†)		(1-23	1-52†)		(1-23	1-52†)		(1-23	1-52†)			
D12*		(1-25	1-56†)		(1-25	1-56†)		(1-25	1-56†)		(1-25	1-56†)			
D13*		(1-27	1-60†)		(1-27	1-60†)		(1-27	1-60†)		(1-27	1-60†)			
D14*		(1-29	1-64†)		(1-29	1-64†)		(1-29	1-64†)		(1-29	1-64†)			
D15*		(1-31	1-68†)		(1-31	1-68†)		(1-31	1-68†)		(1-31	1-68†)			
I0R		(2-7†	1-3)		(2-7†	1-3)		(2-7†	1-3)		(2-7†	1-3)			
I0B		(2-9†	1-4)		(2-9†	1-4)		(2-9†	1-4)		(2-9†	1-4)			
I0A		(2-11†	1-5)		(2-11†	1-5)		(2-11†	1-5)		(2-11†	1-5)			
I1R		(2-13†	1-7)		(2-13†	1-7)		(2-13†	1-7)		(2-13†	1-7)			
I1B		(2-15†	1-8)		(2-15†	1-8)		(2-15†	1-8)		(2-15†	1-8)			
I1A		(2-17†	1-9)		(2-17†	1-9)		(2-17†	1-9)		(2-17†	1-9)			
I2R		(2-19†	1-11)		(2-19†	1-11)		(2-19†	1-11)		(2-19†	1-11)			
I2B		(2-21†	1-12)		(2-21†	1-12)		(2-21†	1-12)		(2-21†	1-12)			
I2A		(2-23†	1-13)		(2 23†	1-13)		(2-23†	1-13)		(2-23†	1-13)			
I3R		(2-25†	1-15)		(2-25†	1-15)		(2-25†	1-15)		(2-25†	1-15)			
I3B		(2-27†	1-16)		(2-27†	1-16)		(2-27†	1-16)		(2-27†	1-16)			
I3A		(2-29†	1-17)		(2-29†	1-17)		(2-29†	1-17)		(2-29†	1-17)			
I4R		(2-31†	1-19)		(2-31†	1-19)		(2-31†	1-19)		(2-31†	1-19)			
I4B		(2-33†	1-20)		(2-33†	1-20)		(2-33†	1-20)		(2-33†	1-20)			
I4A		(2-35†	1-21)		(2-35†	1-21)		(2-35†	1-21)		(2-35†	1-21)			
I5R		(2-36†	1-23)		(2-36†	1-23)		(2-36†	1-23)		(2-36†	1-23)			
I5B		(2-37†	1-24)		(2-37†	1-24)		(2-37†	1-24)		(2-37†	1-24)			
I5A		(2-38†	1-25)		(2-38†	1-25)		(2-38†	1-25)		(2-38†	1-25)			
I6R		(2-50†	1-27)		(2-50†	1-27)		(2-50†	1-27)		(2-50†	1-27)			
I6B		(2-49†	1-28)		(2-49†	1-28)		(2-49†	1-28)		(2-49†	1-28)			
I6A		(2-48†	1-29)		(2-48†	1-29)		(2-48†	1-29)		(2-48†	1-29)			
I7R		(2-47†	1-33)		(2-47†	1-33)		(2-47†	1-33)		(2-47†	1-33)			
I7B		(2-46†	1-34)		(2-46†	1-34)		(2-46†	1-34)		(2-46†	1-34)			
I7A		(2-45†	1-35)		(2-45†	1-35)		(2-45†	1-35)		(2-45†	1-35)			
I8R		(2-44†	1-37)		(2-44†	1-37)		(2-44†	1-37)		(2-44†	1-37)			
I8B		(2-43†	1-38)		(2-43†	1-38)		(2-43†	1-38)		(2-43†	1-38)			
I8A		(2-42†	1-39)		(2-42†	1-39)		(2-42†	1-39)		(2-42†	1-39)			
I9R		(2-41†	1-41)		(2-41†	1-41)		(2-41†	1-41)		(2-41†	1-41)			
I9B		(2-40†	1-42)		(2-40†	1-42)		(2-40†	1-42)		(2-40†	1-42)			
I9A		(2-39†	1-43)		(2-39†	1-43)		(2-39†	1-43)		(2-39†	1-43)			
I10R		(1-35†	1-45)		(1-35†	1-45)		(1-35†	1-45)		(1-35†	1-45)			
I10B		(1-36†	1-46)		(1-36†	1-46)		(1-36†	1-46)		(1-36†	1-46)			
I10A		(1-37†	1-47)		(1-37†	1-47)		(1-37†	1-47)		(1-37†	1-47)			
I11R		(1-38†	1-49)		(1-38†	1-49)		(1-38†	1-49)		(1-38†	1-49)			
I11B		(1-39†	1-50)		(1-39†	1-50)		(1-39†	1-50)		(1-39†	1-50)			

Notes:
1. An asterisk (*) following the function name means signal is true when voltage is low.
2. Table entry n-mp means signal is found on Jn, pin mp of the location given in the heading.
3. ( ) around an entry in the memory column means that signal appears only on that memory.
4. A dagger (†) following an entry means that the signal originates on the circuit module at that location.

Table 5-2. 1602B Motherboard A2 (Memory) Interconnection List (Continued)

FUNCTION	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	PAD E36	PAD E37	TERMINATOR OR PAD
I11A		(1-40†)	1-51)		(1-40†)	1-51)		(1-40†)	1-51)		(1-40†)	1-51)			
I12R		(1-41†)	1-53)		(1-41†)	1-53)		(1-41†)	1-53)		(1-41†)	1-53)			
I12B		(1-42†)	1-54)		(1-42†)	1-54)		(1-42†)	1-54)		(1-42†)	1-54)			
I12A		(1-43†)	1-55)		(1-43†)	1-55)		(1-43†)	1-55)		(1-43†)	1-55)			
I13R		(1-44†)	1-57)		(1-44†)	1-57)		(1-44†)	1-57)		(1-44†)	1-57)			
I13B		(1-45†)	1-58)		(1-45†)	1-58)		(1-45†)	1-58)		(1-45†)	1-58)			
I13A		(1-46†)	1-59)		(1-46†)	1-59)		(1-46†)	1-59)		(1-46†)	1-59)			
I14R		(1-47†)	1-61)		(1-47†)	1-61)		(1-47†)	1-61)		(1-47†)	1-61)			
I14B		(1-48†)	1-62)		(1-48†)	1-62)		(1-48†)	1-62)		(1-48†)	1-62)			
I14A		(1-49†)	1-63)		(1-49†)	1-63)		(1-49†)	1-63)		(1-49†)	1-63)			
I15R		(1-50†)	1-65)		(1-50†)	1-65)		(1-50†)	1-65)		(1-50†)	1-65)			
I15B		(1-51†)	1-66)		(1-51†)	1-66)		(1-51†)	1-66)		(1-51†)	1-66)			
I15A		(1-52†)	1-67)		(1-52†)	1-67)		(1-52†)	1-67)		(1-52†)	1-67)			
IDA*	(2-53†)	2-51)		(2-53†)	2-51)		(2-53†)	2-51)		(2-53†)	2-51)				
IDB*	(2-54†)	2-52)		(2-54†)	2-52)		(2-54†)	2-52)		(2-54†)	2-52)				
IREF	(1-39†)	1-33)		(1-39†)	1-33)		(1-39†)	1-33)		(1-39†)	1-33)				
CDR*	(1-45†)	1-34)		(1-45†)	1-34)		(1-45†)	1-34)		(1-45†)	1-34)				
SDR*	(1-47†)	2-53)		(1-47†)	2-53)		(1-47†)	2-53)		(1-47†)	1-53)				
LWD*	(1-30†)	2-54)		(1-30†)	2-54)		(1-30†)	2-54)		(1-30†)	2-54)				
STRA*	(1-41†)		1-1)	(1-41†)		1-1)	(1-41†)		1-1)	(1-41†)		1-1)			
STRB*	(1-43†)		1-2)	(1-43†)		1-2)	(1-43†)		1-2)	(1-43†)		1-2)			
DB	(1-33†)		2-53,54)	(1-33†)		2-53,54)	(1-33†)		2-53,54)	(1-33†)		2-53,54)			
XS0	(2-51†)		2-16)	(2-51†)		2-16)	(2-51†)		2-16)	(2-51†)		2-16)			
XS1	(2-52†)		2-15)	(2-52†)		2-15)	(2-52†)		2-15)	(2-52†)		2-15)			
XS2	(1-4†)		2-14)	(1-4†)		2-14)	(1-4†)		2-14)	(1-4†)		2-14)			
XS3	(1-2†)		2-13)	(1-2†)		2-13)	(1-2†)		2-13)	(1-2†)		2-13)			
XS4	(1-8†)		2-12)	(1-8†)		2-12)	(1-8†)		2-12)	(1-8†)		2-12)			
XS5	(1-6†)		2-11)	(1-6†)		2-11)	(1-6†)		2-11)	(1-6†)		2-11)			
XS6	(1-12†)		2-10)	(1-12†)		2-10)	(1-12†)		2-10)	(1-12†)		2-10)			
XS7	(1-10†)		2-9)	(1-10†)		2-9)	(1-10†)		2-9)	(1-10†)		2-9)			
XS8	(1-28†)		2-2)	(1-28†)		2-2)	(1-28†)		2-2)	(1-28†)		2-2)			
XS9	(1-26†)		2-1)	(1-26†)		2-1)	(1-26†)		2-1)	(1-26†)		2-1)			
XS10	(1-24†)		2-4)	(1-24†)		2-4)	(1-24†)		2-4)	(1-24†)		2-4)			
XS11	(1-22†)		2-3)	(1-22†)		2-3)	(1-22†)		2-3)	(1-22†)		2-3)			
XS12	(1-20†)		2-6)	(1-20†)		2-6)	(1-20†)		2-6)	(1-20†)		2-6)			
XS13	(1-18†)		2-5)	(1-18†)		2-5)	(1-18†)		2-5)	(1-18†)		2-5)			
XS14	(1-16†)		2-8)	(1-16†)		2-8)	(1-16†)		2-8)	(1-16†)		2-8)			
XS15	(1-14†)		2-7)	(1-14†)		2-7)	(1-14†)		2-7)	(1-14†)		2-7)			
X0A	(2-44†)		2-23)	(2-44†)		2-23)	(2-44†)		2-23)	(2-44†)		2-23)			
X0C	(2-43†)		2-24)	(2-43†)		2-24)	(2-43†)		2-24)	(2-43†)		2-24)			
X1A	(2-47†)		2-20)	(2-47†)		2-20)	(2-47†)		2-20)	(2-47†)		2-20)			
X1C	(2-48†)		2-19)	(2-48†)		2-19)	(2-48†)		2-19)	(2-48†)		2-19)			
X2A	(2-46†)		2-21)	(2-46†)		2-21)	(2-46†)		2-21)	(2-46†)		2-21)			
X2C	(2-45†)		2-22)	(2-45†)		2-22)	(2-45†)		2-22)	(2-45†)		2-22)			
X3A	(2-49†)		2-18)	(2-49†)		2-18)	(2-49†)		2-18)	(2-49†)		2-18)			
X3C	(2-50†)		2-17)	(2-50†)		2-17)	(2-50†)		2-17)	(2-50†)		2-17)			
X4A	(2-41†)		2-26)	(2-41†)		2-26)	(2-41†)		2-26)	(2-41†)		2-26)			
X4C	(2-39†)		2-28)	(2-39†)		2-28)	(2-39†)		2-28)	(2-39†)		2-28)			

Notes:
1. An asterisk (*) following the function name means signal is true when voltage is low.
2. Table entry n-mp means signal is found on Jn, pin mp of the location given in the heading.
3. ( ) around an entry in the memory column means that signal appears only on that memory.
4. A dagger (†) following an entry means that the signal originates on the circuit module at that location.

Table 5-2. 1602B Motherboard A2 (Memory) Interconnection List (Continued)

FUNCTION	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	PAD E36	PAD E37	TERMINATOR OR PAD
X5A	(2-37†)		2-30)	(2-37†)		2-30)	(2-37†)		2-30)	(2-37†)		2-30)			
X5C	(2-35†)		2-32)	(2-35†)		2-32)	(2-35†)		2-32)	(2-35†)		2-32)			
X6A	(2-42†)		2-25)	(2-42†)		2-25)	(2-42†)		2-25)	(2-42†)		2-25)			
X6C	(2-40†)		2-27)	(2-40†)		2-27)	(2-40†)		2-27)	(2-40†)		2-27)			
X7A	(2-38†)		2-29)	(2-38†)		2-29)	(2-38†)		2-29)	(2-38†)		2-29)			
X7C	(2-36†)		2-31)	(2-36†)		2-31)	(2-36†)		2-31)	(2-36†)		2-31)			
YS0	(2-18†)		2-55)	(2-18†)		2-55)	(2-18†)		2-55)	(2-18†)		2-55)			
YS1	(2-16†)		2-57)	(2-16†)		2-57)	(2-16†)		2-57)	(2-16†)		2-57)			
YS2	(2-12†)		2-61)	(2-12†)		2-61)	(2-12†)		2-61)	(2-12†)		2-61)			
YS3	(2-11†)		2-62)	(2-11†)		2-62)	(2-11†)		2-62)	(2-11†)		2-62)			
YS4	(2-17†)		2-56)	(2-17†)		2-56)	(2-17†)		2-56)	(2-17†)		2-56)			
YS5	(2-15†)		2-58)	(2-15†)		2-58)	(2-15†)		2-58)	(2-15†)		2-58)			
YS6	(2-14†)		2-59)	(2-14†)		2-59)	(2-14†)		2-59)	(2-14†)		2-59)			
YS7	(2-13†)		2-60)	(2-13†)		2-60)	(2-13†)		2-60)	(2-13†)		2-60)			
YS8	(2-7†)		2-66)	(2-7†)		2-66)	(2-7†)		2-66)	(2-7†)		2-66)			
YS9	(2-6†)		2-67)	(2-6†)		2-67)	(2-6†)		2-67)	(2-6†)		2-67)			
YS10	(2-4†)		2-69)	(2-4†)		2-69)	(2-4†)		2-69)	(2-4†)		2-69)			
YS11	(2-10†)		2-63)	(2-10†)		2-63)	(2-10†)		2-63)	(2-10†)		2-63)			
YS12	(2-3†)		2-70)	(2-3†)		2-70)	(2-3†)		2-70)	(2-3†)		2-70)			
YS13	(2-9†)		2-64)	(2-9†)		2-64)	(2-9†)		2-64)	(2-9†)		2-64)			
YS14	(2-5†)		2-68)	(2-5†)		2-68)	(2-5†)		2-68)	(2-5†)		2-68)			
YS15	(2-8†)		2-65)	(2-8†)		2-65)	(2-8†)		2-65)	(2-8†)		2-65)			
Y0A	(2-26†)		2-41)	(2-26†)		2-41)	(2-26†)		2-41)	(2-26†)		2-41)			
Y0C	(2-25†)		2-42)	(2-25†)		2-42)	(2-25†)		2-42)	(2-25†)		2-42)			
Y1A	(2-34†)		2-33)	(2-34†)		2-33)	(2-34†)		2-33)	(2-34†)		2-33)			
Y1C	(2-33†)		2-34)	(2-33†)		2-34)	(2-33†)		2-34)	(2-33†)		2-34)			
Y2A	(2-24†)		2-43)	(2-24†)		2-43)	(2-24†)		2-43)	(2-24†)		2-43)			
Y2C	(2-23†)		2-44)	(2-23†)		2-44)	(2-23†)		2-44)	(2-23†)		2-44)			
Y3A	(2-28†)		2-39)	(2-28†)		2-39)	(2-28†)		2-39)	(2-28†)		2-39)			
Y3C	(2-27†)		2-40)	(2-27†)		2-40)	(2-27†)		2-40)	(2-27†)		2-40)			
Y4A	(2-22†)		2-45)	(2-22†)		2-45)	(2-22†)		2-45)	(2-22†)		2-45)			
Y4C	(2-21†)		2-46)	(2-21†)		2-46)	(2-21†)		2-46)	(2-21†)		2-46)			
Y5A	(2-30†)		2-37)	(2-30†)		2-37)	(2-30†)		2-37)	(2-30†)		2-37)			
Y5C	(2-29†)		2-38)	(2-29†)		2-38)	(2-29†)		2-38)	(2-29†)		2-38)			
Y6A	(2-20†)		2-47)	(2-20†)		2-47)	(2-20†)		2-47)	(2-20†)		2-47)			
Y6C	(2-19†)		2-48)	(2-19†)		2-48)	(2-19†)		2-48)	(2-19†)		2-48)			
Y7A	(2-32†)		2-35)	(2-32†)		2-35)	(2-32†)		2-35)	(2-32†)		2-35)			
Y7C	(2-31†)		2-36)	(2-31†)		2-36)	(2-31†)		2-36)	(2-31†)		2-36)			
GND													1-3		E32
GND													1-5		E35
GND													1-7		
GND													1-9		
GND													1-17		
GND	2-2	2-3	2-49	2-2	2-3	2-49	2-2	2-3	2-49	2-2	2-3	2-49	1-18		
GND	1-51	2-1	2-50	1-51	2-1	2-50	1-51	2-1	2-50	1-51	2-1	2-50	1-19		U1-7
GND		1-53	2-51		1-53	2-51		1-53	2-51		1-53	2-51	1-20		U2-7
GND			1-70			1-70			1-70			1-70	1-25		
GND														2-6	
GND															

Notes:
1. An asterisk (*) following the function name means signal is true when voltage is low.
2. Table entry n-mp means signal is found on Jn, pin mp of the location given in the heading.
3. ( ) around an entry in the memory column means that signal appears only on that memory.
4. A dagger (†) following an entry means that the signal originates on the circuit module at that location.

Table 5-2. 1602B Motherboard A2 (Memory) Interconnection List (Continued)

FUNCTION	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	PAD E36	PAD E37	TERMINATOR OR PAD
GND														2-8	
GND														2-22	
GND														2-24	
+5V													1-2		E33
+5V													1-4		
+5V													1-6		
+5V													1-8		
+5V													1-24		
+5V														2-5	
+5V														2-7	
+5V	2-1	2-5	1-32	2-1	2-5	1-32	2-1	2-5	1-32	2-1	2-5	1-32		2-18	U1-14, E22
+5V														2-19	U2-14
+5V														2-20	
+5V														2-21	
+5V														2-23	
-5V			1-69			1-69			1-69			1-69	1-40		E36-40
+12V	1-53	1-54	2-52	1-53	1-54	2-52	1-53	1-54	2-52	1-53	1-54	2-52	1-21		E34
+12V		2-2			2-2			2-2			2-2		1-22		
+12V													1-23		
-12V			1-31			1-31			1-31			1-31	1-1		
														1-6†)	
														1-10†)	
														1-14†)	

Notes:
1. An asterisk (*) following the function name means signal is true when voltage is low.
2. Table entry n-mp means signal is found on Jn, pin mp of the location given in the heading.
3. ( ) around an entry in the memory column means that signal appears only on that memory.
4. A dagger (†) following an entry means that the signal originates on the circuit module at that location.

Table 5-3. Control Panel Connector J9

Pin No.	Function	Pin No.	Function
1	PB0	29	PB14RET
2	PB1	30	PB15
3	PB2	31	PB15 RET
4	PB3	32	PB12 RET
5	PB3 RET	33	PRST*
6	PB0 RET	34	PRST RET
7	PB1 RET	35	PSTP*
8	PB2 RET	36	PSTP RET
9	PB4	37	PRQ
10	PB5	38	PRQ RET
11	PB5 RET	39	SPARE
12	PB6	40	PMAST
13	PB6 RET	41	PMAST RET
14	PB7	42	PDST
15	PB7 RET	43	PDST RET
16	PB4 RET	44	PCLR
17	PB8	45	PCLR RET
18	PB8 RET	46	PRUN
19	PB9	47	PSEL0*
20	PB9 RET	48	PSEL0 RET
21	PB10	49	PSEL1*
22	PB10 RET	50	PINT*
23	PB11	51	PDMA*
24	PB11 RET	52	PANF
25	PB12	53	PSEL1 RET
26	PB13	54	PINT RET
27	PB13 RET	55	PDMA RET
28	PB14		

*Indicates active-low

Table 5-4. EMI Filter Connectors

P1 Pin No.	Function	P2 Pin No.	Function
A1	– DC	A1	– DC
1	NC	1	NC
2	NC	2	NC
3	Chassis Ground	3	NC
4	NC	4	NC
5	NC	5	NC
A2	+ DC	A2	NC
			+ DC

Table 5-5. Power Supply Connector P1

Pin No.	Function	Pin No.	Function
A1	Signal Ground	10	PWR FAIL*
A2	Signal Ground	11	MEM OK
1	Signal Ground	12	+ 5 OK
2	Chassis Ground	13	– 12 VDC
†3	+ 15 VDC	14	– 12 VDC
†4	– 15 VDC	15	+ 12 VDC
†5	– 6 VDC	16	+ 12 VDC
6	– 5 VDC	17	+ 12 VDC
7	– 5 VDC	A3	+ 5 VDC
8	+ 5V Sense Return	A4	+ 5 VDC
9	+ 5V Sense		

† Used for test purposes only
*Indicates active signal

Table 5-6. Power Supply Connector P2

Pin No.	Function
A1	– DC
1	Reset Contact
2	Closure
3	Chassis Ground
4	NC
5	NC
A2	+ DC

SECTION VI
SCHEMATICS

This section contains circuit schematics for the Model 1602B/D Processor power supply and control panel. Schematics for the CPU, core memory, and EMI filter are not included because each is replaceable only as a module, and is not field-serviceable. Schematics for I/O options are contained in Appendices B and D; schematics for other system options are included in Appendix C.

The following schematics are included in this section:

Power Supply Model S665 (DC)	00-110920
Control Panel Model 1638 (DC)	00-107280