INSTRUCTION MANUAL

COMPUTER OF AVERAGE TRANSIENTS
CAT
SERIES 400

TECHNICAL MEASUREMENT CORPORATION
TMC MNEMOTRON DIVISION

EXECUTIVE SALES OFFICE
202 Mamaroneck Avenue
White Plains, New York

MANUFACTURING AND SERVICE
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0861

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Warranty

Equipment manufactured by TECHNICAL MEASUREMENT CORPORATION is fully guaranteed as to material and workmanship for a period of ONE YEAR. Auxiliary components supplied, but not manufactured by TMC are guaranteed by the respective manufacturers of the units. TECHNICAL MEASUREMENT CORPORATION reserves the right to perform warranty service operations either in its own factory, at an authorized repair station, or in the customer's installation. Our obligation under this Warranty is limited to repairing, or at our discretion replacing any defective parts thereof except fuses or batteries, without charge, if such defects occur in normal service, and provided the equipment or defective parts are returned, transportation charges prepaid, to the factory or other service point designated by TECHNICAL MEASUREMENT CORPORATION. Cathode-Ray tubes are guaranteed for a period of ONE YEAR. Cathode-Ray tubes are replaced at no cost for a period of NINETY DAYS and are prorated thereafter for an additional period of NINE MONTHS.

If any defect in material or workmanship is found which is covered by this Warranty, the following steps should be taken:

1. Notify us, giving full particulars of the difficulty and including the model and serial number of the instrument in question. On receipt of this information, we will give you service information or shipping instructions.
2. If return of equipment is deemed necessary, shipping instructions will be forwarded together with an Authorized Return Certificate.
3. On receipt of shipping instructions, forward the apparatus to us prepaid, and we will immediately make repairs and adjustments at the factory and return the equipment to you prepaid.
4. If, during the Warranty period, it is disclosed by our examination that the fault has been caused by misuse or abnormal operating conditions, repairs will be billed at cost. In this case, an estimate of the cost will be submitted before the work is started.

Claims for damage in shipment should be filed promptly with the transportation company. All correspondence covering the instrument should specify the model and serial number and Authorized Return Certificate number.

TECHNICAL MEASUREMENT CORPORATION

441 WASHINGTON AVENUE
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Figure 1–1. Computer of Average Transients, Model 400B (CAT).

SECTION I
INTRODUCTION

1.0 GENERAL

The MNEMOTRON Computer of Average Transients (CAT) (see figure 1–1) is a special-purpose digital computer capable of isolating and evaluating small electrical responses masked by random background noise. This is done on-line, permitting the investigator to monitor and adjust parameters of the experiment while in progress. A summation (averaging) technique is automatically programmed which phase-locks the desired signal with relation to a known stimulus or reference pulse and sums successive responses. As a result, the signal under investigation will add arithmetically and the random background noise which sums out of phase will tend to cancel out.

The CAT incorporates its own analog-to-digital converters, thereby providing for the analysis of analog input signals on-line. The CAT outputs provide both digital and analog data for subsequent analysis. A three inch oscilloscope continuously displays the CAT memory contents during accumulate and display modes.

Digital output in binary-coded-decimal (BCD) form can be used with such MNEMOTRON units as the Model 500 Paper Tape Printer, the Model 510 Typewriter Drive Unit for IBM typewriter print-outs, or the Model 520 Type-Punch-Read Control Unit for punch-read devices.

An analog output of 0 to 100 millivolts is provided for use with strip-chart recorders and X-Y plotters.

1.1 DESIGN FEATURES

PORTABILITY—The Computer of Average Transients is designed for use within the immediate area of experimentation. The unit, weighing 38 pounds, and occupying a space 8-1/2 X 10-1/2 X 22 inches can easily be transported to any location for a variety of applications.

FLEXIBILITY—Experimental procedures incorporating the CAT may be modified by the operator at any time during the investigation. This provides considerable flexibility in its operation and requires no special programming techniques.

EXTERNAL CONNECTIONS—External connections on the instrument are available to permit operation from remote equipment. Provisions are also available for the use of external stimuli for reference pulses as well as internal stimuli capable of activating remote ancillary instrumentation.

MEMORY CAPABILITY—The CAT is composed of a magnetic core system in which the data are stored in BCD form. There are 400 memory addresses, each capable of storing 20 binary digits (bits) representing a count of 10^5-1 in decimal form. Total memory consists of 8000 cores. Memory addresses capable of storing 24 bits (10^6-1) are also available.

ADD OR SUBTRACT FEATURE—Memory information can be stored in either an ADD or SUBTRACT mode. This feature permits a response signal to be added or subtracted from the data already existing in the CAT memory.

OSCILLOSCOPE DISPLAY—A 3″ High-Resolution CRT integral to the unit is provided to monitor the data accumulated in the memory system. It gives an analog display of the stored information and can easily be adjusted for signal delineation. Provisions are available in the Model 400B for slaved operation of external oscilloscope equipment.

ADDRESS IDENTIFICATION—Alternate groups of 10 addresses are intensified for easier identification of data location within the CAT memory.

INPUT ADAPTABILITY—One, two, or four input selections can be obtained which permit processing of individual or up to four simultaneous or consecutive response signals. Outputs clearly define each signal and the CRT simultaneously displays the separate and distinct responses.

TRANSISTORIZATION—The instrument is completely transistorized. All components are mounted on printed circuit boards to insure reliable operation under rugged environmental conditions.

PLUG-IN CARDS—Plug-in circuit board cards are used throughout the unit, providing simple replacement when necessary. Extension cards are provided for testing plug-in cards while the CAT is operating.

ACCESSORY INTEGRATION—The CAT Series 600 Accessories have been designed for use with the MNEMOTRON Computer of Average Transients. They provide the CAT with additional features which greatly expand its capabilities and operation. The following list outlines the current Series 600 Accessories with a brief description of their functions.

SERIES 600 ACCESSORIES

Model No.	*Name*	*Function*
600	CAT ACCESSORY CABINET	Houses Series 600 Accessories. Contains internal power supply for all connected accessories. Provides for all necessary connections to CAT and ancillary equipment.
605	AMPLITUDE DISCRIMINATOR	Contains adjustable baseline voltage selector. Transmits a pulse to CAT when preselected baseline amplitude is exceeded, followed by a pulse when voltage drops below preset amplitude.
606	AMPLITUDE-TO-TIME CONVERTER	Sorts input pulses from zero to ten volts into 400 memory addresses. The CAT receives this programmed data and deposits one count into an address proportional to the amplitude of the input signal.
620	READOUT CONTROL (retrace suppressor)	Eliminates visible traces on associated X-Y plotters when more than one trace is utilized.
635	MEMORY RESET UNIT	Permits manual reset of any memory quarter in the CAT.
645	PRESET SWEEP COUNTER	Permits manual selection of number of CAT analysis sweeps and terminates operation when preset number has been reached. Electromechanically displays sweep numbers downward from preselection to 0000.
646	PRESET SWEEP COUNTER	Permits manual selection of number of CAT analysis sweeps and terminates operation when preset number has been reached. Electronically displays sweep numbers upward from zero to preselected number.

CABLES

3-BNC Cables	Connections from:
(Used only with Models 605 & 606)	J601 to CAT J101
(Used only with Models 605 & 606)	J602 to CAT J107
(Used only with Model 606)	J603 to CAT J103
1-Cable	Connections from J103 to CAT J110, J111, J112
1-Cable	Connections from J109A to CAT J109
1-Cable	3-wire connection to AC power

1.2 SPECIFICATIONS

1.2.1 ELECTRICAL CHARACTERISTICS

INPUTS

Connectors	4 Signals to pin 1 and 2 Chassis ground—pin 3 (pin 1 negative with respect to pin 2 causes reduction of modulator frequency)
Impedance	20,000 ohms
Signal (for linear operation)	Plus or minus 3 volts (6 volts peak to peak)
Maximum	50 volts internally clipped to approximately plus or minus 4 volts
Common Mode Voltage	300 volts maximum
Remote Controls	For start, display, readout, stop, reset function, and external control of input modulators

OUTPUTS

Digital	binary coded decimal (address and arithmetic)
Analog	0 to plus 100 millivolts (for X and Y data)
Stimulus Pulse	plus 50 volts—Model 400B plus 15 volts—Models 400, A, H (10 millisecond duration, approximately 1 microsecond risetime, 20,000 ohms impedance)
Monitor	3-inch Cathode Ray Tube
Readout Speeds	0.8, 4, 16, 40 or 400 seconds—Model 400, H 12 to 120 seconds (continuously variable)—Models 400A, B

OPERATING CHARACTERISTICS

Addresses (Analysis Points)	400
Analysis Time	31.25, 62.5, 125, 250 milliseconds, 0.5, 1.0, 2, 4, 8, 16 seconds—Model 400B 62.5, 125, 250 milliseconds, 0.5, 1.0, 2, 4, 8, 16, 32 seconds—Models 400, A, H (Can be varied externally from 20 milliseconds to any desired value)
Memory Capacity	10^5—1 counts per address 10^6—1 counts per address (available on request)
Delay (between stimulus and response analysis)	100 microseconds or approximately 0.1 to 10 seconds (variable)
Storage Cycle Time	36 microseconds
External Address Advance Rate	20,000 addresses per second
Modulator Linearity (Analog to Digital Converter)	plus or minus 0.5 per cent of full scale
Modulator Frequencies (Analog to Digital Converter)	50, 100, 250, 500 KC
Maximum Input Rate to Modulators	2500 cps

PROGRAM SWITCH C POSITION	
External Trigger	
Rise Time	10 microseconds
Minimum Input Voltage	plus 2 volts (minus 2 volts on Model CAT 400)
Maximum Repetition Rate	50 pps
External Address Advance	
Rise Time	less than 10 microseconds
Minimum Input Voltage	plus 1 volt
Maximum Repetition Rate	20,000 pps
PROGRAM SWITCH H POSITION	
Maximum Address Advance Rate	800,000 pps
Maximum Address Reset Rate	10,000 pps
PROGRAM SWITCH D POSITION	
Maximum Address Advance Rate	800,000 pps
Maximum External Trigger Rate	10,000 pps
Maximum Address Reset Rate	10,000 pps
POWER REQUIREMENTS	
Voltage	100, 115, 200, 215 or 230 volts ac
Frequency	50 to 400 cps
Power	30 watts (approximately)
DC Operation	DC to AC converter available

1.2.2 PHYSICAL DIMENSIONS

Height	10-1/2 inches
Width	8-1/2 inches
Length	22 inches
Weight	38 pounds (approximately)

SECTION II
OPERATING INSTRUCTIONS

2.0 GENERAL

This section contains operating and checkout procedures for the Computer of Average Transients (CAT). Paragraph 2.2 and figures 2–1, 2–2, 2–3, detail all controls, indicators and connectors.

2.1 PREOPERATION INSPECTION

2.1.1 UNPACKING

The CAT is carefully packed into a custom-fitted shipping container at the factory. No special instructions are required to unpack the unit, but extreme caution should be taken not to damage the instrument. Containers should be stored until checkout has been completed in case reshipment is necessary.

2.1.2 VISUAL INSPECTION

After the equipment has been unpacked, perform a thorough visual inspection. Make certain that all knobs and connectors are secure and that there is no external damage.

Loosen four fasteners on each side cover. Without removing cards, thoroughly inspect exposed wiring and plug-in cards for obvious damage. Should front panel knobs appear loose, allen wrenches will be found on left-hand side under CRT.

NOTE

If necessary to remove plug-in cards, do not remove more than one card at a time without marking so that card can be returned to proper position.

CAUTION

Do not remove or replace any cards with power on. Before removal make certain POWER switch is at OFF position.

2.2 CONTROLS, INDICATORS, AND CONNECTORS

The following paragraphs outline the controls, indicators, and connectors for the Computer of Average Transients (CAT).

2.2.1 FRONT PANEL (See figures 2–1, 2–2.)

R5 — VERT. SIZE Control—The VERT. SIZE control is a vernier which covers the range between two adjacent positions of the VERT. RANGE (S3) switch. In the maximum clockwise position of the VERT. SIZE control the full scale values as indicated by the VERT. RANGE switch apply. This position should be used at all times when quantitative amplitude data are to be derived from the displayed trace either by visual inspection or photography. The scale on this control is not calibrated; it is intended to aid the experimenter to find a given setting after the position has been altered. Scale gradations provided only on Models 400A, 400B.

RV254-1 — INTENSITY Control—Dims or brightens CRT display. Proper adjustment of this control will provide for intensity modulation of every 10 addresses for detailed visual inspection of trace on CRT. Alternate addresses are brightened when control is rotated counterclockwise.

RV105-2 — FOCUS Control—Sharpens focus of CRT display.

CRT — SCALE ILLUM. Control—Dims or brightens scale graticules on CRT window. Provided only on Models 400A, 400B.

R1, R2, R3, R4 — VERT. POS. Controls—The VERT. POS. controls (4 potentiometers) determine the vertical location of subgroups of the memory on the CRT display. With the INPUTS IN USE switch on 4, each control positions the trace recorded from the input carrying the same number. At two inputs in use, control 1 positions the trace recorded from input 1, and control 3 the one recorded from input 2. At one input in use, control 1 positions the entire trace.

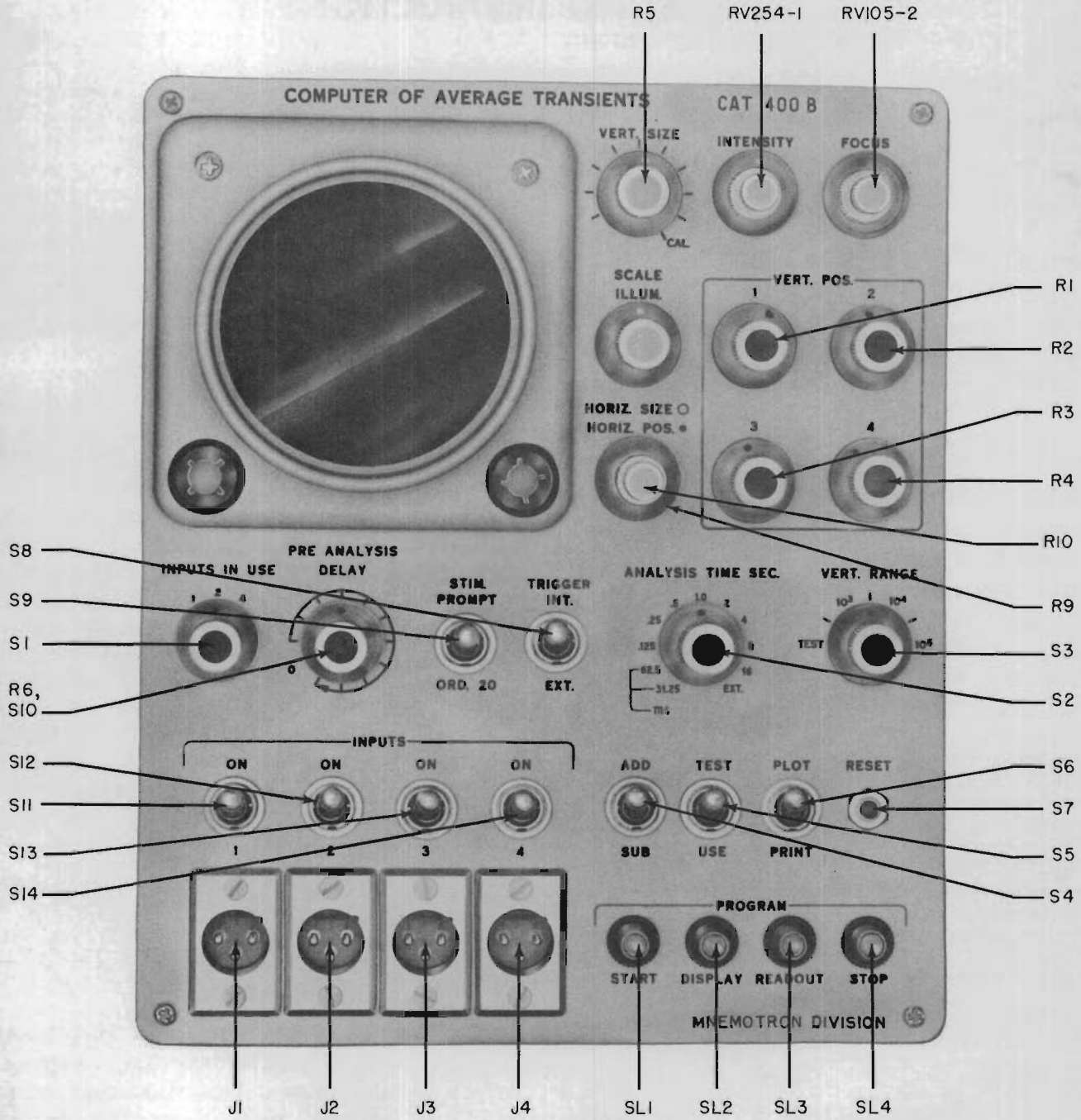


Figure 2–1. Computer of Average Transients, Models 400A, 400B (CAT), Front View.

R9 HORIZ. SIZE Control—Controls width of traces on CRT display.

R10 HORIZ. POS. Control—Positions all traces horizontally.

S1 INPUTS IN USE Selector Switch—The INPUTS IN USE switch selects the number of subgroups of the memory and, therefore, the number of inputs which may be used to receive input information.

In the 1 position only signals supplied to input 1 will be accumulated. The whole memory is used to store the information.

In the 2 position the memory is divided into two subgroups of 200 addresses each. Information is received through inputs 1 and 2 only on a time shared basis; i.e., the signal from input 1 only is routed to zero address of the memory for a predetermined period of time (selected by the ANALYSIS TIME switch), then the signal from input 2 is routed to address 200 of the memory for the same period of time, the further sequence being 1, 201; 2, 202; 3, 303; etc. . . .

In the 4 position the memory is divided into four subgroups and signal information is received through all four inputs again on a time sharing basis. The sequence is:

Time
Interval $t_1 = t_2 = t_3 = t_4 = t_5 = t_6 = t_7 = t_8 = t_9$

Input 1	0				1				2
Input 2		100				101			
Input 3			200				201		
Input 4				300				301	

Addresses

$t_n = \frac{ta}{400}$ where t_n = time interval or dwell time, and ta = analysis time as set on front panel.

R6/S10 PRE ANALYSIS DELAY Control—The PRE ANALYSIS DELAY control provides a delay between the application of a trigger pulse and the start of the analysis sweep. In its maximum counterclockwise (detent) position there is no delay between the application of a trigger pulse and the start of the analysis sweep. Moved out of the detent position a minimum delay between receiving a trigger pulse and the start of the analysis sweep of 100 milliseconds is provided which may be continuously increased to approximately 10 seconds at maximum clockwise position of the control. The scale on this control is not related to the actual delay time but is only provided to aid the experimenter to repeat a previously used setting. (The trigger pulse may be either internally or externally generated.)

S9 STIMULUS Switch—The STIMULUS switch provides 50 volt positive pulse at J105 on the rear panel when the CAT is in the accumulate mode, START switch (SL1) lit. For the other CAT 400 models this pulse is plus 15 volts. If this switch is in the PROMPT position a pulse will occur at the time of the start of each analysis sweep. In the ORD. 20 position this pulse is generated when the sweep passes through address 20.

S8 TRIGGER Switch—With the TRIGGER switch in the EXT. position, an external trigger pulse of at least plus 2 volts applied to J107 on the rear panel is required to actually start on analysis sweep. At the end of a sweep the CAT will return to zero address and wait for a new trigger pulse to initiate another sweep. START pushbutton (SL1) must be depressed before an analysis sweep can be started. Model 400 requires a minus 2 volt trigger pulse.

On the INT. position a sweep is started 50 microseconds after depressing the START pushbutton (SL1) and from thereon 100 microseconds after completion of each sweep.

S2 ANALYSIS TIME SEC. Switch—The ANALYSIS TIME switch determines the period of time, in seconds or milliseconds, allocated for each complete analysis sweep of 400 addresses and, consequently, the time per address is the ANALYSIS TIME divided by 400. Regardless of the position of the INPUTS IN USE switch (S1), the time per

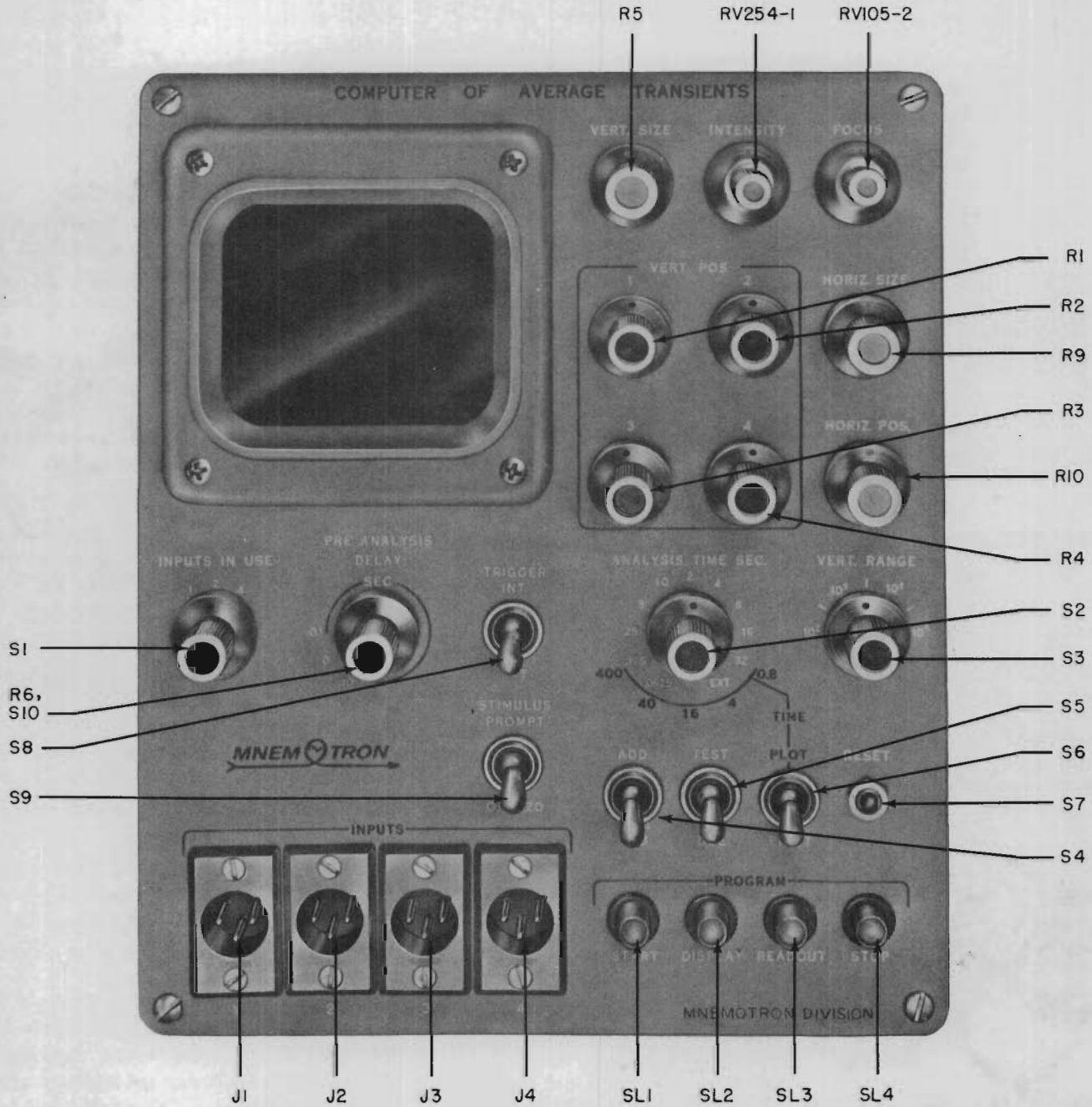


Figure 2–2. Computer of Average Transients, Models 400, 400H (CAT), Front View.

analysis sweep is always as determined by the position of S2. When this control is in the EXT. position the addresses may be advanced at any desired rate up to 20,000 addresses per second (ANALYSIS TIME of 20 milliseconds) by supplying external pulses to J103.

The earlier Model CAT 400 also has a plot time selector operated by the same control. In this case, the knob has one blue dot and one red dot. The blue dot should be in line with the desired analysis time of the inner (white) nomenclature. The red dot should be lined up with a suitable plotting time on the outer (red) nomenclature when the CAT is in readout mode. For Models CAT 400A and B see Rear Panel, PLOT TIME control (R102, figure 2–3).

S3 VERT. RANGE Switch—The VERT. RANGE switch determines the full scale vertical range of the analog output as displayed on the CRT. The line beyond each power of ten setting represents the next higher setting divided by a factor of 3. (Thus a full scale display represents 333, 3333, or 33,333 counts in one of these intermediate positions.) Only the three most significant decades are displayed. The setting of this switch does not alter the capacity of the memory, it merely affects the display on the CRT and the analog voltage output of the CAT.

J1, J2, J3, J4 Input Connectors—The Inputs are directly coupled to the modulators. No amplification is provided. They are isolated from ground and from each other so that signals floating at different dc levels may be connected. The signals should be connected to pins 1 and 2. Pin 3 is connected to chassis ground and is used to ground the shield of the input cable if a shielded cable is employed.

The input impedance is approximately 20,000 ohms. A maximum signal of plus or minus 3 volts (6 volts peak to peak) may be applied to pins 1 and 2. It will result in a plus or minus 50 per cent deviation from the modulator zero signal frequency (input shorted). When the signal voltage on pin 1 is positive with respect to pin 2, a decrease in modulator frequency will result and vice versa. Maximum floating voltage is 300 volts. Thus signals may be applied to pins 1 and 2 which come from "push-pull" circuits and therefore have a common voltage with respect to ground.

An internal clipping circuit limits a maximum input signal to 50 volts applied to the modulator to approximately plus or minus 4 volts.

If one side of the output of a preceding amplifier is grounded, either pin 1 or pin 2 may be connected to the ground terminal of the amplifier.

S11, S12, S13, S14 INPUT Switches—Input signals will only be recorded if the switch located above each input is at the ON position. These switches provide a convenient means of preventing accumulation without physically disconnecting the input plug. This is particularly useful when signals to the different inputs are to be recorded consecutively. Provided only on Models 400A, 400B.

S4 ADD/SUB Switch—The ADD/SUB switch determines whether incoming information is added to or subtracted from the contents of the memory. In normal use it should be in the ADD position. The SUB position may be used to subtract new information from a previously recorded response to obtain the difference between the two signals.

S5 TEST/USE Switch—When the TEST/USE switch is placed in the TEST position, a test program is provided whereby one count is added to each address during each display cycle. This test checks the computer portion of the CAT to determine whether the read-write memory cycle is operating properly. The VERT. RANGE switch (S3) should be in the TEST position. When the data ADD/SUB switch (S4) is in the ADD position the pattern displayed on the oscilloscope should uniformly move to the top of the screen and then reappear on the bottom again. The reverse happens when S4 is in the SUB position. This function is useful to move the baseline of a display on the CRT either upwards or downwards when the display appears "folded over."

S6 PLOT/PRINT Switch—The type of data readout may be selected with the PLOT/PRINT switch. In the PLOT position, an analog readout will be obtained. On Model CAT 400, the plotting speed of an X-Y plotter may be selected with S2 by lining up the red dot on the knob with a suitable plotting time of the outer red nomenclature. For Models CAT 400A and B see PLOT TIME control (R102) on rear panel. Plotting times are only approximate and represent the time in seconds required to plot all 400 addresses. In the PRINT position, readout will be via a digital device, such as the Model 500 Printer, the Model 530 IBM Typewriter, Models 540 or 551 Paper Tape Punch Units via the 520 Type-Punch-Read Control Unit.

S7 RESET Pushbutton—The entire memory is reset to zero by depressing the RESET button. Reset can take place only in the DISPLAY mode, thereby reducing the chance of accidental destruction of memory contents.

SL1 START Pushbutton—By depressing the START pushbutton the CAT is put into the accumulate (analysis) mode. An analysis sweep will either start at once or when an external trigger pulse is received depending on the position of S8. This mode cannot be changed by SL2, SL3, or SL4 before a full sweep is completed, i.e., any of these three pushbuttons have to be in the depressed state at the end of an analysis sweep to initiate a different mode.

SL2 DISPLAY Pushbutton—When the DISPLAY pushbutton is depressed, the information that has been stored in the memory is displayed on the CRT. The DISPLAY mode may be entered directly from either of the other three modes of operation.

SL3 READOUT Pushbutton—When the READOUT pushbutton is depressed, the instrument goes into a readout cycle. Readout will be either in analog or digital form depending upon the position of the PLOT/PRINT switch.

SL4 STOP Pushbutton—When the STOP pushbutton is depressed, any of the modes which have been initiated by the other three pushbuttons (SL1, SL2, or SL3) will be terminated. All data accumulated by the CAT memory are frozen or retained by the CAT.

2.2.2 REAR PANEL (See figure 2–3.)

S101 POWER ON/OFF Switch—The POWER switch applies ac power to the entire CAT. (Always turn OFF before removing covers.) The contents of the memory are not disturbed by removing the power from the CAT. When the unit is turned on again, previous contents will be displayed.

S103 PROGRAM Switch—The PROGRAM switch must be set to C for normal averaging operation or to obtain stimulus related time distributions using modulator by-pass cards. This control is not available on Model 400.

To obtain interval distributions the PROGRAM switch must be in the H position. A minimum pulse of plus 2.5 volts must be applied to connector J101 to automatically register one count in the particular address referenced at that moment, to reset the address to zero, and to start a new sweep after 50 microseconds. The pulse may be derived from external equipment.

With S103 set to D a minimum pulse of plus 2 volts applied to EXT. TRIG. (J107) will start a sweep. The sweep time is selected by the ANALYSIS TIME switch (S2). If S2 is in position EXT, the sweep time is determined by the frequency of an external pulse generator connected to the ADDR. ADV. connector (J103). A pulse applied to J101 stops the sweep, adds one count to the data contained in the address and resets the address to zero. A time of at least 50 microseconds must elapse before a new trigger pulse is applied to J107.

The D position is used for CAT amplitude and dwell time distributions. MNEMOTRON Model 606 Amplitude-to-Time Converter may be employed to furnish the proper signals including address advance pulses for amplitude analysis. Model 605 Amplitude Discriminator may be employed to furnish trigger and address reset pulses for dwell time analysis.

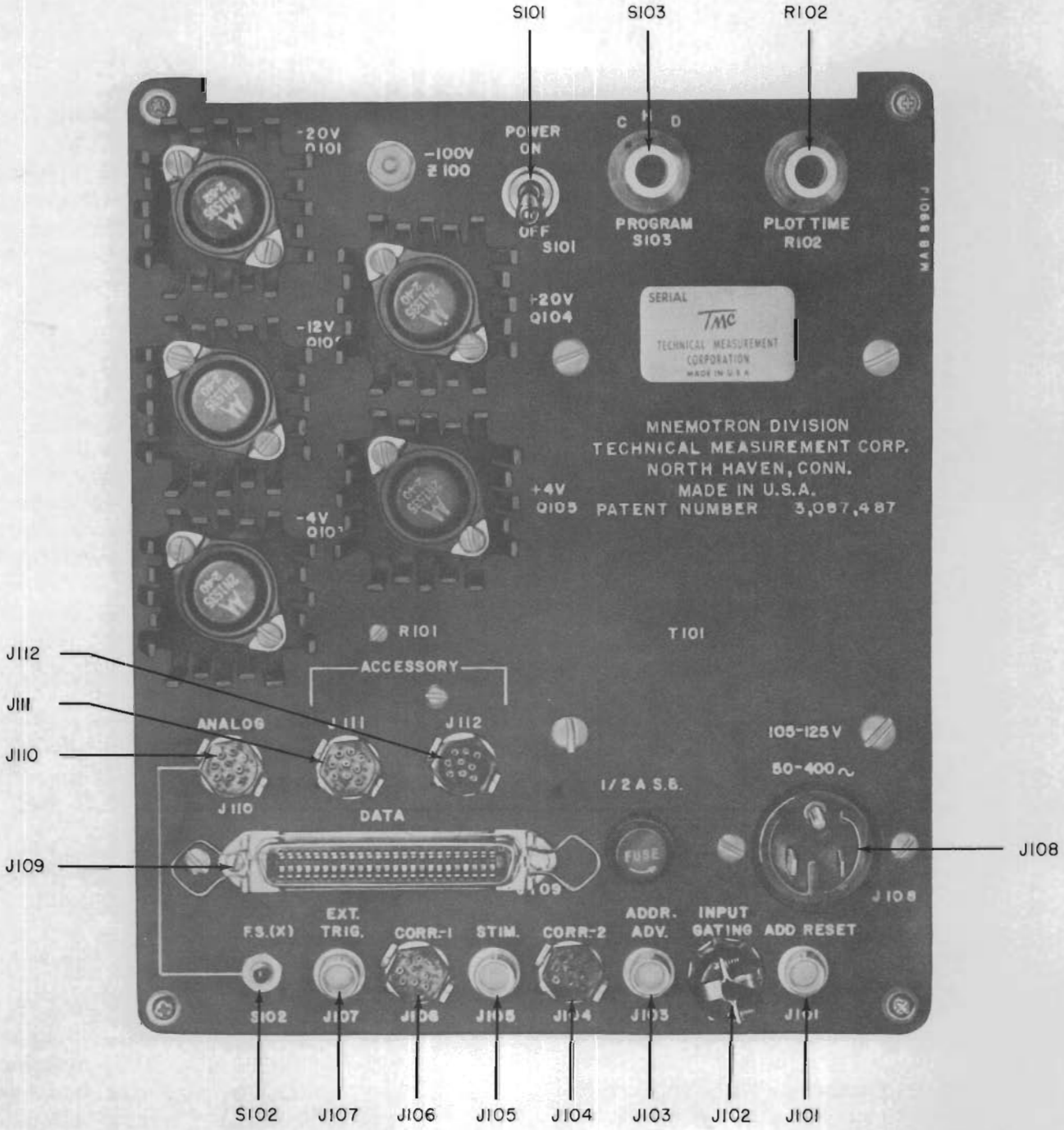


Figure 2–3. Computer of Average Transients, Model 400B, Rear View.

R102 PLOT TIME Control—The plotting speed of an X-Y plotter can be continuously adjusted by the PLOT TIME control from approximately 12 seconds to 120 seconds for 400 addresses. Provided only with Models 400A, 400B.

J110 ANALOG Connector—The ANALOG connector (J110) supplies analog voltages (0 to plus 100 millivolts) to operate either an X-Y Recorder or a Strip-Chart Recorder. (See table 2–5, J110, for pin connections.)

J111 J112 ACCESSORY Receptacles—J111 allows the CAT to be connected to an external control panel. Contacts for START, DISPLAY, READOUT, STOP and RESET functions are available. (See table 2–6, J111, for pin connections.)

J112 is provided for the connection of the Preset Sweep Counters, Models 562 and 592. (See table 2–7, J112, for pin connections.)

J109 DATA Connector—The DATA connector (J109) provides parallel BCD information for the readout devices that can be connected to the CAT, i.e., the Model 500 Paper Tape Printer, the Model 510 Typewriter Drive Unit, or the Model 520 Type-Punch-Read Control Unit. (See table 2–4, J109, for pin connections.)

1/2 A.S.B. FUSE—Slow-blo 1/2 ampere fuse to protect CAT from power overload.

J108 Male Plug Connector—Any ac line voltage between 105 and 125 volts at a frequency between 50 and 400 cps may be used to power the CAT. Power is applied at the male plug. Transformer connections may be changed to permit operation at 210 to 230 volts, 50 to 400 cps.

S102 F. S. (X) Pushbutton—The F. S. (X) pushbutton is used to calibrate an X-Y Recorder in the X direction. When pressed, a full scale voltage appears on the X terminal at J110 so that the recorder sensitivity can be adjusted to give full scale deflection.

J107 EXT. TRIG. Jack—A minimum plus 2 volt signal can be supplied to the EXT. TRIG jack (J107) to start an analysis sweep. The TRIGGER switch (S8) must be in the EXT. position. Input impedance is 6,000 ohms.

J106 Correlator No. 1 Connector—Connects the MNEMOTRON Model COR 256 Correlator to the CAT. (For pin connections see table 2–3, J106.) Provided only on Model 400B.

J105 STIM. Jack—A pulse is obtained from the STIM. jack (J105) which can be used to trigger stimulation equipment either directly or through suitable external equipment. The amplitude of this pulse is plus 15 volts and the duration is approximately 10 milliseconds on Models CAT 400 and 400A. On Model CAT 400B the amplitude is plus 50 volts and the duration is approximately 10 milliseconds. The pulse will appear either at the start of an analysis sweep or at the time when the sweep enters address 20, depending on the position of the STIMULUS switch (S9).

J104 Correlator No. 2 Connector—For connection of MNEMOTRON Model COR 256 Correlator. (See table 2–2, J104, for pin connections.)

J103 ADDR. ADV. Jack—The address may be advanced externally by supplying minimum plus 1 volt pulses to the ADDR. ADV. (J103) jack if analysis times other than those internally available are desired. The ANALYSIS TIME switch (S2) must be in the EXT. position. Each pulse advances the sweep by one address. The pulse frequency for a desired analysis time may be calculated from f=400/Ta where Ta is the analysis time in seconds. Input impedance is 50,000 ohms. Maximum pulse frequency is 20,000 pulses per second.

J102 INPUT GATING Connector—The INPUT GATING jack (J102) is provided for remote control of the modulator gates. To remotely enable an input gate, a ground potential must be provided to the proper pin. To turn the gate off remotely, a minus 12 volt potential must be provided to the same pin. (See table 2–1, J102, for pin connections.) This

connector also supplies an amplified X and Y analog output signal for slaving an external oscilloscope to the CAT. Provided on Model 400B only.

NOTE

A shorting plug, Amphenol 9-pin connector (126-220) must be inserted in J102 when the system is operated manually. It is supplied with the computer.

J101 ADDR. RESET Jack—A signal can be applied to the ADDR. RESET connector only when the PROGRAM switch (S103) is in the H or D position. A minimum pulse of plus 2.5 volts is required to operate the address reset circuitry. When the pulse is applied, the advance of the sweep will be stopped, one count will be deposited in the address just referenced and the sweep will be returned to address zero. The input impedance is 10,000 ohms. Not used on Model CAT 400.

2.3 PREPARATION FOR USE AND OPERATION

2.3.1 INTERCONNECTION PROCEDURES

Interconnection procedures for the Computer of Average Transients (CAT) are dependent upon specific applications. Section 6 outlines the uses of the CAT and their physical set-up. Tables 2–1 through 2–7 list the connections to all external equipment and are referenced in section 6. Paragraph 2.3.3 and figure 2–4 detail the mating of the CAT with the MNEMOTRON Series 600 CAT Accessories.

2.3.2 STARTING AND STOPPING PROCEDURE

To start the Computer of Average Transients, proceed as follows:

a. Connect CAT for particular application. Refer to the Applications Section 6 for use with ancillary equipment or paragraph 2.3.3 for use with MNEMOTRON Series 600 CAT Accessories.

b. Connect male plug (J108) to 105-125, 50-400 cps power source. (210-230 available on request.)

c. Position POWER switch (S101) at ON.

d. Depress DISPLAY pushbutton (SL2).

e. Depress RESET pushbutton (S7).

f. Depress START pushbutton (SL1) for CAT operation.

To stop CAT, depress STOP pushbutton (SL4) until operation ceases and position POWER switch (S101) at OFF.

NOTE

Before initiating a new mode of operation of the CAT, always press STOP pushbutton first, and then the pushbutton of the desired mode. To stop accumulation (START pushbutton lighted) press the STOP pushbutton and keep it in the depressed condition at the time of completion of the analysis sweep. The button may be pressed before the end of the sweep and held; however, the sweep will always be completed due to an internal interlock. Switching from one mode directly into the other may result in loss of information in some addresses.

TABLE 2–1 J102 REMOTE INPUT CONTROL AND SCOPE OUTPUT

(Not available on Models CAT 400, 400A, and 400H)

Pin Number	*Signal*	*Internal Connection*
A	INPUT No. 1 control	S11–1
B	INPUT No. 2 control	S12–1
C	INPUT No. 3 control	S13–1
D	INPUT No. 4 control	S14–1
E	–12 volt supply	PC22L–2
F	Ground	PC23L–4
H	Ground	
J	Y output for oscilloscope	PC11R–17
K	X output for oscilloscope	PC11R–38

NOTE

For manual control from front panel inputs switches S11 through S14, pins A, B, C, and D must be connected to ground pins F and H. A shorting plug (Amphenol 9 pin connector–126-220) is provided. For remote operation, pins A through D must be switched to minus 12 volts (pin E) individually when no signal accumulation is desired through that particular input and to ground (pins F and H) to turn on the corresponding input. Remove the shorting plug from J102 when operating in remote control mode. Pins J and K provide an amplified output of the Y and X signals for oscilloscope display.

2.3.3 CAT INTERCONNECTIONS WITH SERIES 600 CAT ACCESSORIES (See figure 2–4.)

To connect the Series 600 Accessories to the CAT, proceed as follows:

a. Attach BNC cable from ADDR RESET jack (J601) to CAT ADDR. RESET jack (J101). (Used only with Models 605 and 606.)

b. Attach BNC cable from EXT TRIG jack (J601) to CAT EXT TRIG. jack (J107). (Used only with Models 605 and 606.)

c. Attach BNC cable from EXT ADD. ADV. jack (J603) to CAT ADDR. ADV. jack (J103). (Used only with Model 606.)

d. Position Amphenol connector at TO CAT (J103), making certain properly marked connectors at the opposite end are mounted on CAT (ANALOG J110 and ACCESSORY J111, J112) positions.

e. Attach cable from TO CAT connector (J109A) to CAT DATA connector (J109).

f. Attach CAT power cable from CAT male plug (J108) to 600 cabinet convenience outlet (J101).

g. Attach Series 600 power cable from male plug (J102) to 105-125 vac, 50-400 cps power source. (210-230 available on request.)

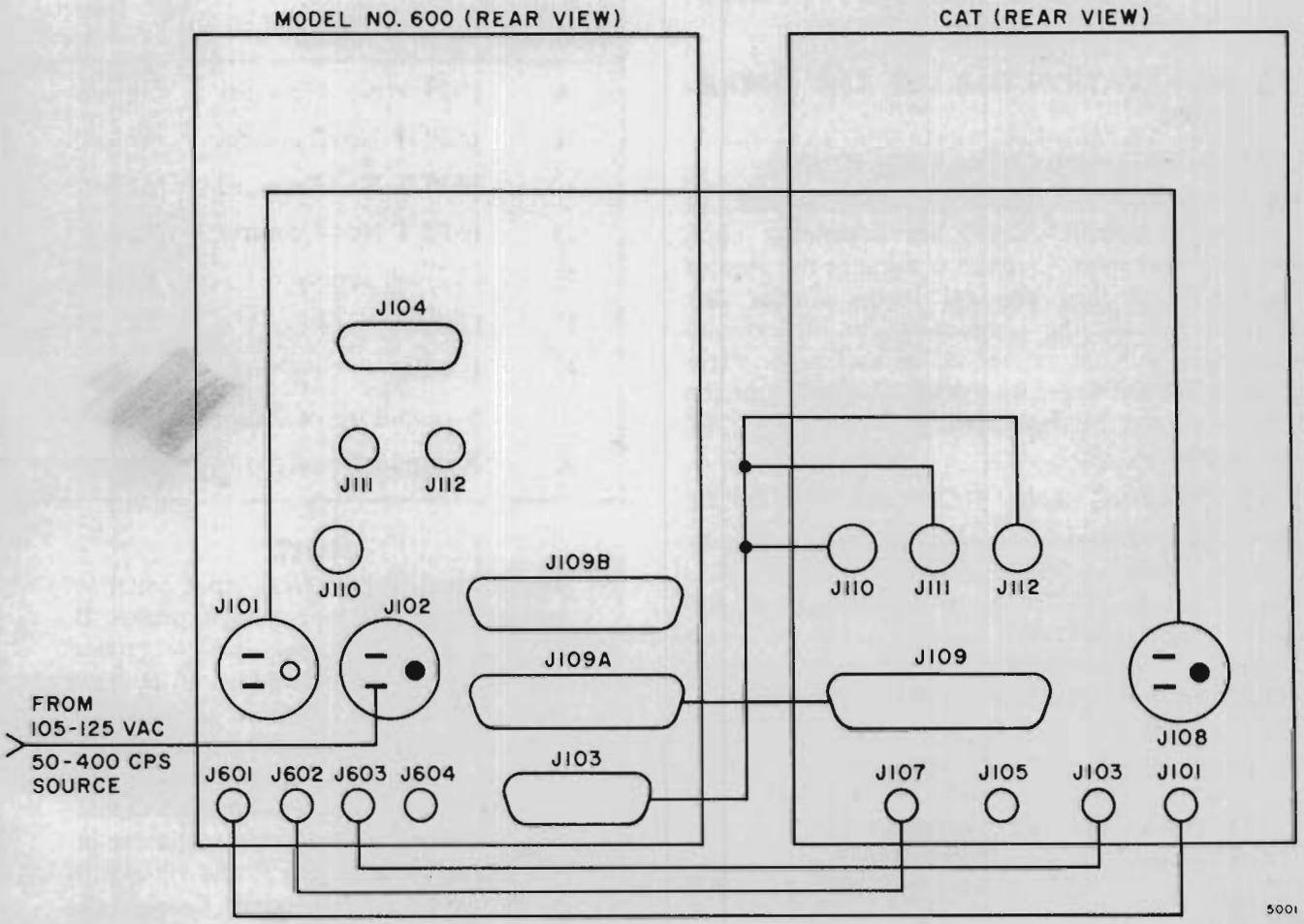


Figure 2–4. Series 600 Interconnection Diagram to CAT.

TABLE 2–2 J104 CORRELATION COMPUTER CONNECTOR (CORR–2)

(Not available on Models CAT 400, 400A, and 400H)

Pin Number	*Signal*	*Internal Connection*
A	MR (memory reset)	PC5R–14
B	Not used	
C	Not used	
D	Not used	
E	Not used	
F	Not used	
H	Not used	
J	Not used	
K	Not used	

NOTE

The MNEMOTRON Model COR 256 Correlation Computer is used in conjunction with the Model CAT 400B to form the Model CC–1 Correlation Computer System. This system provides on-line evaluation of the correlation functions.

TABLE 2–3 J106 CORRELATION COMPUTER CONNECTOR (CORR–1)

(Not available on Models CAT 400, 400A, and 400H)

Pin Number	*Signal*	*Internal Connection*
A	ADA 1 (Address Advance)	PC3R–12
B	AFF– (Accumulate Flip-Flop)	PC1R–17
C	ACPB (Accumulate Push-button)	PC1R–8
D	STPB (Start Pushbutton)	PC13R–20
E	SOC (Start of Conversion)	PC12L–19
F	ADD BUS	PC14R–33
H	SUB BUS	PC14R–31
J	IA1 (Inhibit Accumulate)	PC2R–26
K	RZ (Reset Zero)	PC23R–39

TABLE 2–4 J109 DATA CONNECTOR

Pin Number	*Signal*		*Internal Connection*
1	1	Data 10^0	PC26R–54
2	2		–55
3	4		–56
4	8		–57
5	1	Data 10^1	–58
6	2		–59
7	4		–60
8	8		–61
9	1	Data 10^2	–62
10	2		–63
11	4		–64
12	8		–65
13	1	Data 10^3	–66
14	2		–67
15	4		–68
16	8		–69
17	1	Data 10^4	–70
18	2		–71
19	4		–72
20	8		–73
21	1	Data 10^5	–74
22	2		–75
23	4		–76
24	8		–77
25	–100 volts		–78
26	1	Arithmetic Shift	–79
27	2		–80
28	4		–81
29	8		–82
30	Read Trigger (no filter)		PC2R–28
31			PC26R–84
32			–85
33			–86

Arithmetic Scaler

TABLE 2–4 J109 DATA CONNECTOR (CONT'D)

Pin Number	*Signal*		*Internal Connection*
34	1	Address Decade 10^0	PC26R–87
35	2		–88
36	4		–89
37	8		–90
38	1	Address Decade 10^1	–91
39	2		–92
40	4		–93
41	8		–94
42	1	Scale of 4	–95
43	2		–96
44			–97
45			–98
46	Print Trigger		–99
47	Address Advance		PC5R–9
48	Shift Trigger		PC13R–16
49	Write-in Trigger		PC2R–25
50	Chassis Ground		PC26–108

TABLE 2–5 J110 ANALOG CONNECTOR

Pin Number	*Signal*	*Internal Connection*
A	Recorder ground X terminal (RXG)	PC11R–30
B	Recorder X signal (RX+) + 100 mv.	PC11R–31
C	Recorder ground Y terminal (RYG)	PC11R–14
D	Recorder Y signal (RY+) + 100 mv.	PC11R–13
E	Ground. This is to be connected to the frame of the X-Y plotter. X and Y servo amplifier should be floating.	PC26–110
F	NDR (Null Detector Rush)	PC26R–106
H	RFF+ (high level) (Readout flip-flop)	PC26R–104
J	–26 volts (unregulated)	PC20L–8
K	Not used	

TABLE 2–6 J111 REMOTE CONTROL ACCESSORY CONNECTOR

Pin Number	*Signal*	*Internal Connection*
A	External STOP control (switch to ground)	PC1R–18
B	External READOUT control (switch to ground)	PC1R–30
C	Not used	
D	External DISPLAY control (switch to ground)	PC1R–20
E	Ground	PC23L–5
F	External START control (switch to ground)	PC1R–8
H	+4 volt supply	PC23L–6
J	Memory reset (switch to ground)	PC5R–14
K	DFF—(Display flip-flop)	PC1R–27

NOTE

Whereas it is only necessary to make contact to ground temporarily to initiate STOP, READOUT, DISPLAY, or START (accumulate) modes, it is required to connect pin J to ground for a minimum duration of 70 milliseconds to clear (reset) the memory. This must be done only in the DISPLAY mode of operation.

TABLE 2–7 J112 ACCESSORY CONNECTOR FOR SWEEP COUNTER MODEL 562

Pin Number	*Signal*	*Internal Connection*
A	Stop	PC1R–8
B	Not used	
C	Ordinate 20	PC11L–10
D	+20 volt supply	PC23L–7
E	Ground	PC23L–5
F	AFF+ (Accumulate flip-flop)	PC12L–20
H	+4 volt supply	PC23L–6
J	–4 volt supply	PC23L–3
K	–26 volt supply	PC20L–8

2.4 CHECKOUT PROCEDURES

2.4.1 GENERAL

Checkout procedures for the Computer of Average Transients (CAT) are detailed in paragraphs indicated in the following table:

Description	*Paragraph*
Computer	2.4.2
Modulator	2.4.3
Stimulus Pulse	2.4.4
Pre Analysis Delay	2.4.5
Readout Equipment	2.4.6
Printer	2.4.7
Typewriter and Tape Punch	2.4.8

Procedures determining the operational parameters of the CAT are vital to its successful use. All instruments are checked by the manufacturer, but subsequent handling may dictate the advisability of performing checkout procedures. When such procedures are performed, follow the steps as outlined in the sequence outlined. When equivalent equipment is used, make certain the signals are identical to those set out in the applicable paragraphs. Units which do not perform adequately after careful checkout analysis should be returned to the manufacturer for service.

2.4.2 COMPUTER SECTION

To check out the computer section of the CAT, proceed as follows:

a. Set the CAT controls as follows:
   1) ADD/SUB switch (S4) to ADD.
   2) TEST/USE switch (S5) to USE.
   3) INPUTS IN USE switch (S1) at 1.
   4) VERT. SIZE control (R5) full clockwise.
   5) POWER switch to ON.

b. Note that the light in the STOP (SL4) button is on.

c. Press the DISPLAY (SL2) button. A line or pattern of dots will be displayed on the face of the cathode ray tube. If no line appears, check the cathode ray tube controls (INTENSITY, HORIZ. POS. and VERT. POS.).

d. With the display of dots visible, press the RESET (S7) button to clear any stored information. A straight horizontal line will appear on the screen.

e. Position the line to coincide with the bottom graticule of the CRT face. This may be done by means of the HORIZ. POS. control, VERT. POS. control 1 and HORIZ. SIZE control.

f. Set the VERT. RANGE (S3) switch to TEST (10^2 position on Models CAT 400, 400H).

g. Set the TEST/USE (S6) switch to TEST. The line will move upwards and upon reaching the top line of the graticule, jump down to the bottom line to again start its upward movement.

h. Set the ADD/SUB switch (S4) to SUB. The line will move uniformly downward and jump to the top of the graticule after reaching the bottom line and then resume the downward movement.

NOTE

A small step may appear in the line when the TEST/USE switch is set to TEST. This is normal and only indicates the position of the beam at the time the TEST/USE switch was operated. A new step will appear each time the ADD/SUB switch is operated during the checkout program.

i. Return the TEST/USE switch to USE. The line will now remain stationary.

j. Return the ADD/SUB switch to ADD.

k. Press the RESET button (S7).

l. Set the INPUTS IN USE switch (S1) at 2. Two traces will now appear on the left half of the screen. They may be extended across the full width of the screen by means of the HORIZ. SIZE control.

m. Set the INPUTS IN USE switch at 4. Four traces will now appear on the left half of the screen. They may also be expanded.

n. Set the INPUTS IN USE switch at 1. Note the following:

1) The trace can be moved vertically by VERT. POS. control 1.

2) The trace can be expanded fully horizontally by means of the HORIZ. SIZE control (full clockwise). Any part of the recorded signal can be viewed in more detail.

3) The trace can be positioned horizontally by the HORIZ. POS. control.

o. Set the INPUTS IN USE switch to 2. Note the following:

1) The trace which records the signal connected to INPUT 1 is positioned vertically by VERT. POS. control 1.

2) The trace which records the signal connected to INPUT 2 is positioned vertically by VERT. POS. control 3.

3) Both traces can be expanded simultaneously and any part of them can be positioned on the screen.

p. Set the INPUTS IN USE switch to 4. Note the following:

1) Each of the VERT. POS. controls positions vertically that trace which receives the signal information from the input carrying the same number.

2) The HORIZ. SIZE control expands the four traces simultaneously.

3) The HORIZ. POS. control positions the four traces simultaneously.

2.4.3 MODULATOR SECTION

To check out the modulator section of the CAT, proceed as follows:

a. Set the Models 400A and 400B controls as follows:

1) INPUT switches 1, 2, 3, and 4 (S11, S12, S13, S14) at ON. (Not on CAT 400 and 400H.)

2) INPUTS IN USE switch (S1) to 4.

3) TRIGGER (S8) switch to INT.

4) ANALYSIS TIME (S2) switch to 2 sec.

5) VERT. RANGE (S3) switch to 10^4.

6) On models 400A, 400B, and 400H set PROGRAM (S103) switch at C.

b. Press the START (SL1) button. If a 100 kilocycle modulator is used, four lines approximately one-eighth of an inch high will move across the screen.

If a 250 kilocycle modulator is used, four lines approximately one-fourth of an inch high will move across the screen.

A new sweep will be started as soon as the previous sweep is completed. Each successive sweep will be a little higher with the ADD/SUB switch in the ADD position and a little lower with the ADD/SUB switch in the SUB position.

c. Turn the INPUTS switches (S11, S12, S13, and S14) at OFF individually. Note that the height of the corresponding trace will be considerably reduced and that the trace will not move in a vertical direction but remains stationary while other traces continue to move up or down depending on the position of the ADD/SUB switch.

NOTE

The input switches are not supplied with the Models 400, 400H.

2.4.4 STIMULUS PULSE OPERATION

To check out the stimulus pulse operation, proceed as follows:

a. Connect a Tektronix Model 502 Oscilloscope or equivalent to J105 on the rear panel of the CAT.

b. Set the oscilloscope controls as follows:

1) HORIZ. SWEEP to 5 msec./cm.

2) VERT. SENSITIVITY to 20 volts/cm for Model 400B, 5 volts/cm for other models.

3) TRIGGER to +INT. AC.

c. At the CAT, set the STIM. switch (S9) to the PROMPT position.

d. Press the START button. A pulse of approximately 15 volts amplitude (50 volts on Model 400B) and a duration of 10 to 15 milliseconds will be observed on the external oscilloscope each time a new sweep starts.

e. Set the STIM. switch (S9) to the ORD. 20 position. A pulse will now appear when the sweep enters address 20.

2.4.5 PRE ANALYSIS DELAY OPERATION

To check out the pre analysis delay operation, proceed as follows:

a. Set the CAT controls as follows:

1) INPUTS IN USE switch at 4.

2) ANALYSIS TIME switch at 2.

3) VERT. RANGE switch at 10^4.

4) TEST/USE switch to USE.

b. Press START button.

c. Gradually turn the PRE ANALYSIS DELAY switch clockwise and note that the delay between the end of one sweep and the beginning of the next increases. At full clockwise rotation of the PRE ANALYSIS DELAY switch, the delay will be approximately 10 seconds.

2.4.6 READOUT EQUIPMENT OPERATION

2.4.6.1 X-Y Plotter

To check out X-Y plotter operation, proceed as follows:

An analog readout cable is provided with all Model 400 Series Units.

a. Connect cable from J110 to X-Y plotter as follows:

1) Insert the 9-pin miniature connector (Amphenol type 126-220) to J110 on the rear panel of the CAT.

2) Connect the open ends of the cable to the X-Y plotter as directed on the attached label, and table 2–5.

b. Set the INPUTS IN USE switch (S1) to 1.

NOTE

On the Models 400, 400H set the red dot on the ANALYSIS TIME switch to red number 40. On the Models 400A and 400B turn the PLOT TIME control on the rear panel to a mid position.

c. Set the ADD/SUB switch to ADD.

d. Depress the DISPLAY button and wait for trace to appear. Quickly flick the TEST/USE switch back and forth once.

e. Set the ADD/SUB switch to SUB.

f. Quickly flick the TEST/USE switch back and forth once. Part of the trace will now appear at the bottom of the screen and part at the top. Repeat steps e, g, and h if necessary until these results are obtained.

g. Set the PLOT/PRINT switch (S6) to the PRINT position (with all digital readout equipment disconnected).

h. Push the READOUT button (SL3). (This starts the address readout at the first address.) Then push STOP button (SL4).

i. Set the PLOT/PRINT switch to PLOT.

j. Turn on the power to the X-Y plotter. Allow a few minutes for warm up time.

k. Set the X-Y plotter sensitivity to approximately 100 mv full scale.

l. Turn the servo motor of the X-Y plotter on.

m. Adjust the centering controls of the plotter so that the pen is at the extreme left hand side of the paper and adjusted vertically so that the plot will be centered vertically on the paper.

n. Press FS(X) button on CAT rear panel. Adjust variable X gain of recorder to the desired full deflection of pen.

o. Push the READOUT button (SL3). The X-Y plotter as well as the dot on the screen of the CAT will move forward at the rate of approximately 10 addresses per second and follow the pattern previously described (step h) in the display mode.

p. After one scan through all 400 addresses the CAT will stop automatically.

NOTE

If a strip-chart recorder (EEG recorder) is used for plotting, select a suitable plotting speed for a desired paper length by moving the red dot on the ANALYSIS TIME knob to the 16, 4, or 0.8 seconds for Models 400 and 400H. Adjust the speed by means of PLOT TIME control on the rear panel of 400A and 400B. The range covered by the PLOT TIME control is approximately 12 to 120 seconds for plotting of 400 addresses. To plot with a strip-chart recorder only the leads marked Y (+) and Y (−) GND are connected to the recorder. The ground lead provided should always be connected to chassis ground of the recorder. The plotting function of the computer may also be tested without the analog cable and a recorder connected. The procedure is the same as outlined above. The dot will move across the screen at the selected speed.

2.4.6.2 Printer

To check out printer operation, proceed as follows:

a. Connect the power cables to the Model 500 Printer.

b. Connect the data cable to J109 at the rear panel of the CAT and corresponding end to the printer.

c. Start both the CAT and printer.

d. Set the CAT ADD/SUB switch to ADD and TEST/USE switch to TEST.

e. Press the DISPLAY button. Allow data to accumulate for several seconds. Press the STOP button.

f. Set the PRINT/PLOT switch to PRINT.

g. Set the TEST/USE switch to USE. Press the READOUT button. The printer will print fairly low numbers. At the end of readout, press the DISPLAY button. Clear the memory by pressing the RESET button.

h. Set the ADD/SUB switch to SUB.

i. Set the TEST/USE switch to TEST and allow data to subtract for a few seconds. Press the STOP button.

j. Set the TEST/USE switch to USE.

k. Push the READOUT button. The printer will print large numbers.

2.4.6.3 Typewriter and Tape Punch

To check out typewriter and tape punch operation, proceed as follows:

NOTE

When using typewriter and tape punch instruments, a Shift Logic Card (8511) must be inserted in slot 13R on right hand side of CAT. Refer to Instruction Manual which accompanies unit.

a. Connect the power cables of the Units to be used.

1) Model 510 Typewriter Drive Unit

2) Model 512 Type-Punch Control Unit

3) Model 520 Type-Punch-Read Control Unit

4) Model 530 IBM Computer Typewriter

b. Connect the data cable to J109 on the rear panel of the CAT and to the corresponding connector of the control unit used.

c. Connect the typewriter data cable to the mating connector on the rear panel of the control unit.

d. Energize the ac power to all units. Press the DISPLAY pushbutton and repeat the procedure used in the printer checkout.

e. Follow the same steps for Model 540 Tape Punch as for the typewriter.

NOTE

After the applicable tests are performed successfully, the computer and readout equipment are in good working order. In case of doubtful results of one check or another or a definite malfunction, contact your MNEMOTRON representative or the service department at MNEMOTRON DIVISION of Technical Measurement Corporation, 441 Washington Avenue, North Haven, Connecticut. In case of a malfunction, complete one of the Malfunction Charts supplied in the rear of this Manual. Refer to section 4 for complete service instructions.

SECTION III
THEORY OF OPERATION

3.0 GENERAL

Section 3 outlines the theory of operation for the Computer of Average Transients (CAT). Paragraph 3.1 Block Diagram Discussion utilizes the CAT Block Diagram, figure 3–1 and paragraph 3.4 utilizes the Circuit Diagrams included in Section VII of this publication.

The CAT consists of an Input Section and a Computer Section. While CAT operation depends on signals from both sections, theory discussions will be separated into the two broad categories. Where one section is directly related to the other, specific reference will be made in the text.

3.1 BLOCK DIAGRAM DISCUSSION

3.1.1 INPUT SECTION (See figure 3–1.)

Input signals are connected to the INPUTS connectors (J1 through J4) depending on the number of signals to be processed. These are analog signals which are fed directly to the Modulators 8897 (PC3L through PC6L). The Modulators, pulse oscillators of either 50, 100, 250, or 500 thousand pulses per second, are sensitive to voltage changes from the input signals. The change in pulse frequency is a linear function of the concurrent changes in analog input voltage. These pulses are transmitted to the applicable circuits in the Modulator Gates Circuit 8894 (PC9L) associated with each of the four Modulators.

Modulator By-Pass Cards, 8898, are provided as options when the input signals are in pulse form, requiring no frequency modulation.

The Modulator Gates pass the pulses to the Arithmetic Decades in the Computer Section for accumulation. Depending on the position of the INPUTS IN USE switch (S1), gating signals from the Modulator Gate Control Circuit 8895 (PC8L) enable the individual gates to pass the modulator pulses. Signals (CFF+) from the Delay Control Flip-Flop Circuit 8890 (PC13L) assure that pulses to the Arithmetic Decades occur only during an analysis sweep. Memory busy signals (MB) from the Auto Data Transfer Circuit in the Computer Section prevent signal processing during the memory cycle. When the Delay Control Flip-Flop signal (CFF+) is negative at the end of an analysis sweep, the Modulator Gates (PC9L) are disabled and no signals can be transmitted to the Computer Section. This also occurs when the memory busy signal (MB) is negative during the CAT memory cycle.

The INPUTS IN USE switch (S1) selects the number of inputs which will be operative. The switch position determines which of the signals from the Modulator Gate Control Circuit (PC8L) operate the Modulator Gates (PC9L). Those input positions which are not used remain closed.

Within the Input Section, the Delay Control Flip-Flop Circuit (PC13L) and the Modulator Gate Control Circuit (PC8L) affect the operation of the Modulator Gates (PC9L). The CFF signals indicate that the CAT is in the accumulate mode of operation, and that a 400 address sweep is in progress. When the TRIG. switch (S8) is at the INT. position the Delay Control Flip-Flop Circuit (PC13L) receives a negative pulse from the Trigger Generator Circuit 8899 (PC10L) to start each sweep. At the EXT. position of the TRIG. switch (S8), external pulses start each sweep and allow the Delay Control Flip-Flop Circuit (PC13L) to enable the Modulator Gates and associated operations.

For internal trigger operation, the Trigger Generator Circuit (PC10L) receives a positive accumulate flip-flop signal (AFF+) from the Control Logic Circuit in the Computer Section to start the first sweep. This occurs 100 microseconds after the START pushbutton (SL1) is depressed. At the end of the sweep, the address overflow signal (AOF) is provided. This signal automatically starts the next sweep 100 microseconds later for the resumption of CAT operation. The AOF signal comes from the Scale of Four/Memory Location Circuit in the Computer Section.

A delay time between each trigger pulse and the start of the sweep can be varied by the use of the PRE ANALYSIS DELAY Control (S10) which affects the Delay Control Flip-Flop Circuit (PC13L) output operation.

The Modulator Gate Control Circuit (PC8L) provides signals to the Modulator Gates (PC9L). As stated, these signals only enable those gates selected by the INPUTS IN USE switch (S1).

Modulator Gate Control (PC8L) operation is dependent upon the INPUTS IN USE switch (S1) and the ANALYSIS TIME switch (S2).

The 51.2 KC Oscillator and Shaper Circuit 8888–2 (PC17L) only provides frequency signals when the CAT is in an analysis sweep. The circuit must be enabled by a (CFF) signal to indicate this state. When no sweep is in progress, CFF being negative inhibits circuit operation, and oscillation cannot occur.

The output of the 51.2 KC Oscillator and Shaper Circuit (PC17L) results in pulses which are fed into the first Scale of 16 Circuits 8889 (PC16L). Each binary circuit on the Scale of 16 divides the initial oscillation frequency by successive steps of two. The appropriate timing pulses are selected by the ANALYSIS TIME switch (S2). Sweep time of 0.03125, 0.06250, 0.125 seconds are available from the first Scale of 16 (PC16L). Sweep times of 0.25, 0.5, 1, 2 seconds are available from the second Scale of 16 (PC15L). Sweep times of 4, 8, 16 seconds are available from the third Scale of 16 (PC14L).

NOTE

CAT Models 400, 400H, 400A have sweep times of 0.06250 to 32 seconds.

Outputs from the Scale of 16, plus a connection which provides for the inclusion of external sweep times, complete the positions of the ANALYSIS TIME switch (S2). These positions carry the applicable timing pulses to the Modulator Gate Control Circuit (PC8L) and initiate memory cycles at the appropriate times.

The external connection utilizes pulses for memory address advance through ADDR. ADV. jack (J103) when the ANALYSIS TIME switch (S2) is at the EXT. position. Each pulse advances the address one count. The sweep duration, therefore, is determined by the repetition rate of these external pulses. An external reset pulse can also be provided to reset the memory address. The reset pulse is directed through the ADDR. RESET jack (J101) and is transmitted to the External Address Control Circuit 8998 (PC12L). This feature is only available at the D and H position of the PROGRAM switch (S103).

An additional function of the CAT is the Stimulus Pulse Generator Circuit 8892–2 (PC11L) which provides a plus 50 volt pulse for triggering external equipment. This is available at the STIM. jack (J105) and can occur at the start of analysis sweep or at the 20th address depending on the position of the STIMULUS switch (S9).

NOTE

CAT Models 400, 400A, 400H provide plus 15 volts for triggering external equipment.

3.1.2 COMPUTER SECTION (See figure 3–1.)

Command signals from the front panel pushbuttons, START (SL1), DISPLAY (SL2), READOUT (SL3), STOP (SL4) are received by the Control Logic Circuit 8500 (PC1R) and transmit the appropriate mode program to the associated circuits in the CAT. These program mode commands, when transmitted to the Auto Data Transfer Circuit 8501 (PC2R) initiate the memory timing cycle as indicated in drawing No. WFB8974. The Read Cycle Generator Circuit 8502 (PC3R) also receives the program mode commands and generates signals which provide the READ busy signal as indicated in drawing Nos. WFB8442, WFB8445, WFB8974. This circuit senses the particular address from the magnetic core memory and reads it into the arithmetic register. (Refer to paragraph 3.4.2.7.) The arithmetic register consists of two Second Address Decade Circuits 8507 (PC6R, PC8R), two 4 X 5 Memory Decoder Circuits 8506 (PC7R, PC9R), and the Scale of Four/Memory Location Circuit 8505 (PC10R). The Write Cycle Generator Circuit 8504 (PC5R) provides the WRITE busy signal for memory timing as indicated on drawing Nos. WFB8442, WFB8445, WFB8974. The Memory Current Generator Circuit 8503 (PC4R) supplies the READ and WRITE currents (410 ma) for operation of the magnetic core memory. (Refer to paragraph 3.4.2.7.)

The 1st and 2nd Second Address Decade Circuits 8507 (PC6R, PC8R) constitute that portion of the Computer Section address register which provides output signals combined with the 4 X 5 Memory Decoder Circuits 8506 (PC7R, PC9R) to select the memory storage location in the CAT memory. On receiving the 10th input pulse, the 1st Second Address Decade Circuit (PC6R) generates a carry

pulse which produces one count in the 2nd Second Address Decade (PC8R). These circuits also provide outputs to drive the X deflection plates of the CRT via the Digital-to-Analog Converter and Deflection Amplifier Circuit 8509 (PC11R). The 4 X 5 Memory Decoder Circuits (PC7R, PC9R) consist of logic matrices which produce signals to direct READ and WRITE currents (approximately 400 ma each) for the selection of memory address coordinates. The Scale of Four/Memory Location Circuit 8508 (PC10R) is the last unit of the address register. This circuit, besides being incorporated in the address register, also provides circuitry to select the memory subgroups as determined by the INPUTS IN USE switch (S1) positions.

The Arithmetic Decade Circuits 8512 (PC14R, PC16R, PC18R, PC20R, PC22R, PC24R) receive the signal pulses from the Input Section. These signals which are supplied to the Arithmetic Decade Circuits are added to or subtracted from the data already existing in the memory cores. (Refer to paragraph 3.4.2.7.) The data from the memory cores are SENSED by the Sense and Inhibit Amplifier Circuits 8513 (PC15R, PC17R, PC19R, PC21R, PC23R, PC25R) and transferred to the corresponding Arithmetic Decade Circuits. The incoming pulses from the Modulator Gates Circuits in the Input Section are then added to the data contained in the arithmetic scaler. The arithmetic scaler consists of the Arithmetic Decades plus their companion Sense and Inhibit Amplifier Circuits. Outputs to the Digital-to-Analog Converter and Deflection Circuit (PC11R) from the arithmetic scaler are provided to drive the Y deflection plates of the CRT.

The output of the Digital-to-Analog Converter and Deflection Amplifier Circuit (PC11R) drives the X and Y CRT deflection plates as well as supplying X and Y output signals to plotter equipment.

The Selective Centering Circuit 8887 (PC12R) provides vertical control of the CRT traces through the operation of the VERT. POS. control (R1 through R4) on the CAT front panel.

A filter Circuit Board 8833 (PC26R) is provided to reduce noise transients to Computer Section circuit boards from external accessory equipment.

The Shift Logic Circuit 8511 (PC13R) used only during the readout mode of operation causes the data in the Arithmetic Decade Circuits to advance from the lower decades to succeeding higher decades. This circuit is used in conjunction with the arithmetic scaler. This circuit is only supplied when readout is performed through one of the readout control units (Model 510 or 520).

3.2 USE OF CIRCUIT DIAGRAMS

Circuit Diagrams in Section VII accompany each CAT Instruction Manual. They consist of all the schematic diagrams as well as waveforms and an Interconnection Board Key for the right and left side of the CAT.

Since the CAT is composed of individual plug-in printed circuit cards, all pin connections are similar and contain similar numbers from card to card. The cards on the left side of the CAT have 20 pins and make up the Input Section while the cards on the right side have 40 pins and make up the Computer Section.

Each pin as it appears on the plug-in card is detailed on the Interconnection Board Key. Therefore, the pin number indicating a given signal on any schematic will appear as that number on the Key. Signals printed on the schematic will be repeated at the identical location shown on the Key.

The Interconnection Board Key ties similar signals from card to card and side to side. It also indicates additional connections such as switches and controls. For example: All the plus 4 volt connections appear at pin 6 and are tied internally to each pin 6 on every card.

The AOF signal (overflow pulse) appears at the right hand (Computer Section) plug-in card PC3R pin 39 through PC5R pin 35, PC4R pin 33, PC2R pin 29, PC1R pin 29 and out to the left hand (Input Section) plug-in card PC10L pin 9. The pin connections on each of the schematics for these cards reflect the identical pin numbers indicated in the Key. On the left hand Interconnection Key at PC10L pin 9, the AOF signal can be traced through the Input Section at pin 9 for cards PC11L, PC12L, and PC13L.

One need only locate a given signal on a particular card with an applicable pin number to trace the application of that signal throughout the unit. All circuit diagrams of printed circuit cards carry the same nomenclature and number which appears on the card itself. The circuit diagrams also contain the slot number and side which the card occupies in the CAT. Text references detail both the position in the unit and the schematic number.

3.3 INTRODUCTION TO THEORY OF OPERATION

Digital circuits are composed of a number of individual building blocks. These building blocks reoccur in one or another variation depending on the purpose they have to serve. To facilitate the

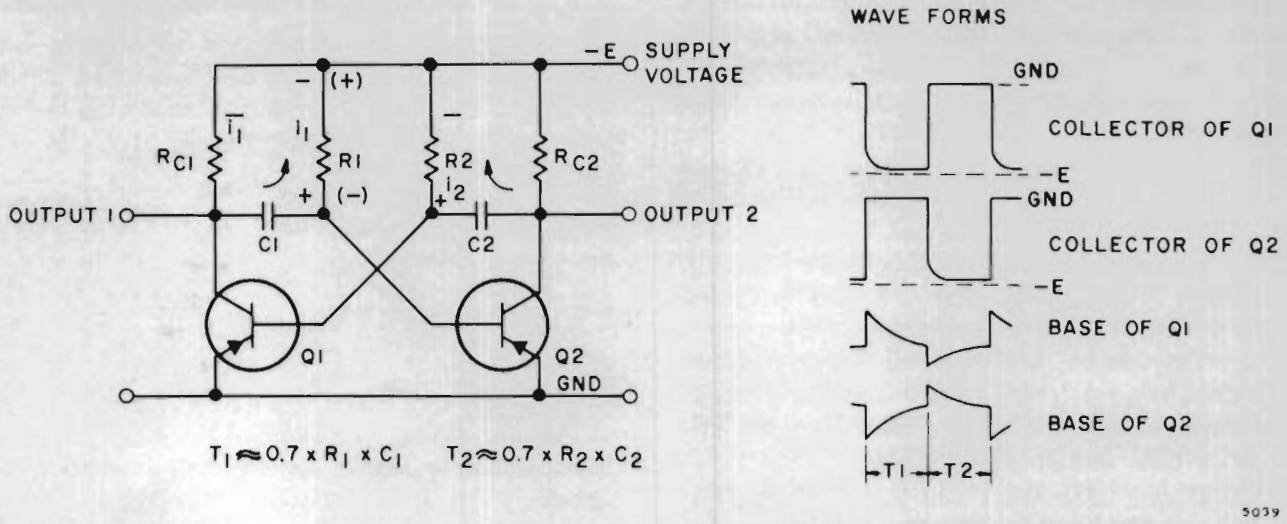


Figure 3–2. Free Running (Astable) Multivibrator, Circuit and Waveform Diagram.

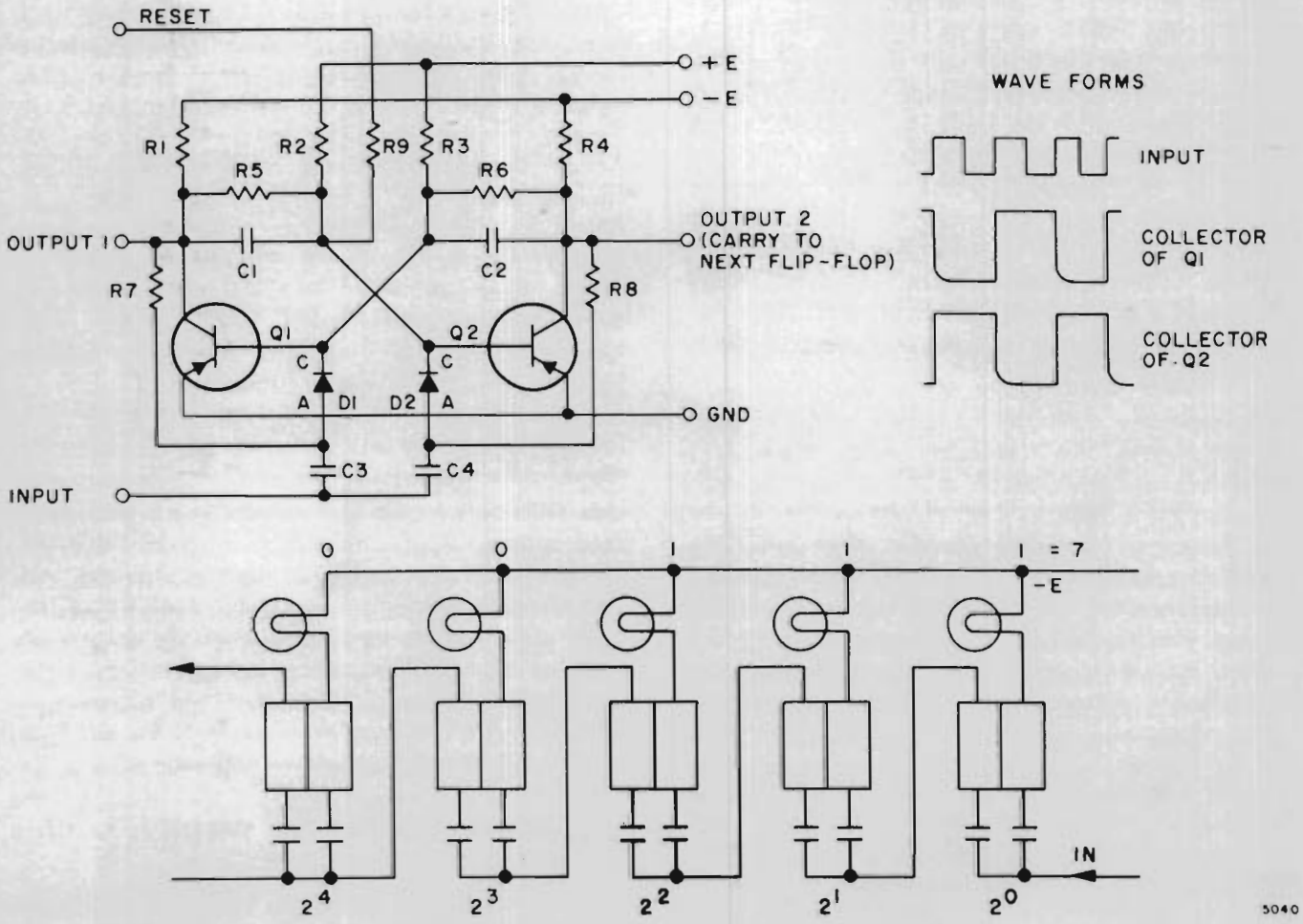


Figure 3–3. Bistable Multivibrator (Flip-Flop), Circuit and Waveform Diagram.

circuit description a few of the basic circuits will be discussed. The transistors used in the illustrations are of the PNP type. The circuits apply also for NPN transistors if the polarity of the supply voltages is reversed.

3.3.1 THE FREE RUNNING MULTIVIBRATOR CIRCUIT (See figure 3–2.)

In digital applications this circuit is generally used to provide timing signals. When the supply voltage is applied, one of the two transistors turns on first due to differences in their characteristics. Assuming transistor Q1 has turned on first, the collector of Q1 assumes ground potential causing a charging current i_1 in the indicated direction. This current produces a voltage drop across R1, which causes a positive voltage at the base of transistor Q2 and thus holds Q2 off until C_1 discharges and the voltage reaches a low enough value so that Q2 can no longer be held off. As Q2 starts to conduct, its collector now assumes ground potential producing a charging current i_2 in the indicated direction and thereby turning off Q1. The collector of Q1, therefore, reaches the supply voltage −E and capacitor C_1 now discharges through R_{c1} and R1. The discharge current i_1 produces a voltage drop across R1 as designated by polarity signs in parenthesis. This discharge current keeps Q2 on. As i_1 maintained Q2 in the off state i_2 now holds Q1 off until it drops so low that Q1 starts to conduct again starting another cycle. The cycles continue until the supply voltage is no longer applied. The output is transmitted from the collector of either transistor.

3.3.2 THE BISTABLE MULTIVIBRATOR (FLIP-FLOP) (See figure 3–3.)

This circuit is used for counting and frequency dividing. Since it is uncertain which transistor is in the on state when power is turned on, a negative reset signal is applied through R9 to the base of Q2 forcing this transistor on. The reset signal is a pulse long enough to reset all flip-flops connected to it. After that, the signal line is returned to the emitter potential, in this case, ground. The flip-flop is now ready to receive input signals. Since Q2 was turned on by the reset pulse, its collector is at emitter (ground) potential. Transistor Q1 is, therefore, held off by R3 which is returned to +E (positive with respect to ground). The collector of Q1 is at the negative supply potential. The base of Q2 is connected through R5 to the collector of Q1 and hence to −E which keeps Q2 in the on state.

Resistors R7 and R8 are called the steering resistors. The purpose of these resistors is to route the input signal to the base of the transistor which is on. This is accomplished with the help of diodes D1 and D2. The collector of Q2 is at ground potential and since base and emitter are always at nearly the same potential, particularly when a transistor is conducting, both sides of diode D2 are at the same potential. The collector potential of Q2 is applied to the anode end A of diode D2 through resistor R8. This diode is thus enabled to pass positive pulses.

The cathode C of diode D1 is connected to the base of Q1 and is, therefore, at approximately ground potential. As stated, the collector of Q2 is at the negative supply potential −E since Q2 is off. This potential applied through R7 to the anode A of D1. A negative potential applied to the anode, however, back biases the diode and prevents it from conducting.

Hence the positive spike derived by differentiating action of capacitors C3 and C4 of the positive going portion of the input square wave shown in figure 3–3 can only reach the base of Q2, turning this transistor off. This causes the collector of Q2 to assume the potential −E; an action which in turn causes transistor Q1 to turn on because its base is connected through R6 to the now negative collector of Q2. The circuit is now in its opposite stable state. The next positive pulse is then automatically routed through the gating action of D1 and D2 to the base of Q1, turning this transistor off and thus bringing the circuit back into its original state. Two periods of the input signal are, therefore, required to achieve one complete period of the output signal and thus a frequency division by two is accomplished. The output of this flip-flop may now be connected to the input of another flip-flop to effect a further frequency division of two, a total of four. Each additional flip-flop divides by two again. This results in a two-four-eight-sixteen, etc. sequence of the division of the original frequency measured on the collector of each successive stage.

The flip-flop may also be used as a counter. Initially all flip-flops are reset to their "0" state (Q2 turned on). If one imagines R1 replaced by a light bulb in each flip-flop then all bulbs will be off in the reset state of the flip-flops indicating zero counts. The first count to arrive at the input of the first flip-flop turns off Q2. Transistor Q1 is turned on and lamp No. 1 lights indicating that one count was received. Since Q2 was turned off, its collector went negative and, therefore, did not create a carry (input) signal for the following flip-flop, the input of which is connected to the collector of Q2.

The second pulse turns off Q1 and Q2 is turned on. The light bulb in the collector circuit of Q1 is extinguished and since the collector potential of Q2

changes in a positive direction (from −E to GND) a carry pulse for the second flip-flop is generated. This turns Q2 in that flip-flop off and thus, by turning its Q1 transistor on, lights the bulb in the second flip-flop which indicates a count of two.

The third pulse turns off Q2 of the first flip-flop and thus energizes the light in the collector circuit of its Q1 transistor. Now the bulbs in the first and second flip-flop are on, indicating a count of one (2^0) plus two (2^1) equal to three counts.

The fourth count will return the first flip-flop to its "0" state and thus generates a carry pulse to the second flip-flop which is also returned to its "0" state and, therefore, generates a carry pulse to the third flip-flop. The lamp in this flip-flop is now turned on indicating that four (2^2) counts have been received, etc. Since each flip-flop represents an increase of counts by a power of two this kind of counter is called a binary counter. To find the number of pulses accumulated in a binary counter, the numbers represented by the power of two of each flip-flop in the "1" state have to be added. For instance, the decimal number seven would be represented by $2^2+2^1+2^0 = 4+2+1 = 7$ or represented in binary form 00111, the number of zeros in front of the ones indicating the total number of binaries (flip-flops) included in the counter.

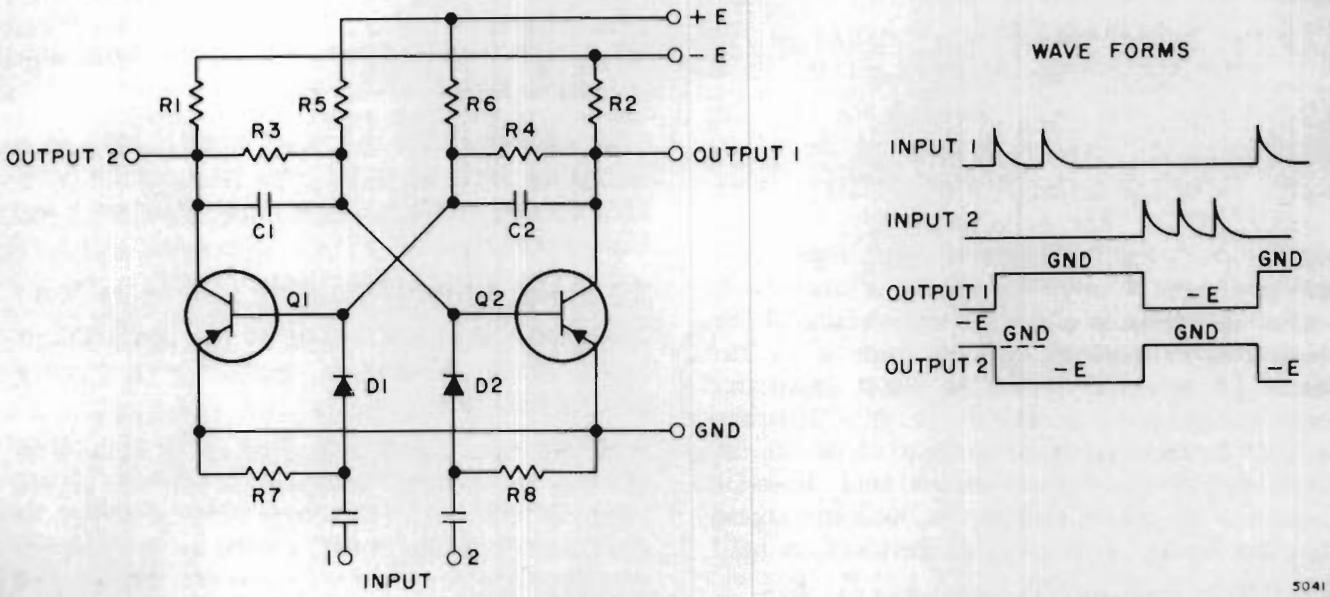


Figure 3–4. Bistable Multivibrator (Toggle), Circuit and Waveform Diagram.

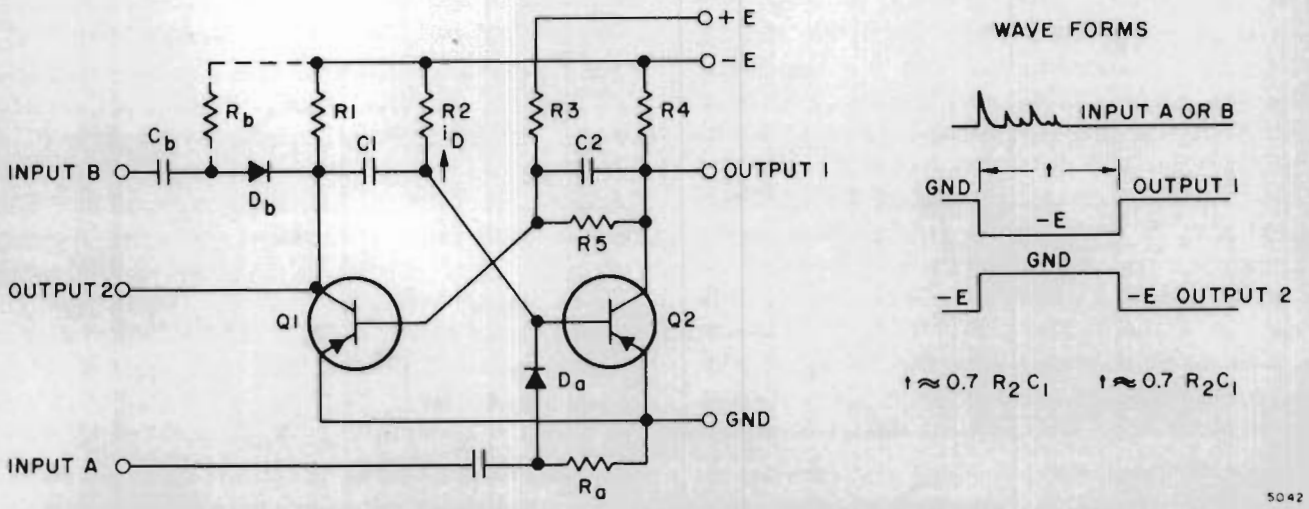


Figure 3–5. Monostable Multivibrator (One-Shot), Circuit and Waveform Diagram.

3.3.3 THE BISTABLE MULTIVIBRATOR (TOGGLE) (See figure 3–4.)

This circuit is distinguished from the flip-flop by having two inputs instead of one. Each input may be operated independently from each other. A positive signal is passed by diodes D1 and D2 to the base of transistors Q1 and Q2, respectively, and turns them off. As one transistor is turned off the other is automatically turned on through the coupling networks R3–C1 and R4–C2. The capacitors speed up the switching operation.

Thus a momentary signal on one of the inputs causes a permanent level change on the outputs, which persists until a signal is supplied to the other input. A repeated signal to the same input, of course, does not change the state of the circuit.

3.3.4 THE MONOSTABLE MULTIVIBRATOR (ONE-SHOT) (See figure 3–5.)

When a pulse of a certain duration t is required regardless of the duration or shape of the signal applied to input A or B, the circuit shown in figure 3–5 is used.

Depending on the requirement, either input configuration A or B may be used. Input circuitry A is somewhat more sensitive, but the on time of the one-shot may depend on the amplitude and duration of the input signal to some extent. Input circuitry B is not quite as sensitive but as soon as the one-shot is triggered and the collector of Q1 assumes the more positive emitter potential, diode D_b is backbiased and so disconnects the input signal from the circuit. The on time, therefore, is only determined by the values of C1 and R2 and independent of the amplitude and duration of the applied trigger signal.

In the stable state of the circuit, transistor Q2 is held on by R2 connected to the negative supply potential. The base of transistor Q1 is connected through R5 to the collector of Q2 which is at ground potential since Q2 is turned on. Through resistor R3, the base is also connected to the positive supply potential ensuring that transistor Q1 is held off.

A positive trigger signal applied to the input of the circuit turns off Q2 causing its collector to assume the negative supply potential. Through resistor R5 connected to its base transistor, Q1 is now turned on. The discharge current i_D of capacitor C1 produces a voltage drop across R2, which is positive at the junction R2–C1. Since the base of Q2 is connected to this junction this positive voltage drop holds Q2 off until current i_D has decayed sufficiently when the circuit returns to its stable state. When R2 is returned to the negative collector supply, the on time $t = 0.7 \times R2 \times C1$.

The one-shot circuit is applied when a pulse of a certain duration has to be obtained to inhibit noise generated by contact chatter or to generate a delayed pulse.

3.3.5 THE SCHMITT TRIGGER (See figure 3–6.)

This circuit does not belong to the multivibrator family but is basically an amplifier with a heavy positive feedback.

With no input signal, transistor Q1 is turned on through resistor R1 which is connected to the supply voltage −E. The voltage drop, e_b across the common emitter resistor R7 caused by the collector current of Q1, holds off transistor Q2. The base of Q2 is connected through R6 to ground potential and is, therefore, more positive than the emitter.

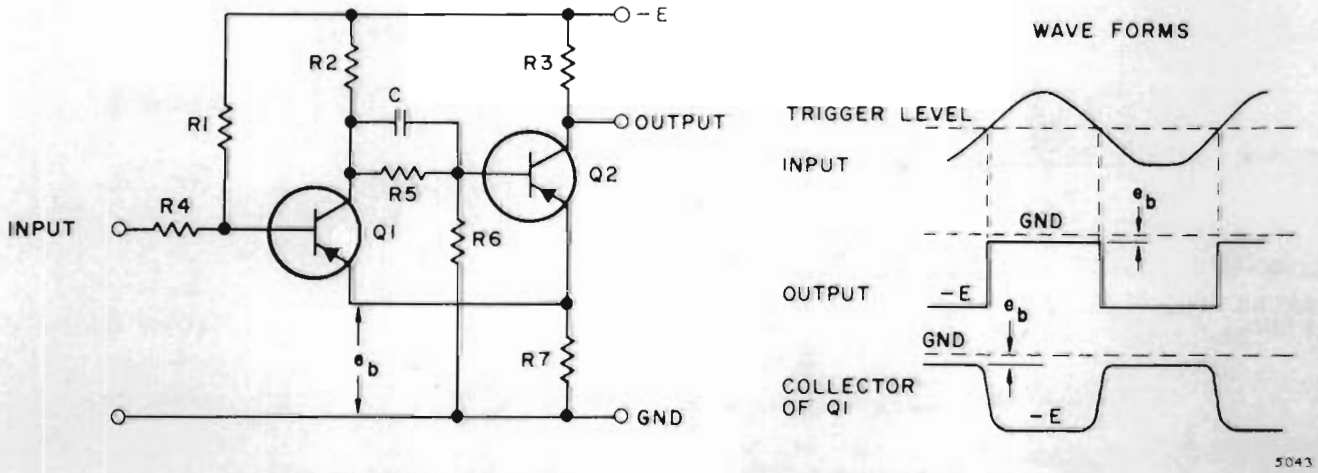


Figure 3–6. Schmitt Trigger, Circuit and Waveform Diagram.

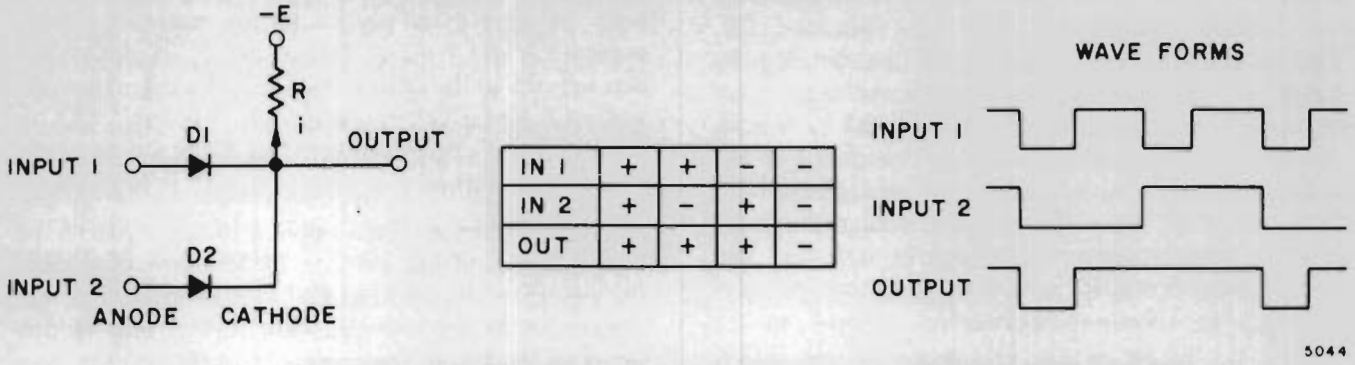


Figure 3–7. Negative AND or Positive OR Gate, Circuit and Waveform Diagram.

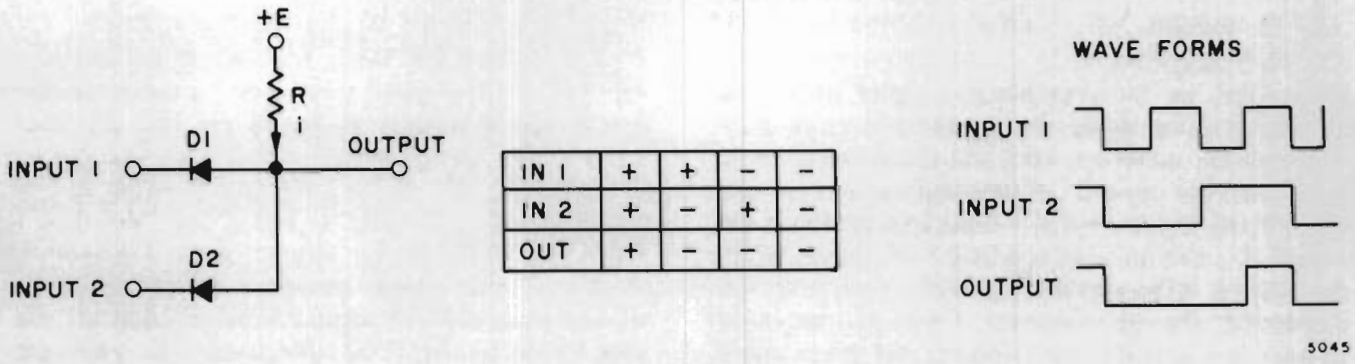


Figure 3–8. Positive AND or Negative OR Gate, Circuit and Waveform Diagram.

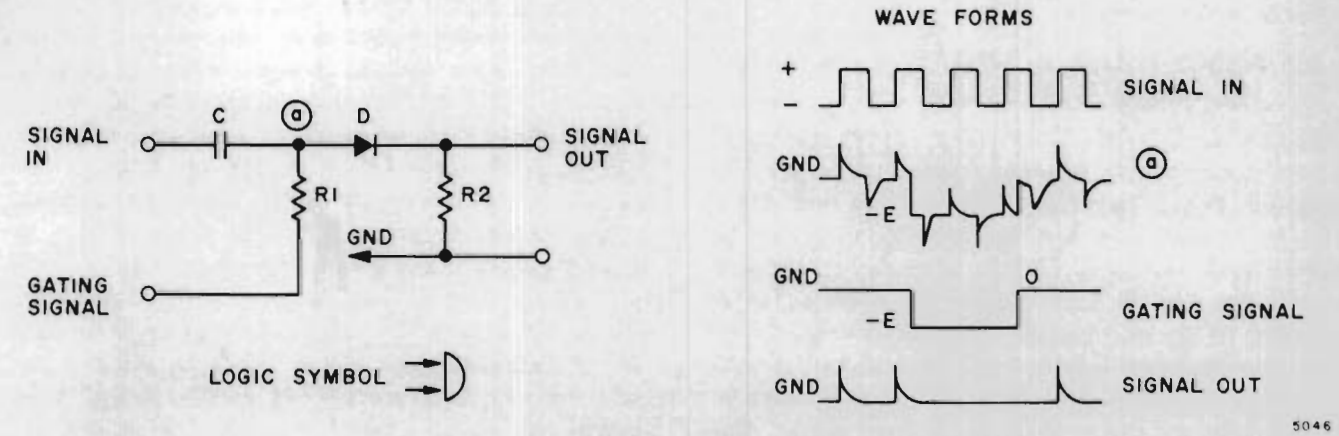


Figure 3–9. Diode Gate, Circuit and Waveform Diagram.

A positive signal exceeding the bias on the base of Q1 through resistor R4 turns this transistor off. The collector of Q1 assumes the negative supply potential −E. Simultaneously, the voltage drop across R7 disappears and transistor Q2 is turned on rapidly and speeded up by the charging current of capacitor C. The voltage at the collector of Q2 changes quickly from the negative supply potential to only slightly negative voltage e_b which is the voltage drop across R7 now caused by the collector current of Q2. When the signal voltage level recedes below the trigger level, Q1 is turned on again switching off Q2.

The Schmitt Trigger circuit is applied when a fast rising pulse has to be generated from a slowly rising signal voltage.

3.3.6 THE NEGATIVE AND or POSITIVE OR GATE (See figure 3–7.)

When an output signal has to be generated depending on the level of two signals AND or OR gates may be applied. The circuit in figure 3–7 constitutes a negative AND gate because the output always follows the more positive signal level. This occurs since the diode whose anode is more positive than the cathode is enabled to conduct current. It will pass that amount of current i so that the voltage drop across resistor R is sufficient to enable the output to assume approximately the potential of the positive input signal. The diode connected with its anode to the more negative of two or more input signals is, therefore, back biased; cannot conduct current, and thus has no effect on the output signal level. Therefore, only if input 1 and input 2 have assumed their negative reference level, can the output then assume this negative potential.

Conversely, the circuit can be considered to constitute a positive OR gate since the output is positive when either input 1 or input 2 are at the positive reference level.

3.3.7 POSITIVE AND or NEGATIVE OR GATE (See figure 3–8.)

When diodes D1 and D2 as well as supply voltage E are reversed, a gate of complementary polarity is achieved. When input 1 and input 2 are both positive, the output will also be positive. However, if either input 1 or input 2 is negative the output will be negative since it has to follow the more negative potential of the two inputs. This permits the corresponding diode to conduct and thus draw current i through resistor R. The current drawn through R is sufficient to cause a voltage drop across the resistor large enough for the output to assume the most negative of the two input signal potentials.

3.3.8 THE DIODE GATE (See figure 3–9.)

This circuit is a form of the AND gate. In figure 3–9 a square wave input signal is assumed. However, any kind of signal may be applied. The square wave is differentiated in the network C–R1 and supplied to diode D whose cathode is connected to ground potential through resistor R2. As long as the gating signal which is connected to R1 is at ground, positive signals will be passed by the diode D and appear at the output of the circuit. Negative signals will be blocked by the diode.

When the gating signal turns negative diode D is back biased and thus blocks the input signal. It is important that the negative gating signal is more negative than the maximum positive signal which can be expected to appear at the input.

3.3.9 DIODE-TRANSISTOR GATE, NAND GATE (NOR GATE) (See figure 3–10.)

The basic operation is the same as described in paragraph 3.3.6. The output of the basic gating circuit is connected to the base of transistor Q1 through resistor R3. When both inputs are negative with respect to ground, point a will assume a negative potential turning transistor Q1 on. The collector of Q1 approximately assumes ground potential, meaning that the gate signal is inverted, hence the designation NAND standing for "not and". When one of the inputs assumes ground potential, point a assumes ground potential and Q1 is turned off and assisted by resistor R4 which connects the base to the positive +E potential. The collector will now be at the negative supply potential −E. Again, since an inversion takes place with regard to the original input signal, this circuit is called a positive NOR gate standing for "not or". Resistor R4 is not necessary when the input signals swing more positive than ground potential.

3.3.10 THE INVERTER (See figure 3–11.)

As in most digital circuits the transistor Q1 is designed to operate either in its saturated or cut-off condition. This circuit is used when a complimentary signal to the original input signal is required. When the input voltage assumes a negative potential, transistor Q1 is turned on through the resistor R1. The collector of Q1, therefore, assumes ground potential. When the input signal swings to ground potential the base of Q1 is at a more positive voltage than ground because of R3 being connected to a positive supply voltage +E turning off Q1. The collector of Q1 will then assume the negative supply potential −E. This circuit thus inverts the input signal. Resistor R3 is not required when the input signal swings more positive than ground potential.

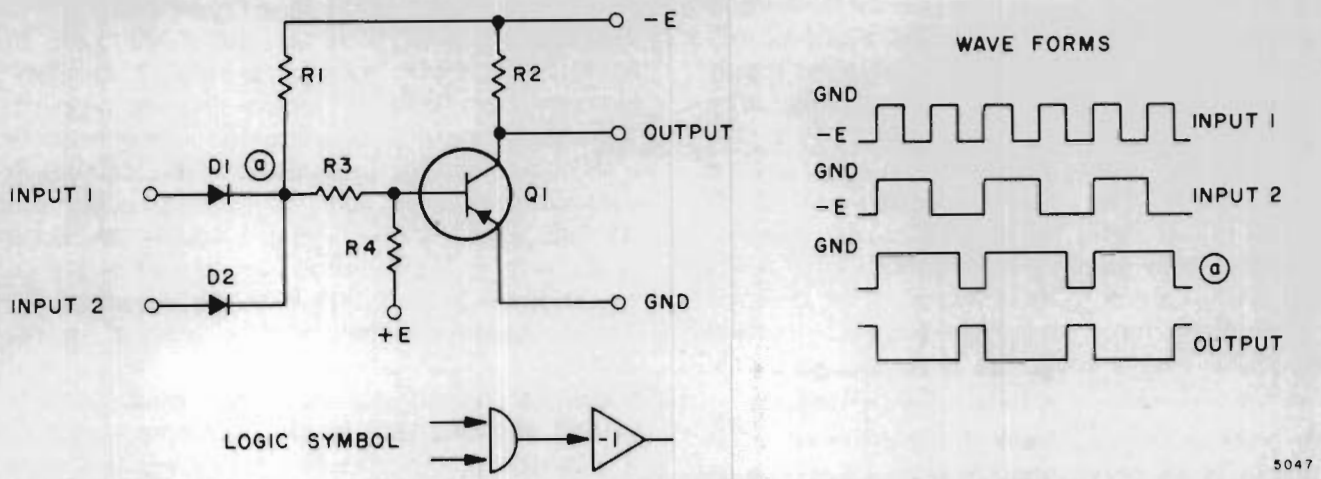


Figure 3–10. Diode-Transistor Gate, NAND Gate (NOR Gate), Circuit and Waveform Diagram.

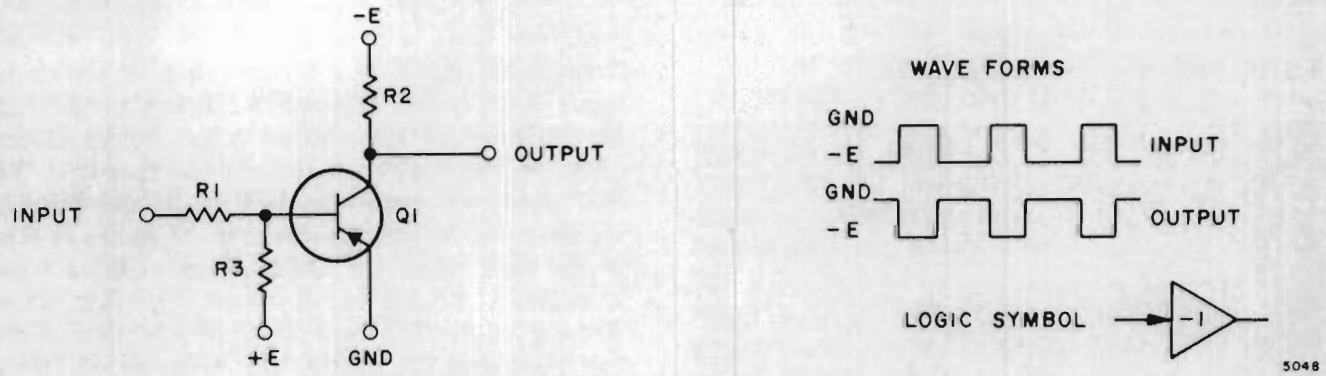


Figure 3–11. Inverter, Circuit and Waveform Diagram.

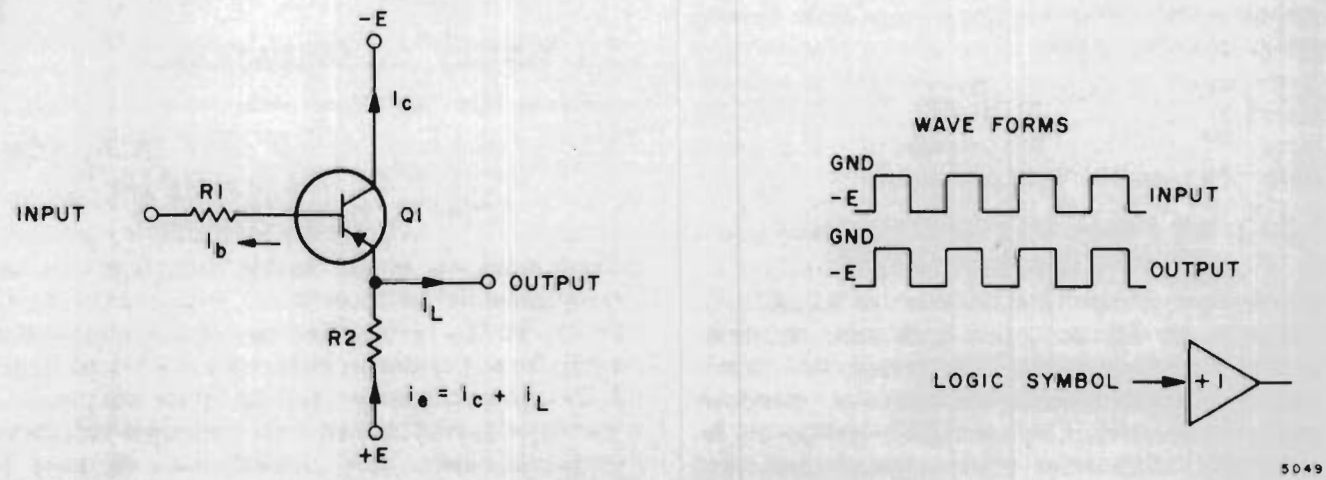


Figure 3–12. The Emitter Follower, Circuit and Waveform Diagram.

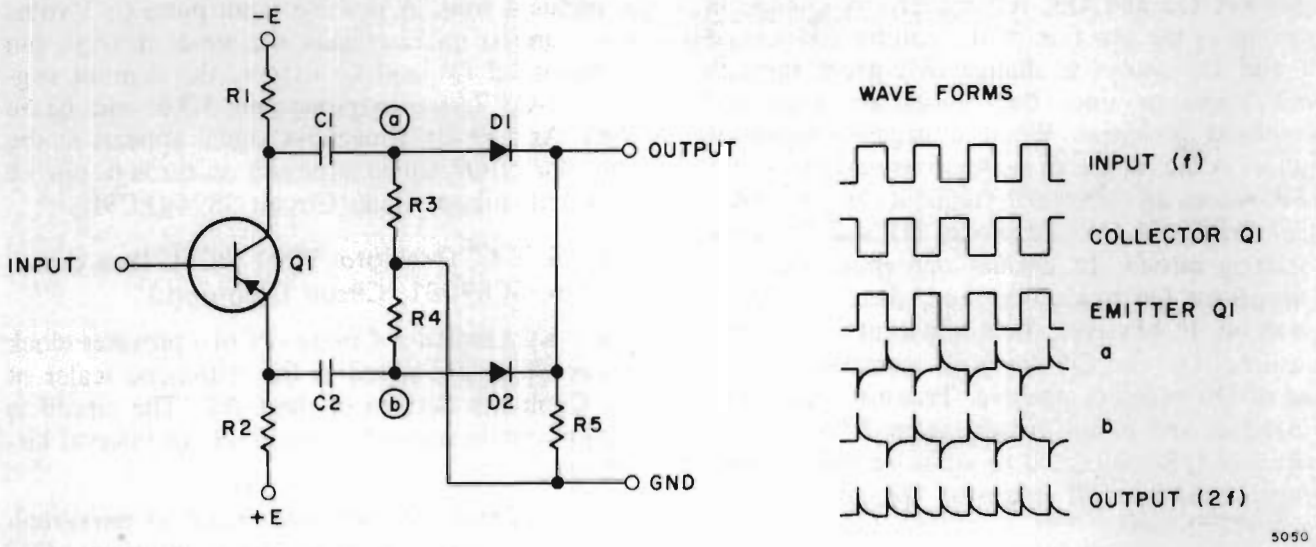


Figure 3–13. Phase Splitter-Frequency Doubler, Circuit and Waveform Diagram.

3.3.11 THE EMITTER FOLLOWER (See figure 3–12.)

As the name of this circuit implies, the emitter of Q1 follows the voltage changes of the input signal very closely. When the input signal assumes a negative potential the resulting increase in base current i_b will cause an increase in collector current i_c and since i_c approximates or is equal to i_e, a larger voltage drop across resistor R2 will occur, resulting in a more negative potential of the emitter of Q1. The emitter, therefore, follows the base voltage (input voltage), hence the name emitter follower. Since a certain current i_e is required to produce a required voltage drop across R2, the current i_c through Q1 increases or decreases depending on whether the load is lighter or heavier. The emitter follower, therefore, constitutes a low impedance output source while requiring very little driving power from the original signal source. No inversion of the signal takes place. Resistor R1 is only required to limit the base current of Q1 when the input voltage achieves the potential of —E and thus drives the transistor into saturation.

3.3.12 THE PHASE SPLITTER-FREQUENCY DOUBLER (See figure 3–13.)

The first part of this circuit consists of R1, R2, and Q1. R1 and R2 are equal and since the same current flows through them the voltage drops across them are equal. The circuit operates, therefore, jointly as an emitter follower (R2) and as an inverter (R1). The input signal appears unchanged at the emitter of Q1 and at the same amplitude, but inverted (180° out of phase) at the collector.

If the input signal is a square wave as shown in figure 3–13, pulses of twice the repetition rate can be generated by differentiating the signals at the collector and emitter of Q1. At the output of the R-C networks consisting of R3–C1 and R4–C2 (points a and b) positive and negative pulses appear at the time when the input signal changes from a negative to a positive value and vice versa. Because of the 180° out-of-phase condition of the two signals at the emitter and collector of Q1, a positive pulse appears at point a while a negative pulse is generated at point b. The reverse condition exists at the next half cycle of the input signal either at point a or point b. These positive pulses are passed by diodes D1 and D2 while negative signals are blocked. The pulse repetition rate at the output is, therefore, twice that of the input signal.

3.4 THEORY OF OPERATION

3.4.1 INPUT SECTION

3.4.1.1 Modulator Circuit 8897 (PC3L, PC4L, PC5L, PC6L) (See drawing No. SCB8897, Circuit Diagrams.)

The conversion of the analog input signal is accomplished by the Modulator Circuit 8897 (PC3L, PC4L, PC5L, PC6L). The modulator is an astable multivibrator (refer to paragraph 3.3.1 and figure 3–2) whose frequency is varied by the input signal. The input signal arrives from the input connector at pin 12 where it is conducted to the base of emitter follower Q1. The base current for the multivibrator transistors Q4 and Q5 is supplied by

transistors Q2 and Q3, respectively. A change in potential at the junction of the emitter resistors of Q2 and Q3 causes a change in current through these transistors since their bases are connected to a fixed potential. When a negative signal is applied to the input, an increase in current results which causes an increase in frequency of the modulator. Transistor Q6 and diodes D1 and D2 form a starting circuit. In normal operation, the base of transistor Q6 is negative and, therefore, Q6 is turned off. If, however, the multivibrator is locked, transistors Q4 and Q5 are both saturated and the base of Q6 becomes positive. Transistor Q6 starts to conduct and passes current through the emitter resistor of Q3, cutting off its collector current and, therefore, turning off transistor Q3, thus starting the multivibrator.

Transistor Q7 is the driver for pulse transformer T1. Only negative pulses from the secondary winding of the transformer are passed by diode D4. Resistor R18 is connected through pin 10 (RL) to the arm of the inputs switches (S11 to S14, 400A, B). In the ON position of the switch the arm is connected to ground. Diode D4 is, therefore, unbiased and can pass negative pulses. In the OFF position, the arm of the switch is connected to minus 12 volts, back biasing the diode and blocking the transfer of pulses from the modulator to the Modulator Gates Circuit 8894 (PC9L).

The CAT Models 400 and 400H do not have the input switches. In order to enable the diode to pass the pulses from the modulator, pin 10 (RL) has to be connected to pin 4 or 5 (GND) by a jumper.

The 500 KC Modulator 8836 (see drawing No. SCB8836, Circuit Diagrams) (PC3L, PC4L, PC5L, PC6L) is suggested for analysis sweeps 125 milliseconds or faster. The circuitry for the 500 KC Modulator is identical to the modulators which it replaces, up to and including the transformer (T1). The circuit description precedes this paragraph. Following the transformer, diode D4 and resistor R18 are removed and the transformer output pulses are fed to the base of transistor Q8, a phase splitter and frequency doubler (refer to paragraph 3.3.12 and figure 3–13). Resistor R24 replaces R18 to pin 10 (RL). Input switches (S11 to S14) operate diode gate formed by D5, D4 in conjunction with R24 (refer to paragraph 3.3.8 and figure 3–9).

3.4.1.2 Modulator By-Pass Circuits 8898 (PC6L) (See drawing No. SCB8898, Circuit Diagrams.)

For direct accumulation of pulses the Modulator By-Pass Circuits 8898 (PC6L) may be used. Transistor Q1 is normally held on by a 33K resistor to minus 4 volts. A positive input pulse (+2 volts, less than 10 microseconds rise time) through pin 12 turns off Q1 and so triggers the Schmitt trigger Q2-Q3 (refer to paragraph 3.3.5 and figure 3–6). As a result, a negative signal appears at the collector of Q3 which is passed on through pin 11 to the Modulator Gates Circuit 8894 (PC9L).

3.4.1.3 1 KC Oscillator 9081 (PC6L) (See drawing No. SCB9081, Circuit Diagrams.)

The 1 KC Oscillator Circuit (PC6L) provides clock pulses which are stored in the arithmetic scaler of the Computer Section of the CAT. The circuit is used to obtain sequential amplitude or interval histograms.

A free-running multivibrator (refer to paragraph 3.3.1 and figure 3–2) consisting of transistors Q1-Q2 is temperature compensated by thermistors R1 and R7. The multivibrator frequency is varied by a rheostat R4 to provide an accurate 1 KC signal. R4 is adjusted at the factory prior to shipment and should not be changed in the field.

Transistor Q3 is biased on by the minus 4 volt supply through resistor R8. Positive pulses applied to the base of Q3 through capacitor C3 turn off the transistor resulting in an inverted signal at its collector (refer to paragraph 3.3.10 and figure 3–11). The output circuit consisting of diode D1 and resistor R10 form a diode gate (refer to paragraph 3.3.8 and figure 3–9). The open or closed condition of this gate is determined by the position of the INPUTS switch (S11).

3.4.1.4 Modulator Gates 8894 (PC9L) (See drawing No. SCB8894, Circuit Diagrams.)

The negative output pulses from the four Modulator Circuits (PC3L, PC4L, PC5L, PC6L) arrive on pins 9 to 12 and are passed on through capacitors C1 to C4 to the bases of Q1, Q3, Q5, and Q7. Transistors Q2, Q4, Q6, and Q8 are gating transistors for the respective transistors receiving the input pulses from the Modulator Circuits. In order to pass on the modulator pulses to the Arithmetic Decade in the Computer Section through pin 8 (ARA1), the gating transistor has to complete the current path for the input transistor. The gating transistors are controlled by the signals 1, 2, 3, and 4 which are generated on the Modulator Gate Control Circuit 8895 (PC8L).

When the INPUTS IN USE switch (S1) is in the 1 position, signal 1 remains negative while the other three lines stay positive. Transistor Q2, therefore, is turned on while the other gating transistors remain off. Only pulses from modulator 1 can be

passed on to the Arithmetic Decades. With S1 in the 2 position, signals 1 and 2 alternately go negative and positive, in turn passing pulses from Modulator Circuits 1 and 2. If the INPUTS IN USE switch (S1) is placed in the 4 position, signals 1 to 4 successively turn negative and thus pass pulses from Modulator Circuits 1 to 4. However, pulses may only be passed when an analysis sweep is in progress and must be blocked when the memory goes through a storage cycle. This interlock is accomplished by transistors Q10, Q11, and Q12. During a memory cycle, the memory busy signal (MB) is negative, turning on transistor Q11. This action turns off Q12 and so disables all modulator gates. Similarly, at the end of an analysis sweep the control flip-flop signal (CFF+) from the Delay Control Flip-Flop Circuit 8890 (PC13L) becomes negative and turns on transistor Q10 which is parallel to Q11 to turn off Q12, again disabling all modulator gates. Transistor Q9 is an inverter (refer to paragraph 3.3.10 and figure 3–11) which generates a CFF+ signal from CFF− obtained from the Delay Control Flip-Flop Circuit 8890 (PC13L).

3.4.1.5 Delay Control Flip-Flop Circuit 8890 (PC13L) (See drawing No. SCB8890, Circuit Diagrams.)

The Delay Control Flip-Flop Circuit 8890 (PC13L) generates the main control signals (CFF+ and CFF−) for the accumulate mode of the CAT. In the reset or off state Q5 is turned off and Q6 is turned on (Toggle, refer to paragraph 3.3.3 and figure 3–4). When a trigger pulse from the Trigger Generator Circuit 8999 (PC10L) arrives at pin 8, transistor Q3 is turned on for the duration of this pulse generating a positive signal on its collector. This positive signal is conducted through a capacitor and a diode to the base of Q6, turning it off. The collector of Q6, therefore, assumes the negative supply potential and thus the negative signal (CFF−) is generated. An inverter circuit (refer to paragraph 3.3.10 and figure 3–11) located on the Modulator Gate Circuit (PC9L) using transistor Q9, inverts the CFF− signal to form CFF+. To avoid accidental triggering of the control flip-flop, transistor Q7 holds the collector of Q6 positive when the CAT is not in the accumulate mode during an analysis sweep. This is achieved by connecting the base of Q7 to the positive accumulate flip-flop signal (AFF+) from the Control Logic Circuit in the Computer Section which is in its negative state in all but the accumulate mode, thus holding Q7 on. An analysis sweep is started at the instant the control flip-flop is turned on by releasing the 51.2 KC oscillator in the 51.2 KC Oscillator and Shaper Circuit 8888-2 (PC17L). Simultaneously, the modulator gates are enabled to pass pulses from one or more modulators as selected by the INPUTS IN USE switch (S1). Also through a negative signal (CFF−) to the Control Logic Circuit the initiation of any other mode during the analysis sweep is prevented. At the end of a sweep a positive address overflow pulse (AOF) from the Scale of Four/Memory Location Circuit in the Computer Section is generated which resets or turns off the control flip-flop. The oscillator is stopped and thus any further address (sweep) advance signals are inhibited; the modulator gates are closed until a new trigger pulse occurs.

When PRE ANALYSIS DELAY is used, the switch (S10) between pins 6 and 10 is closed connecting the emitter of Q2 to plus 4 volts enabling this transistor. Since Q5 is in the off state before a trigger signal is received, Q2 could be turned on. However, the junction of R12 and R18 is clamped to plus 4 volts by transistor Q4 which is kept on by the negative inhibit delay signal (INHD) from pin 18. Another interlock is provided by the accumulate flip-flop signal (AFF+) which is also connected to the base of Q4. Since AFF+ is negative when the CAT is not in the accumulate mode, the junction R12-R18 is again clamped to plus 4 volts holding off Q2. Thus an accidental start of the delay is prevented.

When a trigger pulse is received at the Trigger Generator Circuit 8999 (PC10L), the inhibit delay signal goes to plus 4 volts and turns off Q4, thus enabling the negative collector voltage of Q5 to turn on Q2. The junction of R7 and R11 assumes a positive potential with respect to minus 20 volts back biasing diode D1, and charging capacitor C1 through the 1 megohm PRE ANALYSIS DELAY potentiometer (R6) located on the front panel. When the voltage across C1 reaches the triggering level of the Schmitt trigger (refer to paragraph 3.3.5 and figure 3–6) Q9-Q10, a positive pulse is generated at the collector of Q10 which sets the control flip-flop and so starts a new analysis sweep.

3.4.1.6 Trigger Generator 8999 (PC10L) (See drawing No. SCB8999, Circuit Diagrams.)

The Trigger Generator Circuit 8999 (PC10L) provides the trigger pulses which set the control flip-flop and thus initiate an analysis sweep.

With the TRIG. switch (S8) in the INT. position the first pulse to trigger the one-shot multivibrator (refer to paragraph 3.3.4 and figure 3–5) formed

by Q1 and Q2 is derived from the positive accumulate flip-flop signal (AFF+) from the Control Logic Circuit in the Computer Section. When the START pushbutton (SL1) is depressed, the AFF+ signal goes positive and turns off Q1. The collector of Q1 becomes negative and remains so for 100 microseconds. When it swings back to a positive potential, a positive pulse is derived through C4 and passed through D7 to the base of Q3. Transistor Q3 is turned off for the duration of this pulse producing a negative signal which is passed through pin 8 to the Delay Control Flip-Flop Circuit (PC13L). The same negative pulse also turns on Q4 of the toggle Q4-Q5 (refer to paragraph 3.3.3 and figure 3–4). If a pre-analysis delay had been selected, the delay action as described in paragraph 3.4.1.5 would be started because the inhibit delay signal derived from the collector of Q4 swings positive, turning off the inhibiting transistor Q4 on the Delay Control Flip-Flop Circuit 8890 (PC13L). At the end of an analysis sweep the CFF+ signal assumes a negative potential and through C10 and D9 resets the toggle Q4-Q5 making it ready to repeat the action as described above. Simultaneously, an address overflow pulse (AOF) from the Scale of Four/Memory Location Circuit in the Computer Section is obtained at the end of each sweep which triggers the one-shot Q1-Q2 and a new trigger signal for the control flip-flop is generated.

The TRIG. switch (S8) at the INT. position applies a negative potential to diode D6 through pin 14 which is thus back biased (Diode Gate, refer to paragraph 3.3.8 and figure 3–9) and blocks any external trigger signal which might be supplied to the EXT TRIG. BNC jack (J107).

With S8 in the EXT. position, this negative potential is applied to D7 through pin 11 preventing any internal trigger from reaching the base of Q3. A positive external trigger pulse through J107 is applied to the base of Q3 through C5 and D6. A negative signal is generated again at the collector of Q3 as described, and through D2, triggers the flip-flop in the Delay Control Flip-Flop Circuit 8890 (PC13L).

3.4.1.7 Modulator Gate Control Circuit 8895 (PC8L) (See drawing No. SCB8895, Circuit Diagrams.)

The Modulator Gate Control Circuit 8895 (PC8L) generates the gating signals for the Modulator Gate Circuit (PC9L) and also the control signals which switch the quarters and halves of the Scale of Four/Memory Location Circuit in the Computer Section. The circuit consists of two flip-flops (refer to paragraph 3.3.2 and figure 3–3) and a four line decoder. The input signals for the flip-flops are obtained from the 51.2 KC Oscillator and Shaper Circuit 8888-2 (PC17L) through the arm of the ANALYSIS TIME switch (S2). The pulses are conducted to pin 10 and through C1 and D2 or C3 and D3, respectively to the base of Q1 or Q2.

The decoding of the two binary signals into four successive signals occurs in transistors Q5 to Q8. The base of each of these transistors is connected to two of the four complimentary lines from the collectors of Q1 to Q4. Only when both lines connected to one base of the decoding transistors are positive will the transistor be turned off and its collector attain the negative supply potential and thus generate the negative signal at 1, 2, 3, or 4, respectively.

In the 4 position of the INPUTS IN USE switch (S1) the flip-flops are properly reset by the positive signal (CFF+) from the Delay Control Flip-Flop Circuit (PC13L), which is negative before an analysis sweep starts. In this configuration, Q2 and Q4 are turned on. Signals from the 51.2 KC Oscillator and Shaper Circuit (PC17L) received through pin 10 (ARM) are routed to the first flip-flop, Q1-Q2, and at one half the frequency, carried to the second flip-flop Q3-Q4. Simultaneously, the decoding transistors generate the gating signals for the Modulator Gate Circuit (PC9L) to turn on the individual modulators in the proper sequence. Furthermore, the signals Q^0 (pin 13) and outputs 3 and 4 gate the flip-flops on the Scale of Four/Memory Location Card in the Computer Section. Thus, pulses from the 51.2 KC Oscillator and Shaper Circuit (PC17L) indirectly drive the two flip-flops on the Scale of Four/Memory Location Circuit through a full cycle before the Address Decade Circuit in the Computer Section is advanced by one count. Since each combination in the state of the two flip-flops represents one particular quarter of the memory; and since they are synchronized with the operation of the flip-flops in the Modulator Gate Control Circuit, the pulses from modulator 1 are stored in the first quarter, the pulses from modulator 2 in the second quarter, etc. Refer to drawing No. WFB8975 for waveform and timing information in the 4 inputs in use mode of operation, and drawing No. B1432 for detailed connections on the INPUTS IN USE switch (S1).

With the INPUTS IN USE switch (S1) in the 2 position, HOLD 2^1 (pin 12) is connected to ground, thus blocking the carry pulses from the first to the second flip-flop in the Modulator Gate Control Circuit

(PC8L). Only the first flip-flop operates under this condition. Transistor Q3 is turned on by the control flip-flop signal (CFF+) which is negative before an analysis sweep is started. The decoding transistors Q7 and Q8, therefore, always remain on; 3 and 4 stay positive. Since 3 and 4 control the gates of modulators 3 and 4, these gates remain closed. Transistors Q5 and Q6 are alternately turned on by the signals from the collectors of Q1 and Q2. Gating signals 1 and 2 thus alternately turn negative and positive, operating the gates. Through the INPUTS IN USE switch (S1), the second flip-flop on the Scale of Four/Memory Location Circuit in the Computer Section is operated by signal 2. As a result, the halves of the memory are alternated with the modulator gates in such a manner that when pulses from modulator 1 are passed through the gate, the address register and, therefore the memory, are in the first half, and when modulator 2 is on, they change over to the second half. Refer to drawing No. WFB8976 for timing and wave shapes and drawing No. B1432 for detailed connections on the INPUTS IN USE switch (S1).

With the INPUTS IN USE switch in the 1 position the first flip-flop (Q1-Q2) in the Modulator Gate Control Circuit is disabled by grounding HOLD "0" (2^0) (pin 11). Being reset by the CFF+ signal, the state of the two flip-flops is such that gating signal 1 is negative and gating signals 2, 3, and 4 are positive. The four outputs remain in this state because the flip-flops are held in their positions. Consequently only modulator gate 1 is open, and signals 2 and 4, through the INPUTS IN USE switch (S1), controlling the flip-flops on the Scale of Four/Memory Location Circuit are connected to plus 4 volts. Therefore, the address register operates in a normal manner counting through all 400 channels in numerical order. Refer to drawing No. WFB8977 for waveforms and timing and drawing No. B1432 for detailed connections on the INPUTS IN USE switch (S1).

3.4.1.8 51.2 KC Oscillator and Shaper Circuit 8888–2 (PC17L) (See drawing No. SCB8888–2, Circuit Diagrams.) Oscillator frequency for CAT 400 is 12.8 KC. (See drawing No. 8888.)

The 51.2 KC Oscillator and Shaper Circuit 8888-2 (PC17L) provides the timing (clock) pulses which determine the analysis sweep time. An LC type oscillator is employed to ensure good frequency stability. The winding, T1, of the oscillator coil forms a tuned circuit with capacitor C1 in the collector circuit of Q2. Regeneration is obtained through the winding T2 in the base-emitter circuit. A coarse frequency adjustment is obtained with a padding capacitor to C1. The fine adjustment is achieved by moving the tuning slug in the oscillator coil into or out of the core, varying its inductance.

NOTE

Frequency adjustment is aligned at the factory. No further aligning is necessary.

The oscillator is turned on at the start of an analysis sweep and turned off at the end of the sweep. This switching (gating) is accomplished when transistor Q1 is actuated by a signal from the Delay Control Flip-Flop Circuit (PC13L) signal (CFF+). When no analysis sweep is in progress, the CFF+ signal is negative and transistor Q1, therefore, is turned on, holding down the collector voltage of Q2 and thus preventing it from oscillating.

The oscillator signal is connected to the input of a Schmitt trigger (refer to paragraph 3.3.5 and figure 3–6), Q3 and Q4. This shapes the sinusoidal oscillator signal into narrow rectangular pulses with a faster rise time than the original sinusoidal signal.

The output pulses from the Schmitt trigger are connected to a buffer stage and gated again by a control flip-flop signal (CFF−). This avoids the occurrence of any unwanted pulses from the decaying oscillation of the tuned circuit when the oscillator is gated off. This is accomplished in Q5 and Q6.

3.4.1.9 Scale of 16 Circuit 8889 (PC14L, PC15L, PC16L) (See drawing No. SCB8889, Circuit Diagrams.)

Three Scale of 16 Circuit cards are used to divide the oscillator frequency by successive steps of 2. Each card contains four binaries (flip-flops) (refer to paragraph 3.3.2 and figure 3–3) formed by transistor pairs Q1-Q2, Q3-Q4, Q5-Q6, Q7-Q8, and their associated circuitry. The output (collector of even numbered transistors) of each binary is connected to the input of the succeeding stage.

At the end of each analysis sweep all binaries are reset to their "1" state, meaning that all collectors to which subsequent binaries are connected assume their negative supply potential. The first pulse received from the oscillator will thus change the state of all twelve binaries. In Models 400A and 400H the first three binaries are only used to divide the oscillator frequency by a total of eight so that the first frequency used for timing of the analysis sweep is 6.4 KC, providing one pulse every 156 microseconds. Since each timing pulse advances the sweep by one channel, a total analysis time for 400 channels of 62.5 milliseconds is achieved.

The collectors of the even numbered transistors of the third to the twelfth binaries are connected to the ANALYSIS TIME switch (S2). With this switch it is then possible to select the analysis times as shown on the front panel.

3.4.1.10 External Address Control Circuit 8998 (PC12L) (See drawing No. SCB8998, Circuit Diagrams.)

External address advance pulses received through ADDR. ADV BNC jack (J103) on the rear panel are routed to pin 8 of the External Address Control Circuit 8998 (PC12L). Diodes D1 and D2 protect the base of the input transistor Q1. The input transistor Q1 is forward biased by R1 and therefore is normally in its on state. Transistors Q2 and Q3 form a Schmitt trigger circuit (refer to paragraph 3.3.5 and figure 3–6) and Q4 an inverter (refer to paragraph 3.3.10 and figure 3–11) circuit is the output transistor. A positive pulse applied to J103 will turn off Q1. The negative voltage thus appearing at the collector of Q1 turns on Q2 and produces a negative-going signal at the collector of Q3. This negative signal is coupled through C3 to the base of Q4 which then is turned on producing a positive pulse at the collector of Q4. Through pin 10 this pulse is routed to the EXT. position of the ANALYSIS TIME switch (S2) which in turn channels it to the Modulator Gate Control Circuit (PC8L) to perform the same functions as the internally generated timing pulses. An interlocking circuit formed by Q13 prevents address advance pulses from being generated when the CAT is not ready to go through an analysis sweep or during a memory cycle. The control flip-flop signals (CFF+) from the Delay Control Flip-Flop Circuit (PC13L) (negative when not ready to sweep) and memory busy signals (MB) from the Auto Data Transfer Circuit in the Computer Section (negative during a memory cycle) turn Q13 on during their negative period and thus prevent the voltage at the collector of Q1 to go negative when an external address advance pulse is received during this time.

The second part of the circuitry of this card controls the address reset function. An address reset pulse received through the ADDR. RESET BNC jack (J101) enters the circuit through pin 12 and triggers a one-shot (refer to paragraph 3.3.4 and figure 3–5) Q5-Q6 through the base of Q6. Immediately a storage cycle is initiated by a positive external reset control signal (ESC) derived from the collector of Q5. This signal also resets the Delay Control Flip-Flop Circuit (PC13L). The pulse duration of this one-shot is 25 microseconds. At the end of the on-time, a second 25 microsecond one-shot, Q9-Q10 is triggered and a positive start of conversion signal (SOC) is generated which resets the address register comprised of the two Second Address Decade Circuits and the Scale of Four/Memory Location Circuit in the Computer Section. After 25 microseconds a SET CFF signal is obtained from the collector of Q11 which is controlled by Q9. This signal turns on the Delay Control Flip-Flop Circuit (PC13L) thus enabling the start of a new sweep.

To ensure the address is reset before an analysis run is started, a trigger address reset signal (TAR) is derived from the accumulate flip-flop signal (AFF+) entering the card at pin 20 and going out at pin 15. The AFF+ signal becomes positive as soon as the START pushbutton is pressed. The AFF+ signal through transistor Q8 also prevents an erroneous initiation of a storage cycle when the CAT is not in the accumulate mode, by holding the Q5-Q6 one-shot in its stable state.

3.4.1.11 Stimulus Pulse Generator Circuit 8892–2 (PC11L) (See drawing No. SCB8892–2, Circuit Diagrams.)

The purpose of the Stimulus Pulse Generator Circuit 8892-2 (PC11L) is to provide an output pulse either at the beginning of an analysis sweep or when the sweep enters the 20th address depending on the position of the STIM switch (S9) on the front panel.

With S9 at the PROMPT position a positive pulse (INH. DEL. & PROMPT OUT) generated at the Trigger Generator Circuit (PC10L) is passed to pin 12 and triggers one-shot (refer to paragraph 3.3.4 and figure 3–5) Q3-Q4 which turns on Q5. The collector of Q5 is maintained at minus 50 volts by the voltage divider R16-R17. On receiving a pulse from the one-shot, Q5 saturates, thus creating a 50 volt positive-going pulse (Model 400B) which then is connected through a capacitor and pin 15 to the STIM. BNC jack (J105) on the rear panel.

NOTE

Positive-going pulses to J105 for CAT Models 400, 400A, 400H are plus 15 volts. (See drawing No. 8892-1, Circuit Diagrams.)

With S9 in the ORD 20 position, the toggle (refer to paragraph 3.3.3 and figure 3–4) Q1-Q2 is used. In its reset state Q1 is on and Q2 is off. The signal on pin 8 (2^1) is obtained from the Second Address Decade Circuit in the Computer Section. It appears once every 20 addresses. The first time it appears at address 20, it sets the toggle Q1-Q2, turning off Q1.

This action generates a positive pulse at the collector of Q2, which is passed through pin 10 on to S9 and from there back to pin 12, generating a stimulus pulse as described in the previous paragraph. Any subsequent (2^1) signals do not change the state of the circuit until an address overflow signal (AOF) from the Scale of Four/Memory Location Circuit in the Computer Section appears at the end of an analysis sweep, resetting the toggle so that the first (2^1) signal can set it again.

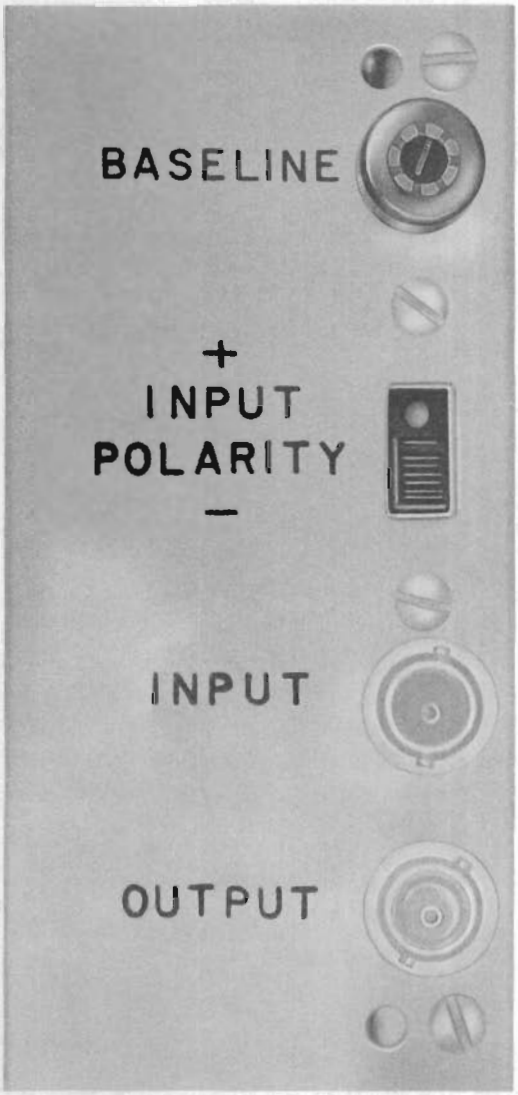


Figure 3–14. Trigger/Amplitude Discriminator, 8842, Front View.

3.4.1.12 Trigger/Amplitude Discriminator 8842 (PC2L) (See figure 3–14 and drawing No. 8847 Circuit Diagrams.)

The Trigger/Amplitude Discriminator Circuit (PC2L) permits the CAT to be externally triggered from a fairly slow rising input signal. The signal is applied at the INPUT jack (J1) on the front panel integral to the circuit card. The OUTPUT signal is fed through J2 on the card and is connected to the EXT. TRIG. jack (J107) at the rear panel of the CAT. Pulses from the Trigger/Amplitude Discriminator through J107 start an analysis sweep when the TRIGGER switch (S8) is at the EXT. position. An INPUT POLARITY switch (S1) on the card permits polarity matching with the input signal and the BASELINE potentiometer (R8) sets the level at which the input signal will trigger the CAT. Refer to paragraph 4.1.7 for trigger level adjustment.

The input signal, positive or negative, is connected to the base of transistor Q5 through capacitor C1. Transistor Q4 must have a positive potential on its base to be at the off state. This permits a negative potential at the base of Q3 to fire the Schmitt trigger configuration Q2-Q3 (refer to paragraph 3.3.5 and figure 3–6). To turn off Q4, a positive potential is selected by the INPUT POLARITY switch (S1) from either the emitter or the collector of Q5. If a negative pulse is applied at the input, a positive pulse appears at the collector. If a positive pulse is applied at the input, a positive pulse appears at the emitter. The switch is manually positioned to match this input polarity and, in so doing, connects the proper signal to the base of Q4, turning it off.

When Q4 is off, Q3 is turned on, turning off Q2. The collector of Q2 at negative potential is transmitted to the base of Q1 turning it on. The signals from the collector of Q1 provide positive output pulses not less than 2 volts in amplitude at the OUTPUT jack (J2).

3.4.2 COMPUTER SECTION (See figure 3–1.)

3.4.2.1 General

The function of the CAT Computer Section is to accumulate and store data which have been received in digital form from the Input Section. Upon command from the operator, the stored data will be displayed on the CRT. Data are also made available to external readout equipment in either digital or analog form.

The Computer Section generates the functional signals which compose the memory cycle phase of CAT operation. A memory cycle is initiated by a

clock pulse from the Input Section. The pulse constitutes the end of an accumulation period set by the PRE ANALYSIS DELAY switch (S2) for one address. The data accumulated in an address of the arithmetic scaler are written into the core memory. The address register is then advanced to the next address where data stored in that address are read into the arithmetic scaler. The arithmetic scaler is then ready to receive new data from the Input Section. The stated procedure is repeated for each of the 400 addresses.

3.4.2.2 Control Logic Circuit 8500 (PC1R) (See drawing No. SCB8500, Circuit Diagrams.)

The Control Logic Circuit is the master programmer of the CAT. It controls the three primary operations (accumulate, display, readout) and the inactive state (stop) of the CAT as selected by the front panel pushbuttons (START, DISPLAY, READOUT, STOP). Each state has an associated pushbutton with a built-in indicator lamp.

The Control Logic Circuit consists of five toggles (refer to paragraph 3.3.3 and figure 3–4) designated as ready accumulate, accumulate, display, ready read, and readout. Each of these transistor flip-flop circuits enables circuitry in other computer-control cards to accomplish the program commanded by the applicable pushbuttons. Diode-resistor logic prevents the operation of more than one flip-flop (toggle) or one combination of flip-flops at any given time, i.e., only a single state can be selected at any time.

When the STOP lamp is lighted, all program flip-flops are reset. However, in the accumulate mode, the lamp will not go on until a full sweep has been completed.

The Control Logic receives enabling, busy, and completion signals from supplementary programming circuits to inhibit or evoke further commands. Memory Busy (MB) from the Auto Data Transfer Circuit (PC2R) or a CFF— signal from the Input Section indicates that either an analysis sweep is in progress in the Input Section or the Computer Section of the CAT is in a storage cycle. The signals inhibit the stopping of CAT operation until a cycle or sweep is completed.

3.4.2.3 Auto Data Transfer Circuit 8501 (PC2R) (See drawing No. SCB8501, Circuit Diagrams.)

Operating in conjunction with the front panel switches and the Control Logic Circuit, the Auto Data Transfer Circuit controls the readout and storage of data out of and into the CAT memory. This circuit enables the storage of all counts deposited into the arithmetic scaler. A gross count flip-flop is enabled by the clock pulse (GRTR) Gross Trigger from the ANALYSIS TIME switch (S1). When the gross count flip-flop is in the on state, the clock pulses (GRTR) are directed to the write-read trigger one-shot multivibrator (refer to paragraph 3.3.4 and figure 3–5) which initiates the memory cycle shown on drawing No. WFB8974, Circuit Diagrams.

3.4.2.4 Read Cycle Generator Circuit 8502 (PC3R) (See drawing No. SCB8502, Circuit Diagrams.)

The Read Cycle Generator Circuit forms signals which control the complete read cycle. This circuit receives command signals from the front panel controls, the Control Logic Circuit, the Auto Data Transfer Circuit, and signals from the Input Section. The signals in this circuit are generated by a string of gated monostable multivibrators. The Read Cycle Generator Circuit produces the signal sequences which combine the read busy signal as shown in the Memory Timing drawing Nos. WFB8442, WFB8445, and WFB8974, Circuit Diagrams. This sequence commands the entire chain of events necessary to a read cycle, during which information is sensed from the magnetic core memory at a particular address or ordinate and is read into the arithmetic scaler.

Circuits on this card not included within read cycle operation are the Address Reset Circuit (AR) Q1, Q2, Q3 and the Arithmetic Add Circuit (ARA1) Q16, Q17. The ARA1 circuit provides the test program for the Computer Section.

3.4.2.5 Write Cycle Circuit 8504 (PC5R) (See drawing No. SCB8504, Circuit Diagrams.)

The Write Cycle Generator Circuit forms the signals necessary for the write portions of a memory cycle. These signals are shown on the Memory Timing drawing Nos. WFB8442, WFB8445, and WFB8974, Circuit Diagrams, and form the write busy signal.

3.4.2.6 Memory Current Generator 8503 (PC4R) (See drawing No. SCB8503, Circuit Diagrams.)

The Memory Current Generator Circuit supplies the READ and WRITE currents for operation of the magnetic core memory. For a reading-out and writing-in sequence, the address (channel) of magnetic cores to be pulsed are selected in the address

register. The actual 410 milliampere half-read or half-write currents are generated in the Memory Current Generator Circuit upon command from the Read or Write Cycle Generator Circuits. Note that a READ pulse will cause currents to flow in one direction through the memory cores while a WRITE pulse will cause memory currents to flow in the opposite direction. One half of each transformer primary (T1, T2) is used in one case and the other half in the other case. A 25 turn, 1K ohm potentiometer is used to adjust the current output of the generators to approximately 410 milliamperes. Refer to paragraph 4.1.2 for adjustment procedures.

Also located in the circuit are two free-running multivibrators, Q12-Q13 and Q14-Q15 (refer to paragraph 3.3.1 and figure 3–2). These are the Display oscillator and the Plot oscillator for X-Y recorder use.

3.4.2.7 Memory Operation (See figure 3–15, and drawing No. B8916, Circuit Diagrams.)

The prime element of the CAT memory is a ferrite magnetic core. The rectangular shape of its hysteresis loop is pertinent to the description of the core as used in a memory application. In any hysteresis loop, such as curve A, figure 3–15, H is the magnetic motor force (MMF) strength and is proportional to the ampere-turns which cause it. Since the current is proportional to the MMF, reference is only made to the currents that magnetize the core.

As used in a magnetic core memory, the core can be in two possible magnetic states; either positive or negative. These two states represent a binary bit of information and an arbitrary choice can be made as to which state represents "0" and which represents "1". In the CAT, the choice presumes that +B on curve A, figure 3–15, represents "1" and −B represents "0". If it is assumed that a core is in the "1" state and a current, I, is passed through it, it would move from position a on the loop to position b. However, no significant change occurs in B. Further, when the current is removed, it will return to position a and the "1" state will remain. On the other hand, if the core is in the "0" state and the current I is passed through, it will move from position c to position b on the loop. When the current is removed it will move to position a. Through this cycle the condition of the core has clearly changed from "0" to "1". A completely analagous situation follows logically when a negative current, −I, is passed through the core. In this case the "0" state will remain unchanged and

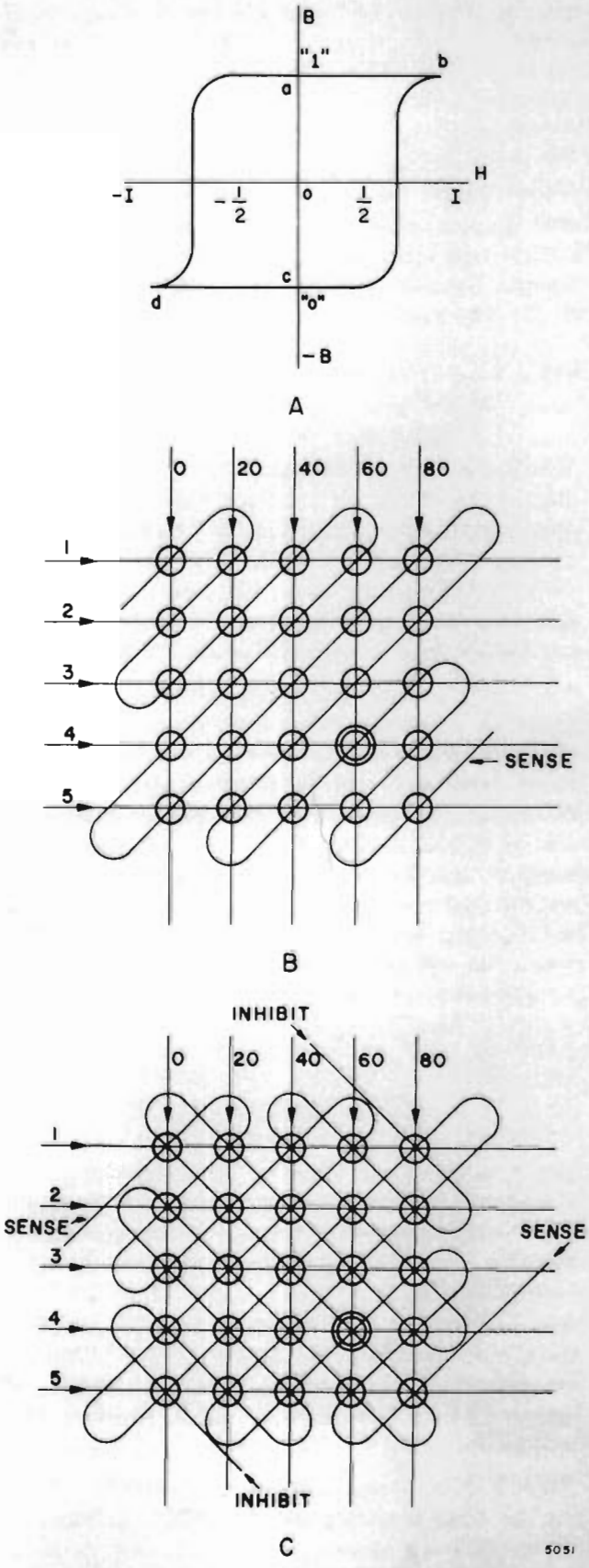


Figure 3–15. Memory Core Operation Diagram.

the "1" state will be changed to "0". If, however, either ±1/2 I current (410 ma) passes through the cores, it is evident that there will be no change regardless of the existing state of the core. The actual amount of the currrent required to switch the cores used in the CAT is approximately 820 milliamperes.

The illustration B, figure 3–15, represents an array of 25 cores arranged in a matrix with each core having two wires passing through it at right angles. If a current of 1/2 I (410 ma) flows through the wire designated 4, none of the cores through which the 4 wire passes can change their state. If, at the same time, a current of 1/2 I were passed through the wires designated 60, the single core through which the 60 wire and the 4 wire pass would now have what amounts to the current of magnitude I passing through it (820 ma). If this core had previously been in a "0" state it would switch to a "1" state. Similarly, as in the case of the 4 wire, the half-current which passes through the other cores of the 60 wire would be insufficient to cause switching of those core states.

By feeding half-currents (410 ma) through appropriate wires, any single core in the matrix can be individually switched. Moreover, each core can be uniquely designated by its numbered wires so that the cores described by the 4 and 60 wires is simply core 64. Similarly, core 25 is the core at the intersection of the 5 wire and the 20 wire, etc. In the CAT there are 20 horizontal wires, 20 vertical wires and 400 cores in a single memory core plane to comprise 400 channels or addresses. However, a single memory plane is only capable of handling one bit of information per channel or address since the single core can only have a "0" or "1" state. If two planes are taken with appropriately numbered wires connected in parallel, each channel or address now has two cores associated with it and can store two bits of information. By adding additional planes in parallel with these two, it is possible to obtain as high an address count capacity as needed.

The preceding discussion outlined the fundamentals of memory operation. The succeeding discussion outlines the process of adding data to the CAT memory. It initially involves the determination of memory contents by employing a READ cycle operation.

In the original single memory plane indicated in B, figure 3–15, assume the 64-core wire is in the "1" state. If negative half-currents are fed to the wires which select this core, the flux in the core would change from +B to −B. This change in flux would induce a measurable current in a third wire passed through this core. However, assuming the original core state to be "0", the negative half-currents would not switch the core; there would, therefore, be no change in B, and no current would then be induced in a third wire passed through this core. As a result, when negative half-currents (READ currents) are passed through the memory core, it is possible to determine whether the state of the core is "1" or "0", depending on measurable currents sensed by a third wire. The third wire, the SENSE winding, is shown in B, figure 3–15. Note that this wire passes through all memory cores on each plane since its sole purpose is to determine the state of any core selected by those channel wires in the designated plane.

The arithmetic scaler temporarily stores the number of counts and adds to it on command. This arithmetic scaler has the same number of binary stages as there are planes in the memory. The SENSE winding from each plane is connected to a companion binary stage in such a way that a SENSE current will set this scaler binary to the "1" state and the absence of SENSE current will leave the companion binary in its "0" state. Resetting all arithmetic scalers to "0" prior to the generation of the READ currents (negative half-currents) results in companion binaries associated with "0" cores remaining "0" and companion binaries associated with "1" cores being switched to "1" states by the SENSE current. Therefore, at the end of a READ cycle, the arithmetic scaler binary states correspond identically to the sensed core states and the number previously in the memory is accurately transferred to the arithmetic scaler. The arithmetic scaler can now receive counts and add them to this stored count number upon a given command.

The READ cycle operation is a destructive one. All the memory cores for the given channel are reset to the "0" state regardless of their original condition. The original state, however, is preserved in the arithmetic scaler.

Since the top of the hysteresis loop (refer to A, figure 3–15) is not actually flat, two side effects must be compensated for during the READ cycle. The first side effect involves the induction of a small current in the SENSE winding in the memory core originally in the "0" state. However, this current is one fifth the amount induced by the "1" state. Amplitude discrimination in sense amplifier circuitry removes this possible source of ambiguity. The second side effect involves the addition of small currents in the SENSE winding by all the

cores along those wires carrying half-currents. To prevent these currents from adding or interfering with the desired signal, the SENSE wire is periodically reversed in direction as it is wound through the cores of the plane. As a result, the small currents tend to cancel out. While the periodic reversal in direction has an additional consequence because a change in core state can induce either a positive or negative current in the SENSE winding (depending on core location), the sense amplifier circuitry is so designed that the scaler binary is switched regardless of current polarity.

As soon as the data from the memory are transferred to the arithmetic scaler, digital pulses whose frequency is determined by the analog input voltage are added to the data now existing in the scaler binaries. A pulse received from the clock oscillator terminates the accumulation of data and initiates a WRITE cycle. The WRITE cycle is the process whereby a new count number is inserted back into the CAT memory. This is essentially the reverse of the READ cycle. That is, the memory cores must be set in a state corresponding to that of their companion binary in the arithmetic scaler. Since the cores are left in the "0" state by the READ cycle, positive half-currents (+1/2 I WRITE currents) for the selected address fed to appropriate channel lines would change all memory cores to the "1" state. In order to keep the core in the "0" state corresponding to a "0" in a companion scaler binary, one more wire (INHIBIT) is passed through each core of the memory plane. The WRITE current like the READ current generates a combined 820 ma (I) through the memory channels. If, while this (I) is being generated, a (−1/2 I) is fed through the INHIBIT winding as shown in C, figure 3–15, the net current through the core becomes (+1/2 I). This is insufficient to switch the core state. Thus, a change in core state is prevented or inhibited as a result of the (−1/2 I) INHIBIT winding current. With the INHIBIT windings connected through appropriate amplifiers to the corresponding binaries in the arithmetic scaler, a "0" arithmetic binary state will generate the INHIBIT current. As a result, the WRITE current will not be able to switch the "0" state core to a "1". Similarly, if the arithmetic binary state is "1", an INHIBIT current will not be generated and the memory core state can then change to "1" during the WRITE cycle. At the end of a WRITE cycle operation, each memory core state corresponds identically to its companion arithmetic scaler binary. Therefore, the count number of the arithmetic scaler has been written back into the CAT memory.

In summary: A READ current is generated and the condition of the selected bit in each memory plane is SENSED. The binary states of the arithmetic scaler are set to correspond to the condition of the memory bits. New data are then added to the count number in the arithmetic scaler. A WRITE current is generated and at the same time an INHIBIT current is supplied, where necessary, so that the final memory core states correspond to the related arithmetic binary states with the new data.

In CAT operation, the channels or addresses are sequentially interrogated for the complete block diagram READ and WRITE cycle timing (see drawing No. WFB8974). The accumulate time duration is determined by the ANALYSIS TIME switch (S2) on the front panel which transmits clock pulses generated from the 51.2 KC Oscillator and Shaper Circuit (PC17L) or external equipment. Each clock pulse initiates a WRITE cycle, an address advance pulse, and a READ cycle of approximately 36 microseconds total duration. At the end of the time alloted to a particular channel or address for the accumulation of new data, the WRITE cycle transfers the data to the appropriate memory core. An address advance pulse is subsequently generated which advances the address to the next channel of cores. Here the READ cycle transfers the information from the new set of cores to the arithmetic scaler. Now, new data can be accumulated until the process repeats itself upon command of the next clock pulse.

3.4.2.8 Second Address Decade Circuits 8507–2 (PC6R, PC8R) (See drawing No. SCD8507–2, Circuit Diagrams.)

The Second Address Decade Circuits are part of the address register complement. The address register also contains two 4 X 5 Memory Decoder Circuits (PC7R, PC9R) and a Scale of Four/Memory Location Circuit (PC10R). As part of the address register, address add driving signals (ADA1) from the Read Cycle Generator Circuit (PC3R) are received by the 1st Second Address Decade Circuit (PC6R) via the Input Section. At the end of an analysis sweep the entire address register is reset to zero.

The 1st Second Address Decade Circuit (PC6R, units) provides the following outputs:

a. A five line decimal code to the 1st 4 X 5 Memory Decoder Circuit (PC7R) selects the memory storage location in a single axis.

b. A four line BCD signal which passes to the external DATA connector (J109) via the Filter

Circuit Board (PC26R). These outputs directly indicate the state of 1st Second Address Decade (PC6R) for external address interpretation.

c. An analog output to drive the X deflection plates of the CRT via the Digital-to-Analog Converter and Deflection Amplifier Circuit (PC11R).

The 2nd Second Address Decade (PC8R, tens) is triggered by a carry pulse from the 1st Second Address Decade Circuit (PC6R, units) which occurs at every tenth input pulse. Each time the 2nd Second Address Decade passes the maximum count (99), it produces an output pulse which is fed to the Scale of Four/Memory Location Circuit (PC10R).

A five line decimal output of the 2nd Second Address Decade Circuit (PC8R) is gated by a four line output of the Scale of Four/Memory Location Circuit (PC10R). This selects one of twenty memory wires in the 2nd 4 X 5 Memory Decoder Circuit (PC9R).

The 2nd Second Address Decade Circuit (PC8R, tens) provides the following outputs:

a. A five line decimal code to the 2nd 4 X 5 Memory Decoder Circuit (PC9R) selects the storage location in a single axis.

b. A four line BCD signal which passes to the external DATA connector (J109) via the Filter Circuit Board (PC26R).

c. An analog output to drive the X deflection plates of the CRT via the Digital-to-Analog Converter and Deflection Amplifier Circuit (PC11R).

3.4.2.9 4 X 5 Memory Decoder Circuits 8506 (PC7R, PC9R) (See drawing No. SCB8506, Circuit Diagrams.)

The two 4 X 5 Memory Decoder Circuits (PC7R, PC9R) provide signals to direct the READ and WRITE currents to the correct horizontal and vertical lines of the CAT memory. These circuits, composed of logic matrices, are used to select memory address coordinates. There are twenty wires in each memory frame producing 400 coordinates.

Input signals to the 1st 4 X 5 Memory Decoder Circuit (PC7R) and the 2nd 4 X 5 Memory Decoder Circuit (PC9R) select only one ground return out of the twenty wires in each axis. Thus, two half-currents of approximately 410 ma coincide at only one memory core out of the 400 coordinates in each memory frame to produce a full switching current of 820 ma.

Since READ half-currents and WRITE half-currents flow through memory cores in opposite directions, bilateral transistors are required for even numbered transistors (Q2 through Q40) of a logic matrix. Bilateral transistors permit current flow from emitter to collector or collector to emitter and in the on state complete a ground for either the WRITE or READ currents. The even numbered bilateral transistors (Q2 through Q40) are biased on when an associated odd numbered 2N404 transistor (Q1 through Q39) is also at the on state. Each 2N404 transistor requires two definite signals to be turned on; a positive-going signal must be applied to the emitter and a negative-going signal must be applied to the base. The 4 X 5 matrixing configuration permits only one odd numbered transistor (Q1 through Q39) to be at the on state at any one time. With the collector connected to the base of the even numbered bilateral transistors (Q2 through Q40), this permits only one of these to be at the on state at any one time.

The "1" bit on both Second Address Decade Circuits (PC6R, PC8R) permit four possible gating conditions on the 1st 4 X 5 Memory Decoder Circuit. These signals are received on the vertical lines and consist of 1 (even), $\overline{1}$ (odd) signals from the 1st Second Address Decade Circuit (PC6R) and 2 (even), $\overline{2}$ (odd) signals from the 2nd Second Address Decade Circuit (PC8R). Negative diode logic selects one of the transistors Q41 through Q44 to provide a complete circuit for a single string of odd numbered transistors (Q1 through Q39), depending on the input signal received. Signals received on the horizontal lines from the 1st Second Address Decade Circuit are indicated on A, B, C, D, E on drawing No. SCB8506 for the 1st 4 X 5 Memory Decoder Circuit (PC7R). By this method of cross-selection, only one even-numbered bilateral transistor (Q2 through Q40) is turned on to complete a half-current path through a single vertical core wire.

The four possible gating conditions (1, $\overline{1}$, 2, $\overline{2}$) on the 2nd 4 X 5 Memory Decoder Circuit (PC9R) are generated by the Scale of Four/Memory Location Circuit (PC10R) for the vertical line signals. Signals on the horizontal lines are received from the 2nd Second Address Decade Circuit (PC8R) and also indicated as A, B, C, D, E on drawing No. SCB8506 for the 2nd 4 X 5 Memory Decoder Circuit (PC9R). This 2nd 4 X 5 Memory Decoder Circuit (PC9R) selects the wire to receive the half-current which is applied to the memory in the horizontal direction.

3.4.2.10 Scale of Four/Memory Location Circuit 8508 (PC10R) (See drawing No. SCB8508, Circuit Diagrams.)

The Scale of Four/Memory Location Circuit contains the last two flip-flop stages in the address register as well as the logic circuitry necessary for memory subgroup selection. The memory subgroup selection is a direct function of the INPUTS IN USE switch (S1).

Positioning the INPUTS IN USE switch (S1) enables memory location gates to receive memory location pulses (ML). The memory location pulses are generated at the Read Cycle Generator Circuit (PC3R) at the beginning of each READ cycle. The ML pulses set the Scale of Four/Memory Location Circuit (PC10R) to a number indicating the selected subgroup. As a result, memory subgroup sequence is established for the number of signal inputs fed to appropriate address quarters in the CAT.

3.4.2.11 Arithmetic Decade Circuits 8512 (PC-14R, PC16R, PC18R, PC20R, PC22R, PC24R) (See drawing No. SCC8512, Circuit Diagrams.)

There are either five or six Arithmetic Decade Circuit Cards in the CAT depending on whether a 10^5-1 or 10^6-1 address count capacity is utilized. The Arithmetic Decade Circuits are capable of adding, subtracting or shifting BCD data.

Each decade circuit is composed of four flip-flops (refer to paragraph 3.3.3 and figure 3–4). A gate at the input of the second flip-flop is operated at the count of eight to prevent the 10th pulse from setting the second flip-flop to the "1" state. This gate is required since four flip-flops can utilize 16 pulses. The fourth flip-flop is reset to the "0" state by the 10th pulse and produces a carry output to the next higher decade. A 1-2-4-8 binary coded decimal (BCD) arrangement is achieved through the use of this configuration.

The Arithmetic Decade Circuits can be enabled to add or subtract when diode gates connected to the inputs of each flip-flop are biased for the desired operation. During the ADD operation, a positive pulse at the ADD BUS input (pin 33) will permit CARRY "0" (INO, pin 41) input pulses to be counted by the decade. The SUB BUS input (pin 31) is disabled by the ADD/SUB switch (S4). During the SUB operation, a positive pulse at the SUB BUS input (pin 31) will permit CARRY "1" (IN1, pin 34) input pulses to be counted and the ADD BUS input (pin 33) will be disabled. Q13 is an inverter (refer to paragraph 3.3.10 and figure 3–11) transistor which operates a gate at the input of the second flip-flop during SUB operation. The diode (AND) gate connected to the input of the last flip-flop from the second and third flip-flops is used to set the last bit for a count of 9 in the SUB mode of operation.

For shift operation of an Arithmetic Decade, additional gates connected to the inputs of each flip-flop are enabled by transfer gate levels from a previous decade. A transfer pulse (XFR PULSE, pin 32) switches the states of any flip-flop that do not correspond to the state of those in the preceding Arithmetic Decade. This is accomplished by the use of the Shift Logic Circuit (PC13R).

3.4.2.12 Shift Logic Circuit 8511 (PC13R) (See drawing No. SCB8511.)

The Shift Logic Circuit is used for digital equipment requiring serial readout of the CAT memory. It utilizes additional gates to the Arithmetic Decade Circuits (PC14R, PC16R, PC18R, PC20R, PC22R, PC24R) for the transfer of gate pulses from preceding flip-flops to succeeding flip-flops.

In shift operation, a free-running multivibrator (refer to paragraph 3.3.1 and figure 3–2) is gated on by an EXT. SHIFT signal (EXT/S, pin 16) on the Shift Logic Circuit Card (PC13R) from the DATA connector (J109). The multivibrator is gated off by the recognition of a number in the most significant decade. BCD signals are sent from an external serial readout control unit to the four SHIFT IN lines. Circuits in the Shift Logic Circuit generate the complement of lines (SHIFT IN 1 pin 24, SHIFT IN 2 pin 28, SHIFT IN 4 pin 31, SHIFT IN 8 pin 38) so that both the original signal number and its complement are available to the first Arithmetic Decade Circuit (PC14R) transfer gates. The application of the EXT. SHIFT signal allows the multivibrator to develop one cycle.

The output of the Shift Logic Circuit is the TRANSFER signal (XFR) which is common to all Arithmetic Decade Circuits. It enters the transfer gates enabled by preceding decade numbers, or in the case of the first Arithmetic Decade Circuit (PC14R) it enters the transfer gates enabled by the numbers complemented by the Shift Logic circuitry. This sets numbers from the preceding decades into the circuits of the succeeding decades.

In summary the shift register operates in the following manner: Transfer gates on each Arithmetic Decade Circuit look at four BCD bits on the preceding decade. This number enables the transfer gate of the decade. The shift trigger is the signal that passes through the open gates and causes the number from the preceding decade to be entered in the succeeding decade.

3.4.2.13 Sense and Inhibit Amplifier Circuits 8513 (PC15R, PC17R, PC19R, PC21R, PC23R, PC25R) (See drawing No. SCB8513, Circuit Diagrams.)

There is one Sense and Inhibit Amplifier Circuit for each Arithmetic Decade Circuit contained in the CAT.

A SENSE signal is generated during the READ portion of the memory cycle if the particular memory core selected is in the "0" state (refer to paragraph 3.4.2.7). The sense amplifier portion of the Sense and Inhibit Amplifier Circuit picks up the small SENSE signal; amplifies it and sets the corresponding bit on its companion Arithmetic Decade binary. Each Sense and Inhibit Amplifier Circuit Card has four sense amplifiers to sense the state of the cores on four memory planes during the READ cycle.

The INHIBIT amplifier of the Sense and Inhibit Amplifier Circuit looks at two signals. One of the signals is the memory core state of a corresponding bit of the companion Arithmetic Decade binary. The second signal is the INHIBIT TRIG. input (pin 37) from the Write Cycle Generator Circuit (PC5R). If the Arithmetic Decade binary contains a "0", then the corresponding INHIBIT amplifier will generate a current to oppose the WRITE current, thereby inhibiting that particular memory core from switching. However, if the Arithmetic Decade bit contains a "1", the corresponding INHIBIT amplifier will not generate a current to oppose the WRITE current and the memory core will be switched to the "1" state.

This card also contains circuitry which is part of the digital-to-analog conversion process. Resistors R11, R22, R33, R44 determine the amount of current which is proportional to the significance of the corresponding binary in the associated Arithmetic Decade. These currents are summed and supplied via the VERT. RANGE switch (S3) to the Digital-to-Analog Converter and Deflection Amplifier Circuit (PC11R) to drive the Y deflection plates of the CRT.

3.4.2.14 Digital-to-Analog Converter and Deflection Amplifier Circuit 8509 (PC11R) (See drawing No. SCB8509, Circuit Diagrams.)

The Digital-to-Analog Converter and Deflection Circuit provides deflection voltages for the CRT and analog output signals to the ANALOG connector (J110) at the CAT rear panel. The analog outputs are available to drive strip-chart or X-Y type plotter equipment.

The current signals supplied by the address register are summed in resistors R34, R36, R37 of the vertical deflection portion of the circuit. The voltage signals are amplified and connected to the X deflection plates of the CRT. The current signals supplied by the arithmetic scaler as selected by the VERT. RANGE switch (S3) are summed by R2, R4, R5 in the horizontal deflection portion of the circuit. These voltage signals, after amplification, are connected to the Y deflection plates of the CRT. In the DISPLAY mode, the 400 addresses of the memory are scanned 16 times a second and the counts stored in each address are displayed on the CRT.

The VERT. RANGE selector switch (S3) selects the three most significant analog out signals from the Sense and Inhibit Amplifier Circuit for display. This occurs in each switch position except TEST (10^2) when only two decades are selected.

3.4.2.15 Selective Centering Circuit 8887 (PC-12R) (See drawing No. SCB8887, Circuit Diagrams.)

The Selective Centering Circuit contains circuitry associated with VERT. POS. controls (R1 through R4) on the CAT front panel. The controls and circuitry enable individual vertical control of the input traces on the CRT.

3.4.2.16 Filter Circuit Board B8833 (PC26R) (See drawing No. B8833, Circuit Diagrams.)

The Filter Circuit Board is a special card which serves as a filter circuit for outputs from other circuit boards in the Computer Section of the CAT. Each of the resistance/capacitance circuits on this card reduces the noise transients which may occur on lines connected to external accessory equipment.

3.4.3 POWER SUPPLIES (See drawings No. B8570, SCB8425, SCB8896, Circuit Diagrams.)

3.4.3.1 Power Supply Filter and Rectifier Circuit No. 2, 8496 (PC23L) (See drawing Nos. SCB8496, B8570, Circuit Diagrams.)

The Power Supply Filter and Rectifier Circuit No. 2 provides the dc voltage for the Zener diode regulated minus 100 volt supply. The minus 100 volt supply is used for the CRT operating circuits and the neon indicator lights. The Zener diode is located on the CAT rear panel. Full wave center tap rectifying circuits are employed. The 115 volt ac voltage from one secondary winding of transformer (T101) is applied to pins 10 and 11, rectified by diodes D1, D2 and is available as minus 160 volts dc at pin 9.

Another secondary winding (20 volts ac) is connected to pins 15 and 16. This ac voltage is rectified by diodes D5 and D6, filtered by capacitor C1 and fed through pin 14 as plus 26 volts dc. The voltage powers the plus 20 volt power supply. Diodes D3 and D4 serve as biasing diodes as the voltage is fed through pin 12 to the plus 20 volt regulating transistor (Q104) on the rear panel.

Ten volts ac is received at pins 17 and 18 and diodes D7 and D8 with associated capacitors C2 and C3 form the plus 13 volt dc supply for the plus 4 volt regulator. This output voltage is available at pin 19.

3.4.3.2 Power Supply Filter and Rectifier Circuit No. 1, 8495 (PC21L) (See drawing No. SCB8495, Circuit Diagrams.)

The Power Supply Filter and Rectifier Circuit No. 1 contains the filter capacitors C1 and C2 for the minus 100 volt dc power supply. Resistors R1, R2 are discharge resistors. Input voltages are fed through pins 8 and 9. Diodes D1 and D2 and capacitor C3 supply minus 26 volts dc through pin 13 to transistors Q101 and Q102 located on the rear panel for the minus 12 and minus 20 volt power supplies. Similarly, diodes D3 and D4 and capacitor C4 supply minus 13 volts dc through pin 20 to Q103 for the minus 4 volt power supply.

3.4.3.3 Voltage Regulator Circuit, —20, —12 8494 (PC20L) (See drawing No. SCB8494.)

The minus 20 and minus 12 Voltage Regulator Circuit consists of amplification stages for the minus 20 volt power transistor (Q101) through pin 11 and minus 12 volt power transistor (Q102) through pin 9.

The minus 20 volt section of the amplifier consists of transistors Q1, Q5, Q6. Transistors Q5, Q6 form a differential stage. The base of Q6 is referenced to minus 4 volts; the base of Q5 through voltage divider R12-R13 is connected to the output of minus 20 volts at pin 1. A variation in the minus 20 volt line is amplified in the differential stage and connected to Q1. Transistor Q1 is an emitter follower (refer to paragraph 3.3.11 and figure 3–12) used as a current amplifier for the minus 20 volt series regulator, transistor Q101.

The amplifier for the 12 volt regulator consists of transistors Q2, Q3, Q4. It operates the same as the minus 20 volt regulator. The base of Q4 is also referenced to minus 4 volts. Because of the ratio of feedback voltage divider R8-R9, an output of minus 12 volts results at the output (pin 2). Transistor Q102 at the rear panel is the series-regulating transistor.

3.4.3.4 —4, +4, +20 Voltage Regulator 8493 (PC19L) (See drawing No. SCB8493.)

The minus 4 volt Regulator Amplifier follows the same pattern as the amplifiers for the minus 20 volt and minus 12 volt regulators. It consists of transistors Q1, Q2, and Q3. The regulator transistor is Q103 on the rear panel. The base of Q3 is referenced to ground and the feedback voltage divider is formed by R4 and R5 connected between plus 4 and minus 4 volts.

The reference for all regulators, diode, DZ1 is contained in the plus 4 volt regulator. The amplifier consists of transistors Q4 and Q5. The base of Q5 is connected to the reference diode and is approximately at ground potentital. The base of Q4 is connected to the feedback voltage divider operating between ground and plus 4 volts. The voltage on this regulator should be adjusted to 3.8 volts for best operation. The series regulator transistor is Q105 on the rear panel. Refer to paragraph 4.1.1 for adjustment procedure.

The amplifier for the plus 20 volt regulator consists of transistors Q6 and Q7 and is identical to the plus 4 volt amplifier except that its feedback voltage divider is connected between ground and plus 20 volts and the base of Q6 is referenced to plus 4 volts. The series regulating transistor is Q104 on the rear panel.

3.4.3.5 Modulator Power Supply 8896 (PC7L) (See drawing No. SCB8896.)

The Modulator Power Supply consists of a conventional dc-to-ac converter operating on a magnetic core saturation principle. The operating voltage is obtained from the minus 12 volt power supply at pin 2. The toroidal core transformer (T1) carries four secondary windings. Positive and negative dc voltages are obtained from these windings through rectification and filtering. The voltages are isolated from ground and from each other so that four independent 4 volt supply voltages for the four modulators make it possible to operate each modulator at a different reference potential.

3.4.3.6 CRT High Voltage Power Supply 8492 (PC18L) (See drawing No. SCB8492.)

The CRT High Voltage Power Supply utilizes minus 100 volts dc input at pin 8 from the Filter and Rectifier Circuit No. 2 (PC23L). A free-running multivibrator circuit (refer to paragraph 3.3.1 and figure 3–2) consisting of transistors

Q2–Q4 produces a square wave pulse train which drives a voltage multiplier type circuit composed of ten diodes (D6 through D15) and ten capacitors (C10 through C19). The output voltage at pin 20 is approximately minus 800 volts. A neon lamp is used to start the multivibrator.

3.5 OPERATION IN THE H AND D MODE

3.5.1 GENERAL

The Computer of Average Transients Models 400A, 400B and 400H have provisions for compiling distribution curves. The distribution curves of time intervals or signal amplitudes can be obtained in the H or D mode of operation. This is accomplished by positioning the PROGRAM switch (S103) at the rear of the cabinet at either the H or D position. At these positions, only a signal to the ADDR. RESET connector (J101) is required. The signal must have an amplitude of not less than 2.5 volts with a rise time of less than 10 microseconds.

3.5.2 H MODE

In the H mode of operation, the first signal applied to connector J101 starts an analysis sweep after the START pushbutton (SL1) is depressed. With the second input pulse, one count is deposited in the channel addressed at that time, and the address register is returned to zero. After 50 microseconds, the CAT will automatically initiate a new analysis sweep. This sweep will continue until a new signal is received at J101. A count will be deposited in the channel addressed and the address register will again be returned to zero. After an additional 50 microseconds, another analysis sweep will start and the operation will continue until terminated by the initiation of a new mode or until no further signals occur. If an interval exceeds the selected analysis time duration as set by the ANALYSIS TIME SEC. switch (S2), the CAT will sweep through all 400 addresses and return to address zero. It will remain at the zero address until a new pulse starts the operation as stated.

In the H mode, the CAT address register is reset to zero when the START pushbutton is depressed. This is accomplished by a trigger address reset signal (TAR) from pin 15 of the External Address Control Circuit Card 8898 (PC12L) (refer to paragraph 3.4.1.10) through the Read and Write Cycle Generator Circuit Cards 8502–2, 8504 (PC3R, PC5R) (refer to paragraphs 3.4.2.4 and 3.4.2.5). This signal is obtained through the PROGRAM switch and affects the gross read trigger (GRTR) to the Auto Data Transfer Circuit Card 8501 (PC2R) (refer to paragraph 3.4.2.3). After the address register is reset to zero, the first signal input pulse into the ADDR. RESET connector starts the H mode process.

The external signal pulse is transmitted to pin 12 of the External Address Control Circuit Card (PC12L). Within the circuitry, an enable storage cycle (ESC) signal is generated and fed to pin 16. The ESC signal out of pin 16 is fed to pin 13 (RESET) of the Delay Control Flip-Flop Circuit Card 8890 (PC13L) (refer to paragraph 3.4.1.5). It is also fed to pin 17 of the Write Cycle Generator Circuit Card (PC5R) and ends the analysis sweep.

The ESC signal from the Write Cycle Generator Circuit (PC5R) is processed through the Read Cycle Generator Circuit Card (PC3R) as a trigger read signal (TRD) and appears at pin 42 as the arithmetic reset signal (ARR). Also out of the Read Generator Cycle circuit at pin 28, a READ pulse to pin 28 of the Memory Current Circuit Card 8503 (PC4R) (refer to paragraph 3.4.2.6) reads out the memory contents into the arithmetic scaler. An arithmetic add 1 signal (ARA1) at pin 39 of the Read Cycle Generator Circuit (PC3R) is fed to the Arithmetic Decade Circuit Cards (PC14R, PC16R, PC18R, PC20R, PC22R, PC24R) (refer to paragraph 3.4.2.11). Then a write signal (WRT) appears at pin 41 of the Write Cycle Generator circuit (PC5R). The write signal is fed to the Memory Current Generator circuit (PC4R) to write the contents of the arithmetic scaler back into the CAT memory.

3.5.3 D MODE

In the D mode of operation, the PROGRAM switch (S103) is set at the D position. The operation of the CAT is exactly the same as the H mode except that the trigger which initiates the analysis sweep is externally connected to the EXT TRIG. connector (J107) at the rear of the cabinet. When the reset of the CAT occurs, a new trigger, minimum of 2 volts with a rise time of less than 10 microseconds, is necessary at J107 to restart analysis sweep operation.

SECTION IV
MAINTENANCE

4.0 GENERAL

Maintenance for the CAT Model 400B is limited to procedures which can be accomplished by personnel in the field. For detailed maintenance and repair MNEMOTRON provides a completely staffed Service Department at 441 Washington Avenue, North Haven, Connecticut.

Paragraph 4.1 indicates internal adjustments for proper CAT operation. Paragraph 4.2 outlines detailed trouble shooting procedure, table 4–1 for the location and solution of operating problems. Figures 4–1, 4–2, 4–3 indicate the location of CAT circuit board cards, test points, and potentiometers for alignment and adjustment.

4.1 INTERNAL ADJUSTMENTS
(See figures 4–1, 4–2, 4–3.)

Internal adjustments for the CAT 400B consist of the establishment of the plus 4 volt reference voltage, the memory current adjustment, and digital-to-analog alignment in the Y and X axes. Equipment necessary for internal adjustment is a multimeter with 20,000 ohms per volt capability such as the Simpson 260 or equivalent.

4.1.1 REFERENCE VOLTAGE (plus 4 volts)

To adjust the CAT reference voltage, proceed as follows:

a. On the Voltage Regulator Circuit Card 8493 (PC19L) connect the multimeter between plus 4 volt fuse (F2) and chassis ground. (See figure 4–1, F2.)

b. Adjust the voltage at potentiometer R7 to read plus 3.8 ~~vac.~~ VDC

c. Reapply glyptal to set adjustment.

4.1.2 MEMORY CURRENT GENERATOR ADJUSTMENT

To adjust the CAT memory current generator, proceed as follows:

a. Apply power to the CAT. Allow adequate time for warm up.

b. On the Memory Current Generator Circuit Card 8503 (PC4R) connect the multimeter between the TIP JACK (figure 4–2) and chassis ground. The voltage reading should be between 12 and 20 volts negative.

c. At the CAT front panel, set the ADD/SUB switch (S4) at ADD.

d. Set the VERT. RANGE switch (S3) at TEST. (10^2 on Models 400, 400H.)

e. Adjust the memory current potentiometer (R9) counterclockwise until some addresses start dropping counts when START pushbutton (SL1) is depressed.

f. Record the voltage reading on the multimeter.

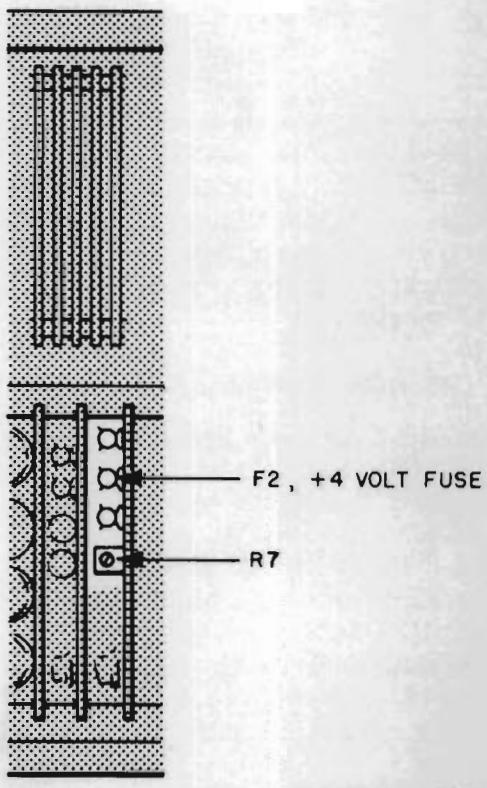


Figure 4–1. Reference Voltage Adjustment Diagram.

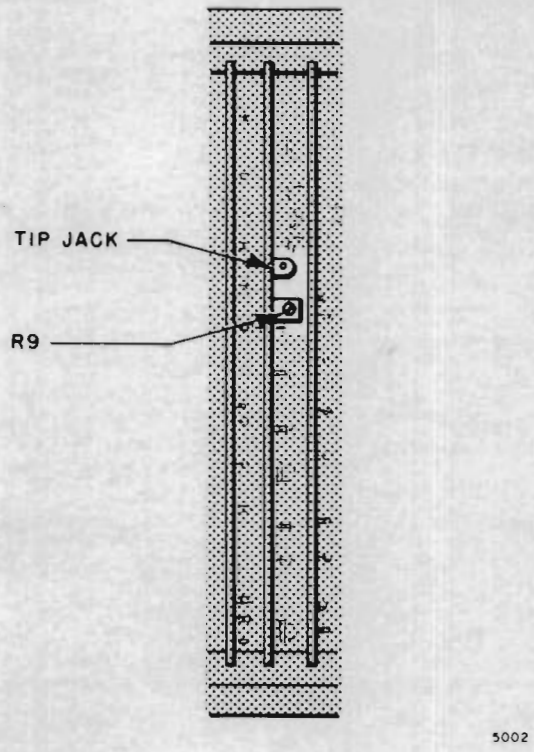


Figure 4–2. Memory Current Adjustment Diagram.

g. Adjust the potentiometer clockwise until counts are added to the memory addresses.

h. Record the voltage reading on the multimeter.

i. Adjust the potentiometer to the midpoint value between the two recorded voltage readings.

j. The setting indicates optimum memory current for CAT operation.

4.1.3 CRT HORIZONTAL ALIGNMENT

To align the CAT trace horizontally, proceed as follows:

a. Remove Selective Centering Circuit Card 8887 (PC12R).

b. Set INPUTS IN USE switch (S1) at 1.

c. Set VERT. RANGE switch (S3) at 10^4.

d. Set ADD/SUB switch (S4) at SUB.

e. Set TEST/USE switch (S5) at USE.

f. Set PLOT/PRINT switch (S6) at PRINT.

g. Depress DISPLAY pushbutton (SL2). Lamp should light.

h. Depress RESET pushbutton (S7). A row of 400 dots should appear on the CRT in some horizontal position.

i. If the row of dots is not parallel to the horizontal lines on the grid window, proceed as follows:

WARNING

Proceed with extreme caution. The CRT high voltage is capable of bodily injury.

1) Lift clip at rear of CRT.

2) Rotate CRT until the row of dots is parallel with a horizontal line.

4.1.4 DIGITAL-TO-ANALOG Y AXIS BALANCE ALIGNMENT

To align the CAT digital-to-analog Y axis balance, proceed as follows:

a. Complete procedures outlined in paragraph 4.1.3.

b. Alternately set the VERT. RANGE switch (S3) between 10^4 and an intermediate position on either side of it. On the CRT note the change in position of the vertical line.

c. At the Digital-to-Analog Converter and Deflection Amplifier Circuit Card 8509 (PC11R), figure 4–3, adjust the Y balance potentiometer (R8) until no deflection appears on CRT when step b is accomplished.

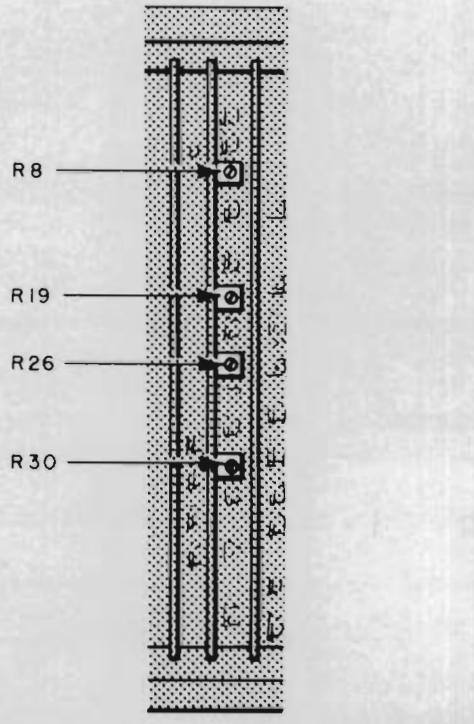


Figure 4–3. CRT Alignment Diagram.

4.1.5 DIGITAL-TO-ANALOG Y AXIS CENTER AND SIZE ALIGNMENT

To align the digital-to-analog Y axis centering and size, proceed as follows:

a. Complete procedures outlined in paragraph 4.1.3.

b. Quickly switch the TEST/USE switch (S5) to TEST and back to USE again. On the CRT note that all channels go to 9-9-9-9-9, etc., to the top line of the graticule.

c. Sharply tap the RESET button (S7). Note that some channels drop out to "0" to the bottom line of the graticule.

d. At the Digital-to-Analog Converter and Deflection Amplifier Circuit Card 8509 (PC11R), adjust the Y size potentiometer (R19), figure 4–3, until the channels which are 9-9-9-9-9, etc., are across the top line of the graticule.

e. Adjust the Y center potentiometer (R26), figure 4–3, until the channels at "0" fall on the bottom line of the graticule.

4.1.6 DIGITAL-TO-ANALOG X AXIS BALANCE ALIGNMENT

To align the digital-to-analog X axis balance, proceed as follows:

a. Complete procedures outlined in paragraph 4.1.3.

b. Vary the HORIZ. SIZE control over its entire range. On the CRT, note a horizontal shift in the position of the left end of the trace.

c. At the Digital-to-Analog Converter and Deflection Circuit Card 8509 (PC11R), adjust the X balance potentiometer (R30), figure 4–3, until no horizontal shift is noted.

4.1.7 TRIGGER/AMPLITUDE DISCRIMINATOR LEVEL ADJUSTMENT (See figure 3–14.)

To adjust the Trigger/Amplitude Discriminator trigger level, proceed as follows:

a. Connect a dual trace oscilloscope, Tektronix Model 502 or equivalent, to both the INPUT jack (J1) and the OUTPUT jack (J2) and chassis ground.

b. Connect the input signal to the INPUT.

c. Adjust the BASELINE potentiometer (R8) fully counterclockwise.

d. Observe oscilloscope for input and output display.

e. Adjust the potentiometer to a position at which the desired portion of the input signal triggers the CAT. This is indicated by an output trigger pulse on the scope.

f. Remove scope and attach cable from OUTPUT jack to EXT TRIG. jack (J107) of the CAT for proper operation of the Trigger/Amplitude Discriminator Circuit Card.

4.2 TROUBLE SHOOTING

4.2.1 GENERAL

Trouble shooting for the Computer of Average Transients (CAT) consists of the identification of malfunctions which cause the suspension of investigative processes; the location of the cause of the malfunction; and subsequent eradication of the malfunction. While superficially this appears to be a simple procedure, extreme care must be taken to accurately identify the trouble with full knowledge that all operating parameters are correct. Before trouble shooting the CAT, perform the following procedures:

a. Apply source voltage to CAT.

b. Make certain all power switches on the CAT, CAT accessories, and ancillary equipment are at the ON position.

c. Make certain all source voltages are of the correct amplitude and type and are actually being applied to the equipment.

d. Check the operating procedures outlined in paragraph 2.3, and the checkout procedures outlined in paragraph 2.4.

e. Check all operating parameters for the experiment under investigation. Make certain accessory and ancillary equipment are operating properly.

f. Check voltage supplies as indicated in table 4–1. Refer to paragraph 4.2.2 for Power Supply Malfunctions.

CAUTION

Before checking voltage supply fuses, make certain all source voltage has been removed. POWER switch (S101) must be at OFF position. Exercise care in the replacement of fuses for correct positioning and prevention of card damage.

g. Check main fuse at CAT rear panel. Check fuses on −20, −12 Voltage Regulator Circuit Card 8494 (PC20L) and −4, +4, +20 Voltage Regulator Circuit Card 8493 (PC19L).

TABLE 4–1 VOLTAGE SUPPLIES

(Equipment required: Simpson Model 260 Multimeter or equivalent)

Voltage Supply	*Test Points (to pin 4)*	*Acceptable Reading*
−12	PC20L-2	−12 to −11
−20	PC20L-1	−20 to −18
−4	PC19L-3	−4 to −3.8
+4	PC19L-6	3.8 (set at factory)
+20	PC19L-7	+20 to +18

h. Perform trouble shooting procedures outlined in the Trouble Shooting Chart, table 4–2. Follow the order indicated proceeding from one remedy to another. If trouble is located before all remedies are performed, trouble shooting analysis can be terminated.

TABLE 4–2 TROUBLE SHOOTING CHART

Malfunction	*Probable Cause*	*Remedy*
1. All control indicator lamps not lighted.	1. Fuses on Power Supply Cards blown.	1. Check and replace fuses if necessary.
	2. −100 volt Zener on CAT rear panel defective.	2. Remove side cover and connect multimeter probe in through the top rear of the CAT to the point of the −100 volt Zener. Connect the other probe to chassis ground. If voltage is low, remove CRT HVPS (High Voltage Power Supply). If reading is still low, remove Control Logic Circuit Card 8500 (PC1R). If reading is still low, remove Write Generator Circuit Card 8504 (PC5R). If still low, replace Zener.
	3. High Voltage Power Supply shorted.	3. Pull CRT High Voltage Power Supply Circuit Card 8492 (PC18L). Replace card if lights go on.
2. No data display on CRT. (CRT filament aglow)	1. CRT control settings incorrect.	1. Check settings for correct positioning. Return for repair if necessary.
	2. CRT HVPS inoperative.	2. Place CRT HVPS Circuit Card on Extender Card and replace in correct position (PC18L). With multimeter connected from pin 20 to ground. Voltage reading should be from −800 to −900 volts. Replace card if reading is unacceptable.
	3. Digital-to-Analog Converter and Deflection Amplifier Circuit Card defective.	3. Replace Digital-to-Analog Converter and Deflection Circuit Card 8509 (PC11R) if necessary.
3. No CRT display. (filament extinguished)	1. CRT defective.	1. Replace CRT.
	2. Primary transformer (T101) inoperative.	2. Check for open winding. Remove and replace transformer if necessary.

TABLE 4–2 TROUBLE SHOOTING CHART (CONT'D)

Malfunction	*Probable Cause*	*Remedy*
4. Display traces cannot be controlled by SIZE or CENTERING knobs.	Digital-to-Analog Converter and Deflection Amplifier Circuit Card.	Replace Digital-to-Analog Converter and Deflection Circuit Card 8509 (PC11R) if necessary.
5. Visual display ripples and appears to "strobe" toward either side of CRT in X or Y axis.	Power Supply Regulator Circuit Cards inoperative.	Remove both Power Supply Circuit Cards 8493, 8494 (PC19L, PC20L) and replace if necessary.
6. With 2 of 4 inputs in use; display cannot be controlled.	Selective Centering Circuit Card inoperative.	Replace Selective Centering Circuit Card 8887 (PC12R) if necessary.
7. With 4 inputs in use; only 3 traces appear. 4th trace is a straight line with no data.	1. Modulator Circuit Cards inoperative. 2. Modulator Gates Circuit Card or Modulator Gate Control Circuit Card inoperative.	1. Swap Modulator Circuit Cards 8897 (PC3L, PC4L, PC5L, PC6L) to locate defective card. Replace appropriate card if necessary. 2. Remove both Modulator Gates Circuit Card 8895 (PC8L) and Modulator Gate Control Circuit Card 8894 (PC9L). Replace if necessary.
8. With 4 inputs in use; only 3 displays on CRT.	Scale of Four/Memory Location Circuit Card inoperative.	Replace Scale of Four/Memory Location Circuit Card 8508 (PC10R) if necessary.
9. With 2 inputs in use; only 1 trace appears. No data on second trace which appears as a straight line.	Same as item 7.	Same as item 7.
10. With 2 inputs in use; only one on CRT.	Same as item 8.	Same as item 8.
11. With either 2 or 4 inputs in use; trace appears on CRT with incorrect data.	Modulator Gate Control Circuit Card or Modulator Gates Circuit Card inoperative.	Same as item 7, step 2.
12. CAT will not deposit counts in memory addresses beyond a specific point on Y axis. Vertical counts fall to bottom of CRT screen before top is reached.	1. VERT SIZE control inoperative; not in CAL position.	1. Check calibration of VERT SIZE control. Reposition if necessary.

TABLE 4–2 TROUBLE SHOOTING CHART (CONT'D)

Malfunction	*Probable Cause*	*Remedy*
12. Continued	2. Arithmetic Decade Circuit Card inoperative.	2. Swap Arithmetic Circuit Cards 8512 (PC14R, PC16R, PC18R, PC20R, PC22R, PC24R) to locate defective card. Replace appropriate card if necessary.
	3. Sense and Inhibit Amplifier Circuit Card inoperative.	3. Swap Sense and Inhibit Amplifier Circuit Cards 8513 (PC15R, PC17R, PC19R, PC21R, PC23R, PC25R) to locate defective card. Replace appropriate card if necessary.
13. Address counts drop out of CRT screen after a number of addresses have swept correctly.	1. Sense and Inhibit Amplifier Circuit Card inoperative.	1. Same as item 12, step 3.
	2. Arithmetic Decade Circuit Card inoperative.	2. Same as item 12, step 2.
14. One or two counts (same amount each time) from every group of ten completely drop out of CRT screen.	1. 1st Second Address Decade Circuit Card inoperative.	1. Swap two Second Address Decade Circuit Cards 8507 (PC6R, PC8R) to locate defective card. Replace appropriate card if necessary.
	2. 4 x 5 Memory Decoder Circuit Card inoperative.	2. Swap 4 x 5 Memory Decoder Circuit Cards 8506 (PC7R, PC9R) to locate defective card. Replace appropriate card if necessary.
15. Complete blocks of ten addresses completely drop out of CRT screen.	2nd Address Decade Circuit Card inoperative.	Same as item 14, step 1.
16. One or uniform group of ten addresses fall to the bottom of CRT screen and remain there.	1st 4 x 5 Memory Decoder Circuit Card inoperative.	Replace 1st 4 x 5 Memory Decoder Circuit Card 8506 (PC7R) if necessary.
17. Uniform group of twenty addresses fall to the bottom of CRT screen and remain there.	2nd 4 x 5 Memory Decoder Circuit Card inoperative.	Replace 2nd 4 x 5 Memory Decoder Circuit Card 8506 (PC9R) if necessary.
18. Blocks of 100 addresses completely disappear.	Scale of Four/Memory Location Circuit Card.	Replace Scale of Four/Memory Location Circuit Card 8508 (PC10R) if necessary.

TABLE 4–2 TROUBLE SHOOTING CHART (CONT'D)

Malfunction	*Probable Cause*	*Remedy*
19. CAT adds or drops counts in memory when not in accumulate mode. (Arithmetic Y axis)	Memory Current Generator Circuit Card inoperative.	Check adjustments on Memory Current Generator Circuit Card 8503 (PC4R). Refer to paragraph 4.1.2 for adjustment procedure.
20. More than one pushbutton indicator lamp is lighted.	1. Fuses. 2. Power Supply Regulator Circuit Cards. 3. Control Logic Circuit Card inoperative.	1. Check fuses and replace if necessary. 2. Check voltages on Power Supply Regulator Circuit Cards 8493, 8494 (PC19L, PC20L). Replace appropriate card if necessary. 3. Replace Control Logic Circuit Card 8500 (PC1R) if necessary.
21. CAT will not go into accumulate mode when START pushbutton is depressed. Light will not go on.	1. Fuses. 2. Control Logic Circuit Card inoperative.	1. Same as item 20, step 1. 2. Same as item 20, step 3.
22. CAT will not switch between accumulate, DISPLAY, and READOUT modes of operation. (CAT is in STOP mode.)	1. Fuses. 2. Control Logic Circuit Card inoperative.	1. Same as item 20, step 1. 2. Same as item 20, step 3.
23. CAT will not go into STOP mode from DISPLAY or READOUT mode.	Control Logic Circuit Card inoperative.	Replace Control Logic Circuit Card 8500 (PC1R) if necessary.
24. CAT will not go into STOP mode from accumulate mode.	Delay Control Flip-Flop Circuit Card or Control Logic Circuit Card inoperative.	Turn CAT off. Turn CAT on; STOP mode should be operative. If so, replace Delay Control Flip-Flop Circuit Card 8890 (PC13L) and check all operating controls for correct positions. If STOP mode is not operative, replace Control Logic Circuit Card 8500 (PC1R).
25. Analysis time cannot be controlled.	1. Scale of 16 Circuit Card inoperative. 2. 51.2 KC Oscillator and Shaper Circuit Card inoperative.	1. Swap Scale of 16 Circuit Cards 8889 (PC14L, PC15L, PC16L) to locate defective card. Replace appropriate card if necessary. 2. Replace 51.2 KC Oscillator and Shaper Circuit Card 8888-2 (PC17L) if necessary.

TABLE 4–2 TROUBLE SHOOTING CHART (CONT'D)

Malfunction	*Probable Cause*	*Remedy*
26. No READOUT mode, READOUT indicator lamp will not light.	Control Logic Circuit Card inoperative.	Same as item 23.
27. No serial readout. Parallel readout OK.	1. Readout equipment inoperative.	1. Check readout equipment. Repair or replace if necessary.
	2. Arithmetic Decade Circuit Cards inoperative.	2. Swap Arithmetic Decade Circuit Cards 8512 (PC14R, PC16R, PC18R, PC20R, PC22R, PC24R) to locate defective card. Replace appropriate card if necesscary.
	3. Sense and Inhibit Amplifier Circuit Cards inoperative.	3. Swap Sense and Inhibit Amplifier Circuit Cards 8513 (PC15R, PC17R, PC19R, PC21R, PC23R, PC25R) to locate defective card. Replace appropriate card if necessary.
	4. Shift Logic Circuit Card inoperative.	4. Replace Shift Logic Circuit Card 8511 (PC13R) if necessary.
28. No parallel readout. (Model 500 Printer, -10^{6})	1. Readout equipment.	1. Same as item 27, step 1.
	2. Arithmetic Decade Circuit Cards inoperative.	2. Same as item 27, step 2.
	3. Sense and Inhibit Amplifier Circuit Cards inoperative.	3. Same as item 27, step 3.
29. CAT does not add or subtract in TEST mode.	1. Sense and Inhibit Amplifier Circuit Cards inoperative.	1. Same as item 27, step 3.
	2. Arithmetic Decade Circuit Cards inoperative.	2. Same as item 27, step 2.
	3. 4 x 5 Memory Decoder Circuit Cards inoperative.	3. Swap two 4 x 5 Memory Decoder Circuit Cards 8506 (PC7R, PC9R) to locate defective card. Replace appropriate card if necessary.
	4. Read Cycle Generator Circuit and Write Cycle Generator Circuit Cards inoperative.	4. Replace both Read Cycle and Write Cycle Generator Cards 8502, 8504 (PC3R, PC5R) if necessary.

TABLE 4–2 TROUBLE SHOOTING CHART (CONT'D)

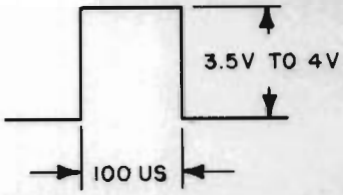
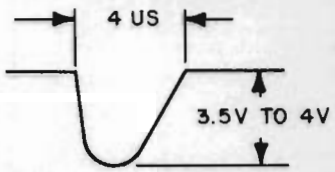
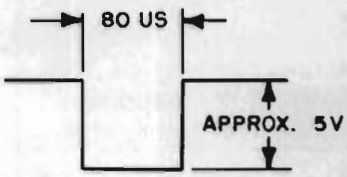
Malfunction	*Probable Cause*	*Remedy*
30. CAT does not add or subtract in the START mode with Trigger switch at INT. (Works in the TEST mode.)	1. Trigger Generator Circuit Card inoperative.	1. Connect oscilloscope at Trigger Generator Circuit Card 8999 (PC10L) between SYSTEM TRIG. Test Point at the top of the card and chassis ground to obtain the following waveshape:  Replace card if necessary.
	2. Delay Control Flip-Flop Circuit Card inoperative.	2. Connect scope at Delay Control Flip-Flop Circuit Card 8890 (PC13L) between CFF-Test Point and chassis ground to obtain the following waveshape:  Replace card if necessary.
	3. Modulator Gates Circuit Card inoperative.	3. Connect scope at Modulator Gates Circuit Card 8894 (PC9L) between CFF+ Test Point at the top of the card and chassis ground to obtain the following waveshape:  Replace card if necessary.
	4. 51.2 KC Oscillator and Shaper Circuit Card inoperative.	4. Replace 51.2 KC Oscillator and Shaper Circuit Card 8888-2 (PC17L) if necessary.
31. CAT does not add or subtract in START mode with Trigger switch at EXT. (Works in TEST mode and at INT.)	Trigger Generator Circuit Card inoperative.	Replace Trigger Generator Circuit Card 8999 (PC10L) if necessary.

TABLE 4–2 TROUBLE SHOOTING CHART (CONT'D)

Malfunction	*Probable Cause*	*Remedy*
32. CAT adds but does not subtract, or subtracts but does not add in TEST mode.	1. Arithmetic Decade Circuit Cards inoperative.	1. Same as item 27, step 2.
	2. Sense and Inhibit Amplifier Circuit Cards inoperative.	2. Same as item 27, step 3.
	3. Read Cycle Generator Circuit and Write Cycle Generator Circuit Cards inoperative.	3. Same as item 29, step 4.
33. CAT adds but does not subtract, or subtracts but does not add in START mode.	1. Arithmetic Decade Circuit Cards inoperative.	1. Same as item 27, step 2.
	2. Sense and Inhibit Amplifier Circuit Cards inoperative.	2. Same as item 27, step 3.
	3. Write Cycle Generator Circuit Card inoperative.	3. Replace Write Cycle Generator Circuit Card 8504 (PC5R) if necessary.
34. No stimulus out of CAT at PROMPT position of STIMULUS switch. (OK at ORD 20 position.)	Trigger Generator Circuit Card inoperative.	Replace Trigger Generator Circuit Card 8999 (PC10L) if necessary.
35. No stimulus out of CAT at ORD 20 position. (OK at PROMPT position.)	Stimulus Pulse Generator Circuit Card inoperative.	Replace Stimulus Pulse Generator Circuit Card 8892-2 (PC11L) if necessary.
36. No stimulus out of CAT at either PROMPT or ORD 20 position.	Stimulus Pulse Generator Circuit Card inoperative.	Same as item 35.
37. PRE ANALYSIS DELAY control inoperative.	Delay Control Flip-Flop Circuit Card inoperative.	Replace Delay Control Flip-Flop Circuit Card 8890 (PC13L) if necessary.
38. No external CAT address advance.	External Address Control Circuit Card inoperative.	Replace External Address Control Circuit Card 8998 (PC12L) if necessary.

TABLE 4–2 TROUBLE SHOOTING CHART (CONT'D)

Malfunction	*Probable Cause*	*Remedy*
39. CAT does not reset with an address reset pulse. (Pulse present and OK at J101.)	External Address Control Circuit or Write Generator Circuit Cards inoperative.	Connect scope at External Address Control Circuit Card between ESC and SOC Test Points and ground to obtain minus 4 volt pulses of 30 millisecond duration. If pulses are present, replace Write Generator Circuit Card 8504 (PC5R). If pulses are not within specification, replace External Address Control Circuit Card 8998 (PC12L).

4.2.2 POWER SUPPLY MALFUNCTIONS

Repetitive failure of the main power fuse, or individual fuses on any voltage regulator card will require isolation of the short circuit or overload causing this breakdown. The Simpson 260 VOM may be used as a milliammeter in series with the main-line supply or in series with the power regulator cards to monitor current drain.

In case of continual failure of the primary fuse, the difficulty may be isolated to the power transformer by moving all power supply cards back from their connectors approximately one inch. This removes all the loading on the secondary windings of the power transformer. (Five power supply cards are located at the rear of the left side card box.) They extend back from the CRT HVPS card in slot 18 at the rear of the left hand side of the CAT.

If the shorting or overload does not occur with power supply cards removed, the cards should be replaced individually while observing the milliammeter. The +4 volt supply should be replaced first because this card furnishes a stable reference source for other supply voltages. Replace cards while the power switch is OFF; turn power ON and wait to observe the effect of each card on the primary fuse. Failure of the primary fuse after the insertion of a card usually indicates that the circuitry of this particular voltage regulator card is defective.

Some voltage regulator cards have a fuse in their output circuits. Failure of any of these fuses indicates an overload beyond the output of the card concerned. The −12 volt fuse, if blown, causes all the front panel pushbutton lights to be illuminated simultaneously. The values of these power supply fuses are printed on each circuit card.

When one of these fuses fails continually, switch CAT power off and move all right hand and left hand circuit cards approximately one inch back from the card connectors. Starting with the +4 volt reference card (−4, +4, +20 Voltage Regulator Card 8493), reconnect each power supply card, turn power on, and observe the effect on the fuse and milliammeter. When power supply cards are installed, continue replacing left hand cards, followed by right hand cards.

4.3 SERVICE INSTRUCTIONS

4.3.1 RETURN OF THE COMPUTER OF AVERAGE TRANSIENTS (CAT)

Merely returning an inoperative CAT does not supply sufficient information for adequate servicing. CAT malfunction charts are included at the rear of the Instruction Manual. Their use enables service personnel to diagnose the problem and quickly repair the unit, or communicate additional trouble areas which might be involved. In addition to the chart, please set down the control positions of your laboratory equipment. Refer to the manufacturer of that equipment, the model number, and name of the equipment. A detailed account of the operational parameters of the instrumentation involved will assure prompt service and marked savings in time and expense.

4.3.2 REPLACEMENT OF PLUG-IN CIRCUIT CARDS

To replace a defective plug-in circuit card, contact the MNEMOTRON Service Department, 441 Washington Avenue, North Haven, Connecticut. Detail the trouble and explain the decision to replace the particular card in question. The MNEMOTRON Service Department will send a replacement card without delay. Retain the defective card until the replacement has been accepted.

4.3.3 SHIPPING INSTRUCTIONS

Before the unit may be returned for service an authorized return tag must be received from the Service Department.

When the unit is prepared for shipment to the factory, it must be securely packed in the original carton with the blue return authorization tag attached to the exterior of the carton. If the original carton has been misplaced, the Service Department will send a new one.

Upon receipt of a new plug-in card the defective card should immediately be returned in the new card container to the Service Department.

SECTION V
COMPONENT BREAKDOWN

5.0 GENERAL

Component breakdown for the Computer of Average Transients (CAT) is outlined in Section V. This section includes disassembly and assembly of replaceable parts. Paragraph 5.1 and figures 5–1 and 5–2 detail CAT circuit card replacement. This can be accomplished at any time during the life of the CAT with a minimum amount of effort.

Paragraphs 5.1.2 through 5.1.7 detail disassembly procedures for CAT components which can be replaced with normal care and effort.

NOTE

CAT users are cautioned to replace no components other than circuit boards for the duration of the original warranty. Details of the warranty are contained in the WARRANTY located in the front of this Instruction Manual. MNEMOTRON Division of Technical Measurement Corporation cannot assume responsibility for damage incurred while replacing CAT components.

5.1 DISASSEMBLY AND ASSEMBLY PROCEDURE

5.1.1 REMOVAL OF SIDE PANELS

To remove side panels, unscrew four captive fasteners and slip off plates.

5.1.2 REMOVAL OF PLUG-IN CIRCUIT CARDS (See figures 5–1, 5–2.)

To remove plug-in circuit cards, hold CAT cabinet firmly and slowly withdraw cards. Make certain not to damage card components or connector pins. Table 5–1 lists the circuit cards, their position in the CAT cabinet, and the card numbers necessary to reorder replacements.

5.1.3 REPLACEMENT OF CATHODE RAY TUBE (3RP–1)

To replace the CAT CRT, proceed as follows:

a. Remove the CRT face panel.
b. Remove the clip at the rear of the CRT.
c. Remove CRT socket.
d. Remove and replace CRT.
e. Reverse steps a through c replacing indicated components.

5.1.4 REPLACEMENT OF —100 VOLT ZENER DIODE (IN1375RA)

To replace the —100 volt Zener, proceed as follows:

a. Remove nut on rear panel.
b. Lift Zener from behind panel top of CAT cabinet.
c. Carefully unsolder two leads.
d. Replace and solder new Zener to leads, being extremely careful to connect correct leads. Use extreme caution not to damage leads or contiguous areas while soldering.
e. Replace rear panel nut.

5.1.5 REPLACEMENT OF —20, —12, —4, +20, +4 VOLT POWER TRANSISTORS (1536, 1535)

To replace power transistor, unscrew component at rear panel and replace new transistor in socket. Replace screws.

5.1.6 REPLACEMENT OF NINE PIN CONNECTORS (Amphenol 126–220)

To replace nine pin connectors, proceed as follows:

a. Remove nut at rear panel and withdraw connector.
b. Unsolder leads and resolder replacement connector. Table 5–2 lists table numbers for pin connections.

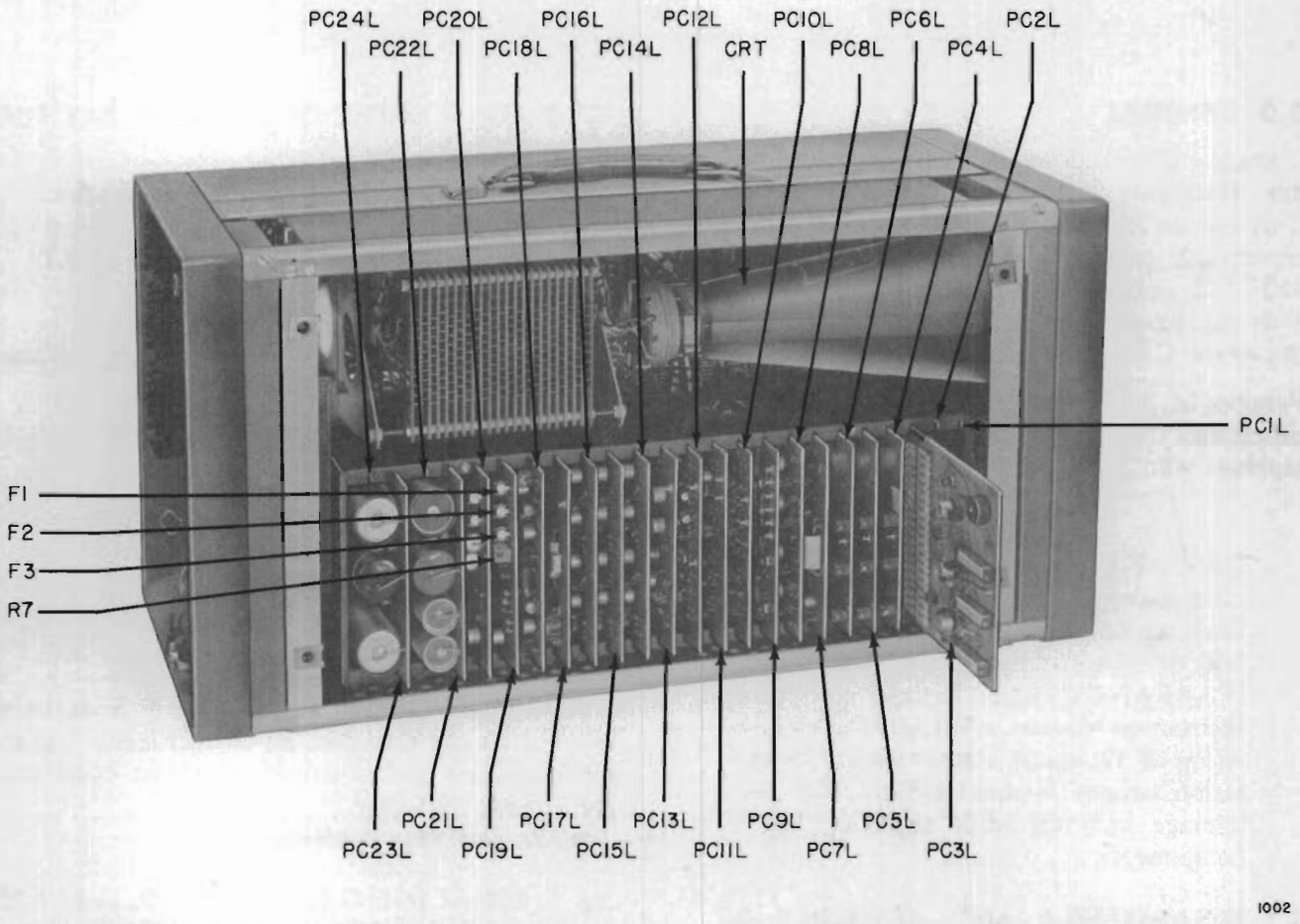


Figure 5–1. Computer of Average Transients, Model 400B (CAT), Left Hand Side.

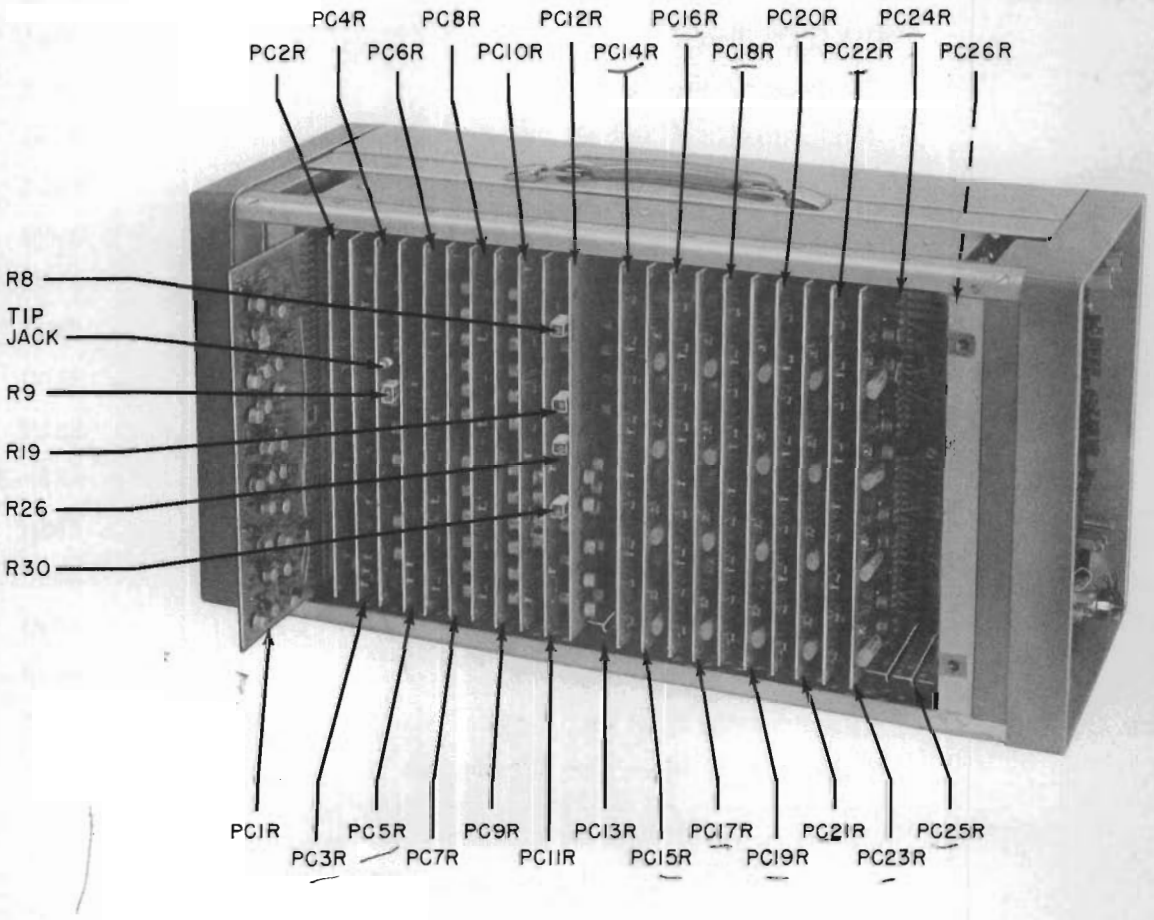


Figure 5–2. Computer of Average Transients, Model 400B (CAT), Right Hand Side.

TABLE 5–1 COMPUTER OF AVERAGE TRANSIENTS (CAT) PLUG-IN CIRCUIT BOARD LIST

Slot No.	*Nomenclature*	*Card No.*
	LEFT HAND SIDE (Figure 5–1)	
2L	Trigger/Amplitude Discriminator	8842
3L, 4L, 5L, 6L	Modulator	8897
3L, 4L, 5L, 6L	500 KC Modulator	8836
3L, 4L, 5L, 6L	Modulator By-Pass	8898
6L	1 KC Oscillator	9081
7L	Modulator Power Supply	8896
8L	Modulator Gate Control	8895
9L	Modulator Gates	8894
10L	Trigger Generator	8999
11L	Stimulus Pulse Generator	8892-2
12L	External Address Control	8998
13L	Delay Control Flip-Flop	8890
14L, 15L, 16L	Scale of 16	8889
17L	51.2 KC Oscillator and Shaper	8888-2
17L	12.8 KC Oscillator and Shaper	8888
18L	CRT High Voltage Power Supply	8492
19L	−4, +4, +20 Voltage Regulator	8493
20L	−20, −12 Voltage Regulator	8494
21L	Power Supply Filter and Rectifier No. 1	8495
23L	Power Supply Filter and Rectifier No. 2	8496
	RIGHT HAND SIDE (Figure 5–2)	
1R	Control Logic	8500
2R	Auto Data Transfer	8501
3R	Read Cycle Generator	8502-2
4R	Memory Current Generator	8503
5R	Write Cycle Generator	8504
6R	1st Second Address Decade	8507-2
7R, 9R	4 x 5 Memory Decoder	8506
8R	2nd Second Address Decade	8507
10R	Scale of Four/Memory Location	8508
11R	Digital-to-Analog Converter and Amplifier	8509

TABLE 5–1 COMPUTER OF AVERAGE TRANSIENTS (CAT) PLUG-IN CIRCUIT BOARD LIST (CONT'D)

Slot No.	*Nomenclature*	*Card No.*
12R	Selective Centering	8887
13R	Shift Logic	8511
14R, 16R, 18R, 20R, 22R, 24R	Arithmetic Decades	8512
15R, 17R, 19R, 21R, 23R, 25R	Sense and Inhibit Amplifiers	8513
26R	Filter Board	B8833

TABLE 5–2 NINE PIN CONNECTOR LIST

Connector No.	*Table No.*
J102	2–1
J104	2–2
J106	2–3
J110	2–5
J111	2–6
J112	2–7

5.1.7 FRONT PANEL COMPONENT REPLACEMENT

To replace components on the front panel, proceed as follows:

a. Detach CRT panel.
b. Remove four cover screws.
c. Drop front panel to expose components mounted on the back side.
d. Remove and replace appropriate component.

5.1.7.1 RESET Pushbutton (S7) and Toggle Switches (S4, S5, S6, S8, S9, S11, S12, S13, S14)

To replace RESET pushbutton and toggle switches, unscrew nut on front panel and replace component.

TABLE 5–3 EQUIPMENT SUPPLIED

Quantity	*Nomenclature*	*Manufacturer*	*Part No.*
1	Card Extender	TMC	580 Type A
1	Card Extender	TMC	580 Type B
1	Line Plug	Belden	I 550
1	3-pin to 2-pin Connector	Hubbel	
4	Input Connector	Cannon	XLR–3–11C
2	9-pin Connector	Amphenol	126–220
2	Allen wrenches (located at the base of the CRT)		

5.1.7.2 Indicator Lamps (SL1, SL2, SL3, SL4)

To replace indicator lamps, proceed as follows:

a. Unscrew nut on front panel.
b. Unsolder four terminals. Mark wire positions.
c. Replace unit and carefully resolder.
d. Replace front panel screw.

5.1.8 EQUIPMENT SUPPLIED

Equipment supplied with a shipment of the Computer of Average Transients (CAT) is detailed in table 5–3.

5.1.9 REPLACEABLE PARTS LIST

Table 5–4 lists the replaceable parts indicated in paragraphs 5.1.3 through 5.1.7 and the equivalent Technical Measurement Corporation stock numbers. The use of the stock numbers will facilitate delivery of the CAT components.

TABLE 5–4 REPLACEABLE PARTS LIST

Nomenclature	*Part No.*	*Stock No.*
Cathode Ray Tube	3RP–1A	780–003
−100 Volt Zener Diode	1N1375RA	280–100
Power Transistor	2N1535	770–201
Power Transistor	2N1536	770–202
Nine Pin Connector	126–220	370–050
Pushbutton (RESET)		670–003
Toggle Switch		690–004
Toggle Switch		690–005
Toggle Switch		690–009
Indicator Lamp		410–007

SECTION VI
APPLICATIONS

6.0 GENERAL

The Computer of Average Transients (CAT) Model 400B provides for widely varied applications of this multi-purpose computer. There are three programs which can be used with the CAT. A particular program is selected by means of the PROGRAM switch (S103) on the rear panel of the CAT. Paragraph 6.1 outlines CAT applications utilizing program C (PROGRAM switch in C position). Paragraphs 6.2 and 6.3 outline CAT applications using program H and D with appropriate PROGRAM switch positions.

6.1 APPLICATIONS OF THE CAT USING PROGRAM C

With the Program switch at the C position, the output of the Modulator Circuit Cards (PC4L, PC5L, PC6L) or the By-Pass Circuit Cards replacement is fed to the arithmetic scaler for accumulation and subsequent storage in the magnetic core memory. This program lends itself to signal averaging as well as various amplitude or time interval counting functions.

6.1.1 SIGNAL AVERAGING

Signal averaging is the largest general area of application of the CAT. It is a data processing technique which is used to increase the signal-to-noise ratio of repetitively occurring data. It achieves an increase in signal-to-noise ratio by serially adding together repetitive signals. The addition cycle is initiated by a synchronizing signal that is related in time (constantly) to the data signal. The coherent portions of the signal (phase-locked to the synchronizing signal) reinforce each other with each successive addition; the noncoherent noise adds out-of-phase and therefore tends to cancel out with each successive addition. The CAT, upon command from the synchronizing signal, samples the data signal at regular intervals and converts each sample into a discrete number of counts proportional to the amplitude of the signal (see figure 6–1). These counts are then stored in a particular address in the magnetic core memory after being added to the number previously stored in this same address. Stated mathematically

$$A(t_i) = \frac{1}{N} \sum_{j=1}^{N} V(t_{ij}) \quad i = 0, 1, 2, 3, \ldots 399$$

where $A(t_i)$ = average signal amplitude at the i^{th} time increment after the synchronization signal

$V(t_{ij})$ = signal amplitude at the i^{th} time increment after the j^{th} synchronization signal

N = total number of signals added together

NOTE

The $\frac{1}{N}$ scale factor must be taken into account in the readout calibration procedure.

Figure 6–2, A illustrates the ongoing data signal masked by noise with the synchronization signals directly below. After each synchronization signal (j), the data signal is sampled at 400 points (i). Each i^{th} sample (ranging from 0 to 399) of the j^{th} signal (ranging from 1 to N) is added to the previous i^{th} sum and stored. Figure 6–2, B illustrates the summation signal as it appears on the CRT of the CAT. The rate at which the data signal is sampled is determined by the setting of the ANALYSIS TIME SEC. switch (S2) on the front panel. Two inversely related factors must be considered in the selection of this switch setting:

1. The duration of the individual response or transient under investigation.

2. The number of samples desired per cycle of the highest frequency component present in the signal response. This may be regarded as horizontal resolution.

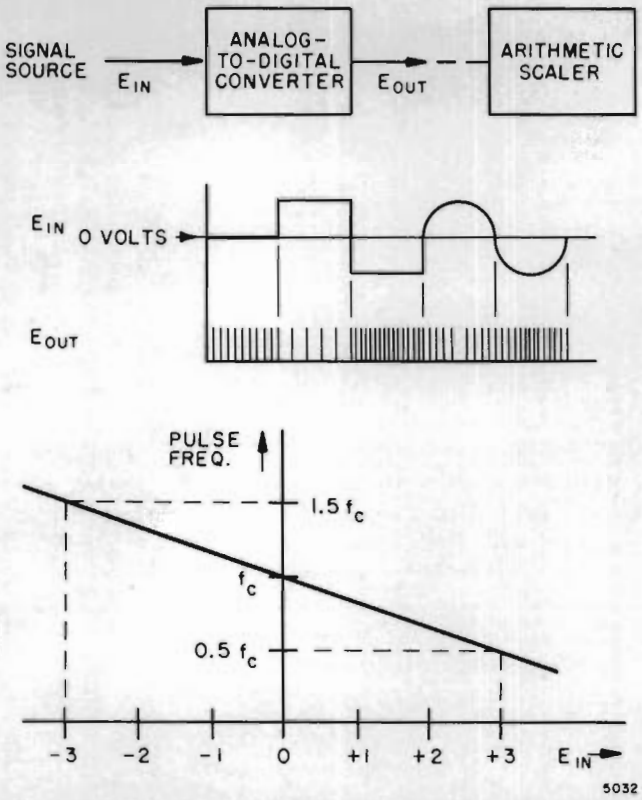


Figure 6–1. CAT Modulator, Analog-to-Digital Converter.

The stated factors are inversely related because of the finite number of addresses in the memory. The addresses may be spread out to cover a large portion of the signal data in time, with the possible loss of some high frequency information, or may be contracted in time to retain fast changes in data over short periods of time. The compromise, when setting the ANALYSIS TIME SEC. switch, must take the stated factors into account.

Sampling rate is also affected by the INPUTS IN USE switch (S1). With only one input in use, the sampling rate is equal to 400 divided by the analysis time. However, 2 or 4 inputs in use divide the sampling rate of each input by additional factors of 2 or 4 respectively. This is a direct result of the fact that each input is sampled consecutively rather than simultaneously.

The CAT operates in three distinct modes; Accumulate, Readout, Display. The readout mode is provided within the computer through the use of ancillary equipment, and can be in either analog or digital form.

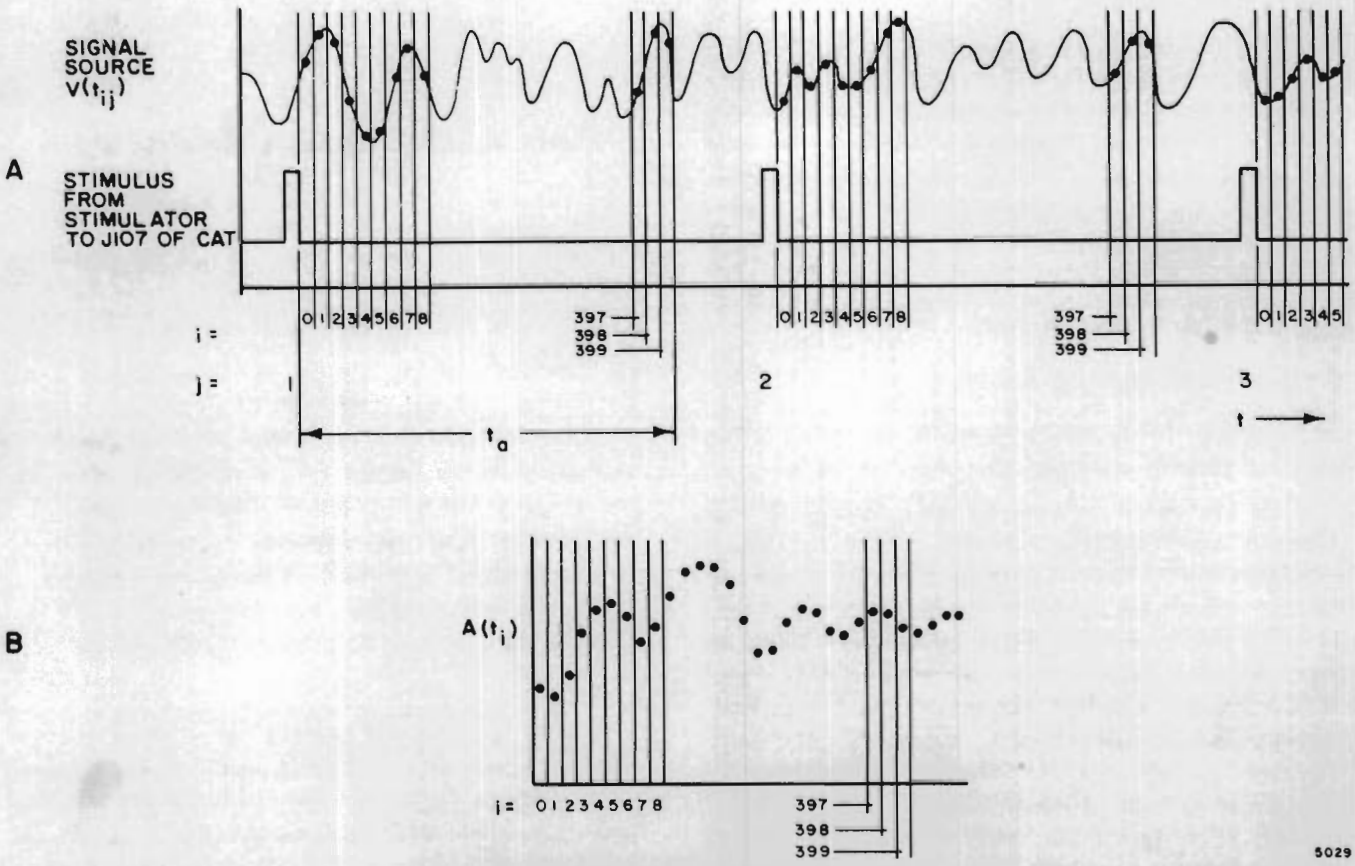


Figure 6–2. CAT Averaging Process.

Should analog representation of the memory contents be required, the operator may parallel the CRT of the CAT with a larger oscilloscope thereby permitting photography of the signal traces (signals are obtained from INPUT GATING connector J102 of the CAT 400B, or from the X-Y test points of the D to A Converter Circuit Card 8509 of the CAT 400, 400A, or 400H). Analog voltages from ANALOG connector J110 may also be fed to an X-Y plotter or strip-chart recorder for a permanent record. Point plots may also be obtained with appropriate equipment.

Should digital representation of the memory contents be required, the operator has several choices. A numerical indication is provided by means of a paper tape printer which prints the address number and the number of counts stored in that address for all 400 addresses. Another means of digital readout for further computer processing is the punched paper tape capability. Standard format for data readout is the IBM Binary Coded Decimal format (BCD). Other codes are available on request. An IBM Typewriter can be paralleled to the punch tape readout for a visual record of the data.

6.1.2 CALIBRATION PROCEDURE

6.1.2.1 General

When using the CAT in the averaging mode of operation (program C), it is sometimes useful to obtain quantitative, in addition to qualitative, results. In either case, input signal levels are usually too low for proper CAT operation. In general, therefore, amplifiers (Tektronix Type 122 or equivalent) are used for amplifying minute voltages to the proper levels for computer processing and should be included as part of the system for calibration purposes. (See figure 6–3.)

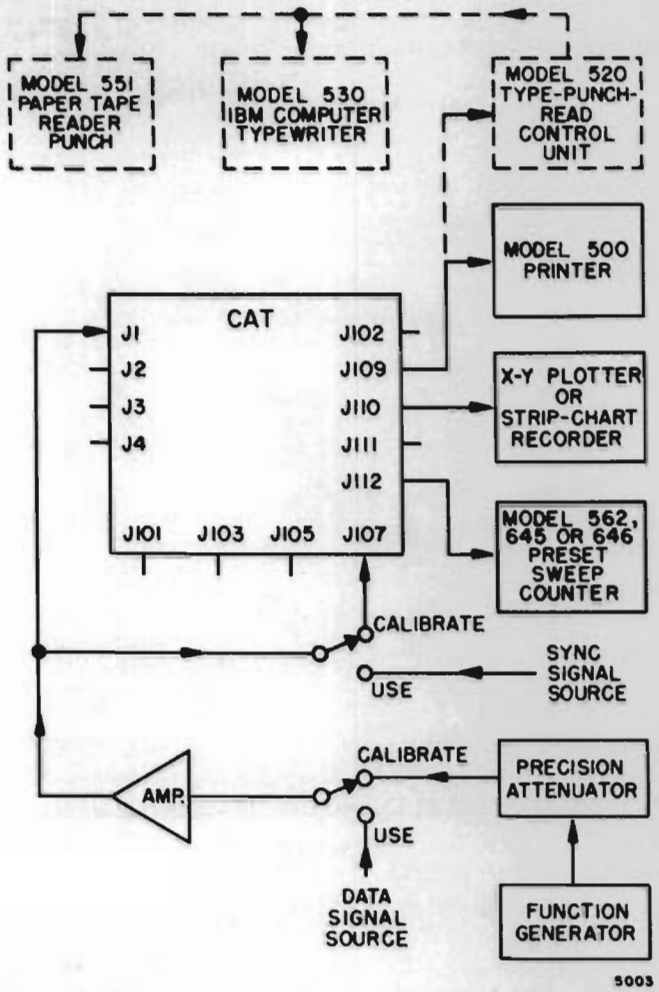


Figure 6–3. Analog Calibration Procedure, Block Diagram.

6.1.2.2 Calibration of Analog Data

To calibrate the readout operation to an X-Y plotter or strip-chart recorder, proceed as follows:

a. Immediately following the plotting of the averaged input data onto the recorder device, apply a calibration voltage of the same order of magnitude as the input signal to the input terminals of the amplifier. Calibration voltage may be obtained from the combination of a General Radio Type 1450 Precision Decade Attenuator and a Hewlett-Packard Model 202A Low Frequency Signal Generator or equivalents. The calibration voltage should be a square wave signal of known amplitude and of such a frequency that two or three full cycles occur within the specific analysis time set at the CAT. If amplification produces a signal greater than 2.0 volts and is a square wave, it can be paralleled with the EXT. TRIG. input (J107) of the CAT to provide a synchronization signal to trigger the CAT. (See figure 6–3.)

NOTE

Specific care must be taken not to change the control settings of the recording device or computer which might affect the plotted amplitude between data run and calibration run. This includes the sensitivity settings of the recording device, and the vertical size, or readout speeds of the CAT.

b. Sum a sufficient number of analysis sweeps with the calibration voltage so that a distinct square wave pattern exists on the CRT screen. Change only the VERT. RANGE switch (S3), if necessary, to produce a clearly-defined calibration voltage waveform.

c. Calculate the average signal input voltage by using the following equation:

$$E_s = \frac{A_s \times E_c \times S_c \times R_s}{A_c \times S_s \times R_c} \quad (1)$$

where E_s = average input signal voltage in volts

E_c = calibration voltage in volts

A_s = amplitude of averaged input signal in inches or centimeters

A_c = amplitude of averaged calibration voltage in inches or centimeters

S_s = numbers of sweeps for input signal

S_c = number of sweeps for calibration voltage

R_s = vertical range switch setting when plotting the input

R_c = vertical range switch setting when plotting the calibration voltage

For example: (See figure 6–4.) The upper trace illustrates an averaged input signal as plotted on the recording device. It represents 100 sweeps (100 accumulations of the input signal) and measures 0.975 inches when plotted out. The VERT. RANGE switch (S3) was at the 10^4 position.

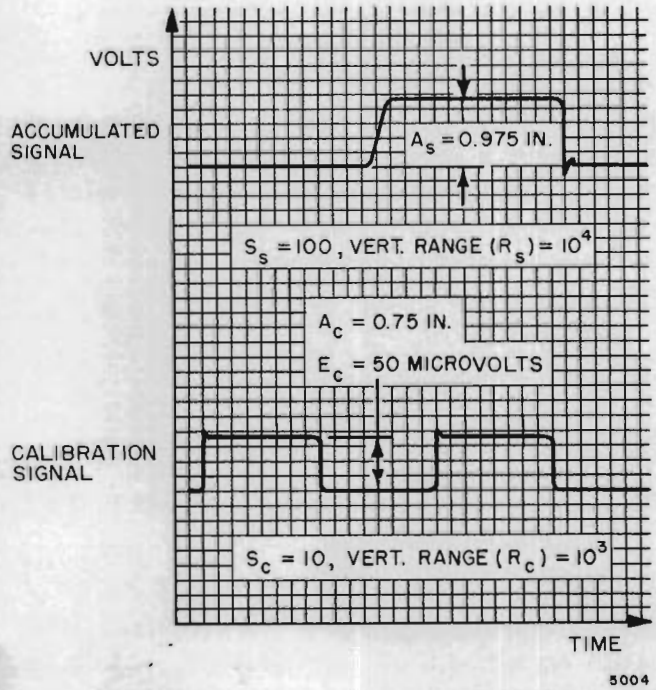


Figure 6–4. Analog Calibration Procedure, Waveforms.

The lower trace illustrates an averaged calibration voltage as plotted on the recording device. The calibration voltage was accumulated for 10 sweeps and was 50 microvolts in amplitude. It measures 0.75 inches when plotted out with the VERT. RANGE switch at the 10^3 position. The averaged input signal is therefore

$$E_s = \frac{0.975 \times 50 \times 10 \times 10{,}000}{0.75 \times 100 \times 1000} = 65$$

microvolts through equation (1). Volts per inch would therefore be

$$\frac{65}{0.975} = 67 \text{ microvolts/inch}$$

6.1.2.3 Calibration of Digital Data

When readout is performed digitally, the CAT may be calibrated with respect to the input voltage which is fed into the CAT. The calibration procedure for digital readout differs from the analog method since the CAT input and not the amplifier input forms the basis for the procedure. If the amplifier gain is fixed and known, the procedure may still be referenced to the input of the amplifier. This is accomplished by multiplying the counts per volt constant by the amplifier gain. Counts per volt may be mathematically determined by

$$\frac{\text{counts}}{\text{volts}} = \frac{(2.5t_a - 0.036)f_cS}{6} \quad (2)$$

where t_a = analysis time in seconds

f_c = modulator center frequency

S = total number of sweeps

The zero volt baseline is calculated from

$$(2.5t_a - 0.036)f_cS \text{ counts} \quad (3)$$

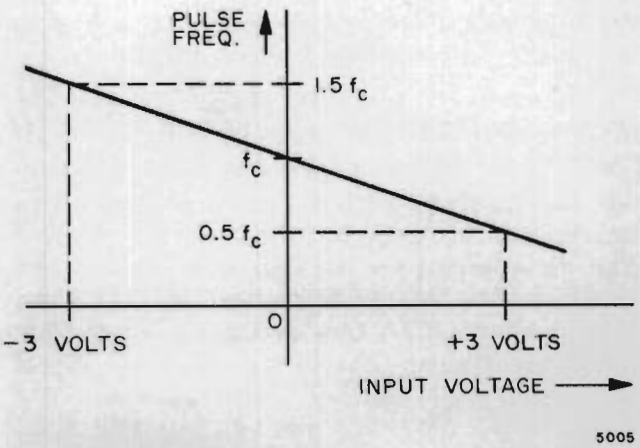


Figure 6–5. Modulator Characteristics.

Derivation of counts/volt equation for calibration procedure:

a. Refer to modulation curve as indicated in figure 6–5.

b. Equation for modulation curve

$$f = me + b$$

where $m = \text{slope} = \frac{\Delta f}{\Delta e}$

b = intersection of f axis

e = instantaneous input voltage

f = instantaneous modulator frequency (number of pulses per second from modulator)

$$\text{therefore } f = -\frac{0.5f_c}{3} e + f_c$$

$$\text{or } f = f_c\left(1 - \frac{e}{6}\right) \quad (1A)$$

f may be regarded as the number of pulses per second coming from the modulator for any value of the input voltage e.

c. The number of counts stored in any one address would be equal to the modulator frequency multiplied by the amount of accumulation time spent in this address, i.e.:

$$n = fS\left(\frac{t_a}{400} - 36 \times 10^{-6}\right)$$

where n = number of counts stored in an address

t_a = ANALYSIS time in seconds

(36×10^{-6}) = memory cycle time

S = total number of sweeps made

d. Upon substitution

$$n = f_c\left(1 - \frac{e}{6}\right)(0.0025t_a - 36 \times 10^{-6})\, S \quad (2A)$$

where e now becomes the average input voltage for S analysis sweeps

e. Solving for e

$$e = 6\left[1 - \frac{n}{(0.0025t_a - 36 \times 10^{-6})}\right] \quad (3A)$$

f. If

$$f_c = KC$$

$$\text{then } e = 6\left[1 - \frac{n}{(2.5t_a - 0.036)f_cS}\right] \quad (4A)$$

g. To obtain a count per volt constant equation (4A) is solved for n yielding

$$n = \frac{(6 - e)(2.5t_a - 0.036)f_cS}{6} \quad (5A)$$

h. Equation (5A) is then differentiated with respect to e to yield the counts per volt constant

$$\frac{dn}{de} = -\frac{(2.5t_a - 0.036)f_cS}{6} \text{ counts/volt} \quad (6A)$$

i. To calculate the rise in the baseline in order to establish a dc zero, e is set equal to zero in equation (5A) resulting in

$(2.5t_a - 0.036)f_c$ counts/analysis sweep

or $(2.5t_a - 0.036)f_cS$ counts for S analysis sweeps

NOTE

These derivations are valid for all modulators having a ± 3 volt input sensitivity giving a ∓ 50% modulation of the center frequency. The polarity is assumed for terminal 2 of the input connector as the reference. Since the input connector is floating above chassis ground, terminal 1 of the input connector can be made common, in which case the above become reversed on the right hand side of the equation.

6.1.3 AVERAGING APPLICATIONS

6.1.3.1 General

Detailed descriptions of averaging applications in the C mode of operation are outlined for EEG responses, ECG signals, and NMR signals. While the specific applications set out in the succeeding paragraphs incorporate historical uses of the CAT, analogous applications utilize identical or similar procedures. Applications Engineers are available for consultations and help for any adaptations that may be required which stem from the uses indicated in this section of the Instruction Manual.

6.1.3.2 Averaging of Evoked Responses from the Brain (EEG)

In the field of electrophysiology there is a particular need for automated data processing techniques due to the tediousness and time required to do such processing manually. This is particularly true in the investigation of evoked potentials from the brain as a result of stimulation to the nervous system.

The evoked potentials or evoked responses are generally quite low in amplitude relative to the continuous cortical activity normally seen in electroencephalographic records. A primary response may sometimes be visible in such records, but secondary and tertiary responses are rarely detected from the raw data.

Response averaging with the CAT is the superimposition or summation of responses. It is an extremely useful technique for the detection of such responses while discriminating against the concurrent background noise. Noise in this instance is defined as electrical activity unrelated to the stimulus-response sequence.

Set-up Procedure — Most EEG apparatus consist of a preamplifier section and a power amplifier section. The power amplifier section is necessary to drive the pens for strip-chart recorders integral to the instrument since the preamplifier output is too low in amplitude. The preamplifier section output is also too low in amplitude (usually 1 to 2 volts or less) and too high in impedance (usually 500K ohms or greater) to serve as a proper input signal into the CAT. As a result, the input signal to the CAT must come from the power amplifier section. However, this signal is usually too high in amplitude (approximately 150 volts), and since the source is a power amplifier, it will usually be a push-pull vacuum tube configuration.

Example: Consider a Grass Model IIID EEG apparatus. To adequately process the EEG responses from approximately 150 volts, 1K ohms impedance output from terminals J9 to J10 of the EEG apparatus to the ±3 volts, 20K ohms impedance necessary for the operation of the CAT, a voltage divider network must be associated with the EEG unit. Figure 6–6 illustrates a typical interface addition. It should be remembered that the CAT has an isolated input and may therefore accept signals from a push-pull source.

The CAT requires an input current of 0.15 milliamperes ($\frac{3 \text{ volts}}{20\text{K ohms}}$). In order to prevent recorder pens from becoming inaccurate due to loading effects, one percent or less of the total available current should be diverted when the voltage is reduced for CAT operation. This means that at least 15 milliamperes should be available at the output from the power amplifiers.

To measure the dynamic impedance of the EEG apparatus at the output terminals:

a. Measure open circuit voltage with an oscilloscope (Grass IIID at pins J9–J10).

b. Insert a variable resistance decade box across the output terminals.

c. Adjust resistance until output voltage is exactly one half of original open circuit reading.

d. Value at decade box is output impedance at EEG apparatus.

To solve for the typical circuitry indicated in figure 6–6, proceed as follows: Since R_1 and R_2 form the voltage divider, then

$$\frac{R_1 + R_2'}{R_2'} = \frac{150 \text{ volts}}{3 \text{ volts}} = 50$$

where R_1 = first resistor of voltage divider

R_2' = equivalent parallel resistance of second resistor of voltage divider (R_2) and 20K ohms impedance of CAT (R_{CAT}) ($K = 10^3$)

$$\text{therefore } R_1 = 49\, R_2' \qquad (1B)$$

Since current diverted cannot exceed 1% of the available EEG apparatus current

$$\frac{R_1 + R_2'}{R_{EEG}} = \frac{100}{1} \qquad (2B)$$

$R_1 + R_2'$ = $100\, R_{EEG} = 100 \times 1K = 100K =$ total resistance of voltage divider network (including CAT)

Substituting equation (1B) in equation (2B)

$$49R_2' + R_2' = 100K$$

$$50R_2' = 100K \qquad (3B)$$

$$\therefore \quad R_2' = 2K$$

The equivalent resistance of the parallel leg of the divider circuit is

$$R_2' = \frac{R_2 \times 20K}{R_2 + 20K} \qquad (4B)$$

substituting (3B) in (4B) we obtain

$$2K = \frac{R_2 \times 20K}{R_2 + 20K}$$

$$2KR_2 + 40K^2 = R_2 \times 20K$$

$$\text{or} \quad 18KR_2 = 40K^2$$

$$\text{or} \quad R_2 = 2.2K$$

R_1 may also be found by substituting (3B) in (1B)

$$R_1 = 49R_2 = 49 \times 2K$$

$$R_1 \approx 100K$$

Should R_1 or R_2 become a negative value, an amplifier rather than a voltage divider configuration is necessary.

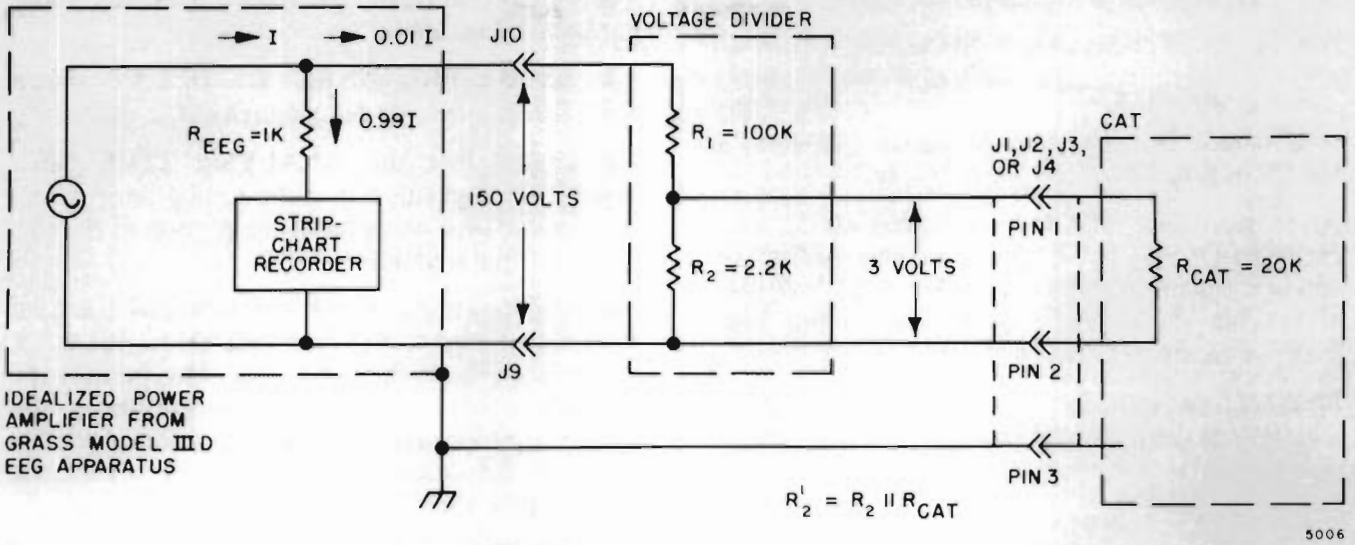


Figure 6–6. EEG Interface Configuration, Circuit Diagram.

External Stimulation — When the CAT is to be triggered by an external pulse, proceed as follows (see figure 6–7):

a. Set up the CAT as previously stated, with the number of inputs (see figure 6–6) from the power amplifier section connected to the input connectors J1 through J4.

b. Set the INPUTS IN USE switch at the position corresponding to the number of inputs in use.

c. Connect the external stimulator (with the proper polarity) to the EXT. TRIG. BNC jack (J107) at the rear of the CAT. If the output of the stimulator is in the order of 50 volts with high impedance (as is the case with the Grass Stimulator), an interface match can be accomplished as shown in figure 6–7. This consists of a speed-up capacitor across the series resistor of a voltage divider network. Adjust indicated potentiometer until analysis sweep begins.

d. Connect DATA connector (J109) to digital readout devices or Series 600 Accessory Cabinet as required.

e. Connect ANALOG connector (J110) to plotting device as required.

f. Connect ACCESSORY connector (J112) to MNEMOTRON Model 562, 645 or 646 Preset Sweep Counter as required.

g. Set PRE ANALYSIS DELAY control (S10/R6) at 0.

h. Set TRIGGER switch (S8) at EXT.

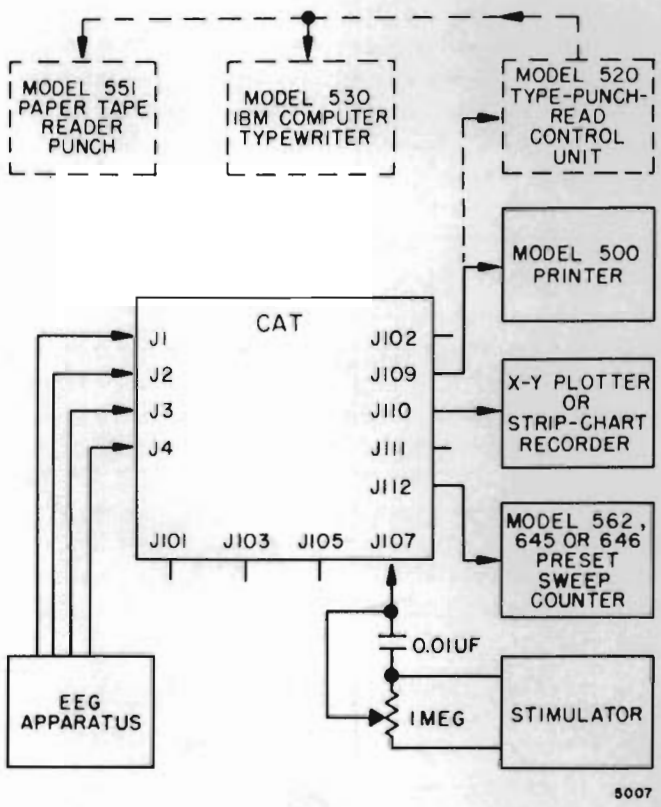


Figure 6–7. External Stimulation in EEG Application, Block Diagram with Interface Circuitry.

i. Set ANALYSIS TIME SEC. switch (S2) at desired time setting.

j. Set INPUTS switches (S11, S12, S13, S14) at applicable positions.

k. Set ADD/SUB switch (S4) at ADD.

l. Set TEST/USE switch (S5) at use.

m. Set PLOT/PRINT switch (S6) as required.

n. Check that PROGRAM switch (S103) is at the C position.

After depressing START pushbutton (SL1), each external stimulus pulse which initiates patient reaction starts an analysis sweep. The CAT will then accumulate the evoked responses for on-line summation (averaging). (See A, figure 6–8.)

External Stimulation (Pre Analysis Delay) — When a delay is desired from the time the external stimulation occurs to the time the analysis sweep starts, proceed as follows:

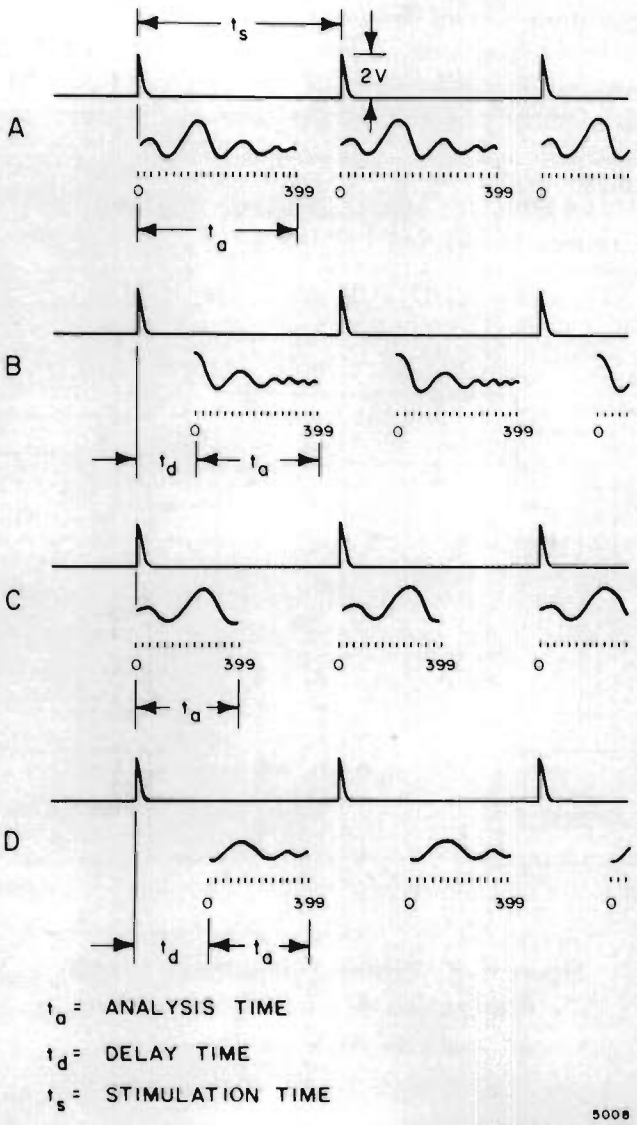


Figure 6–8. External Stimulation in EEG Application, Waveforms.

a. Follow the set-up procedure indicated under *External Stimulation.*

b. Set the PRE ANALYSIS DELAY switch (S10/R6) at a desired delay increment.

c. Check that the ANALYSIS TIME SEC. switch (S2) is positioned at the setting most favorable for the time duration of the portion of the signal under investigation.

After depressing the START pushbutton, the time delay set at step b. will transpire before the CAT accumulates the evoked responses. This permits the investigator to sample the further portion of the evoked response signal since that portion of the response occurring during the delay time will not be accumulated. (See B, figure 6–8.)

External Stimulation (Analysis Time Control) — When a change in the duration of the analysis time for the 400 addresses of the CAT is desired, proceed as follows:

a. Follow the set-up procedure indicated under *External Stimulation.*

b. Set the ANALYSIS TIME SEC. switch (S2) at a position which provides a shorter time duration than one which will encompass the entire evoked response.

After depressing the START pushbutton, the time duration for the 400 addresses will only encompass the forward portion of the evoked response signal since the complete response must utilize a longer analysis time duration. This provides the investigator with better resolution over a smaller forward section of the evoked response. (See C, figure 6–8).

External Stimulation (Pre Analysis Delay/Analysis Time Control) — When a delay from the time the external stimulation occurs and a change in the duration of the analysis time is desired, proceed as follows:

a. Follow the set-up procedure indicated under *External Stimulation.*

b. Set the PRE ANALYSIS DELAY switch at a desired delay increment.

c. Set the ANALYSIS TIME SEC. switch at a position which provides a shorter time duration than one which will encompass the entire evoked response.

After depressing the START pushbutton, the time delay will start the analysis sweep at a point in time after the evoked response signal has begun. It will also utilize the 400 memory addresses for a smaller

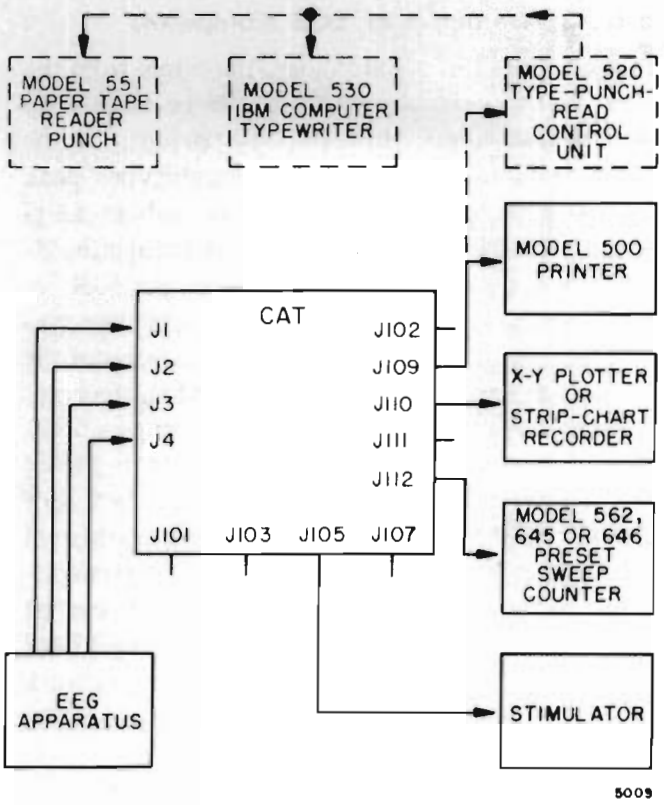


Figure 6–9. Internal Stimulation in EEG Application, Block Diagram.

portion of the signal after the delay. This provides the investigator with better resolution for any desired portion of the evoked response for clearer definition of response characteristics. (See D, figure 6–8.)

Internal Stimulation (Address 0) — When external stimulation equipment is triggered by the CAT, proceed as follows: (See figure 6–9.)

a. Follow the set-up procedure as indicated under *External Stimulation.*

b. Connect the STIM. connector (J105) to the external stimulator.

c. Set the TRIGGER switch (S8) at INT.

d. Depress the START pushbutton (SL1) for CAT operation.

At the start of CAT operation, a stimulus pulse will be transmitted to external stimulation equipment. Patient evoked responses will be summed (averaged) 100 microseconds after initiation of sweep and repetitively 100 microseconds after each analysis sweep. (See A, figure 6–10.)

Internal Stimulation (Address 20) — When external stimulation equipment is triggered by the CAT and a delay is desired between the time the analysis sweep begins and the stimulus is applied, proceed as follows:

a. Follow the set-up procedure indicated under *Internal Stimulation.*

b. Set the STIMULUS switch (S9) at ORD. 20.

c. Depress the START pushbutton for CAT operation.

At the start of CAT operation the analysis sweep will begin. However, the stimulus pulse will not be transmitted to external stimulation equipment until the 20th address has been reached. Patient evoked responses will be summed (averaged) starting at the 0 address. This provides time for the investigation of anticipatory responses to the applied stimulus. (See B, figure 6–10.)

Subtract Operation — When operation of the CAT requires the subtraction of input signals from the data already stored in the memory, proceed as follows:

a. Follow the set-up procedure indicated under *External Stimulation.*

b. Set the ADD/SUB switch (S4) at SUB.

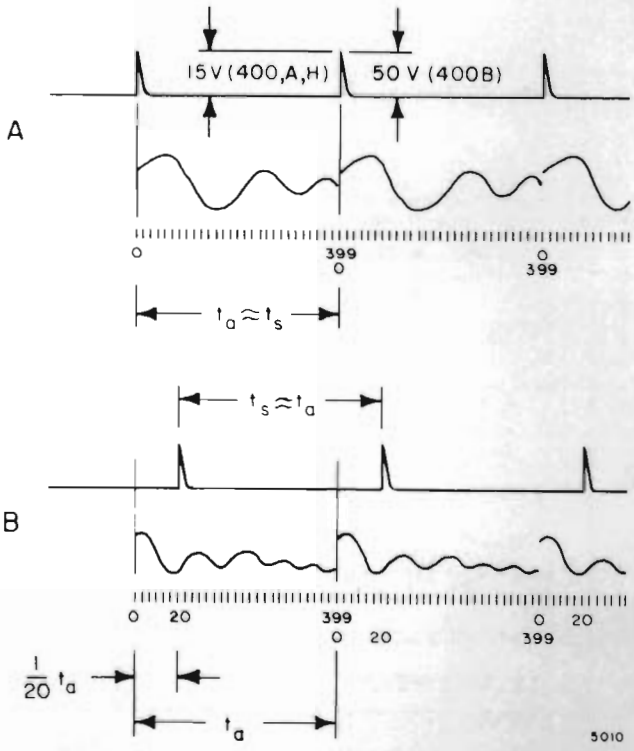


Figure 6–10. Internal Stimulation in EEG Application, Waveforms.

c. Set the TRIGGER switch (S8) at either EXT. or INT. as required. After depressing the START pushbutton, the CAT will subtract the input signals from the data stored in the CAT memory. This will permit the accumulation and subtraction of an equal number of analysis sweeps for signal comparison.

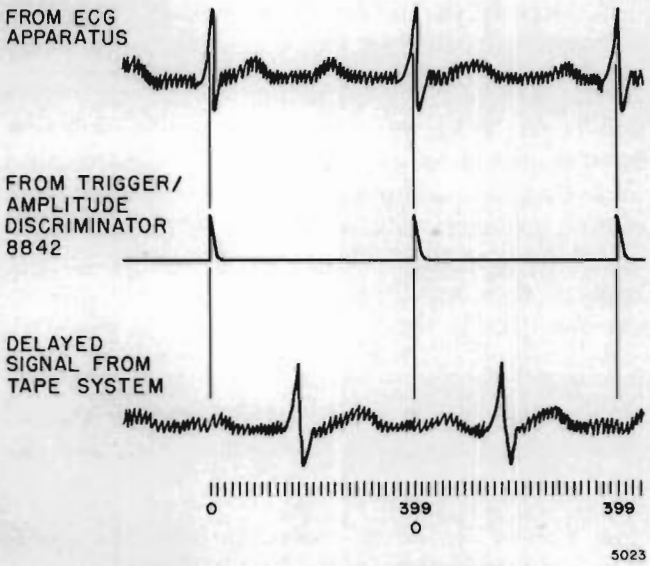


Figure 6–11. Averaging of ECG Complexes, Waveforms.

6.1.3.3 Averaging of ECG Complexes

In the field of electrocardiology, the signal from the heart or ECG signal may sometimes be masked by background noise. However, the R-wave of the heart beat usually provides an unambiguous peak and is immediately recognizable as such in ECG signal processing (see figure 6–11). Although the R-wave peak is specifically determined, the R-R interval varies from beat to beat and a repetitive synchronization signal for the averaging process of the entire complex cannot be obtained. When the complete ECG signal is required for averaging, a delay technique must be provided to acquire a triggering signal locked in time to each ECG complex. For this purpose a MNEMOTRON magnetic tape system is used to create a delay through use of separate record and reproduce heads. The CAT 400B can be provided with a Trigger/Amplitude Discriminator Circuit Card 8842 as an accessory which will work in conjunction with the magnetic tape system.

For averaging ECG data utilizing the CAT, proceed as follows (see figure 6–12):

a. Insert Trigger/Amplitude Discriminator Circuit Card 8842 in slot 2L on left hand side of CAT.

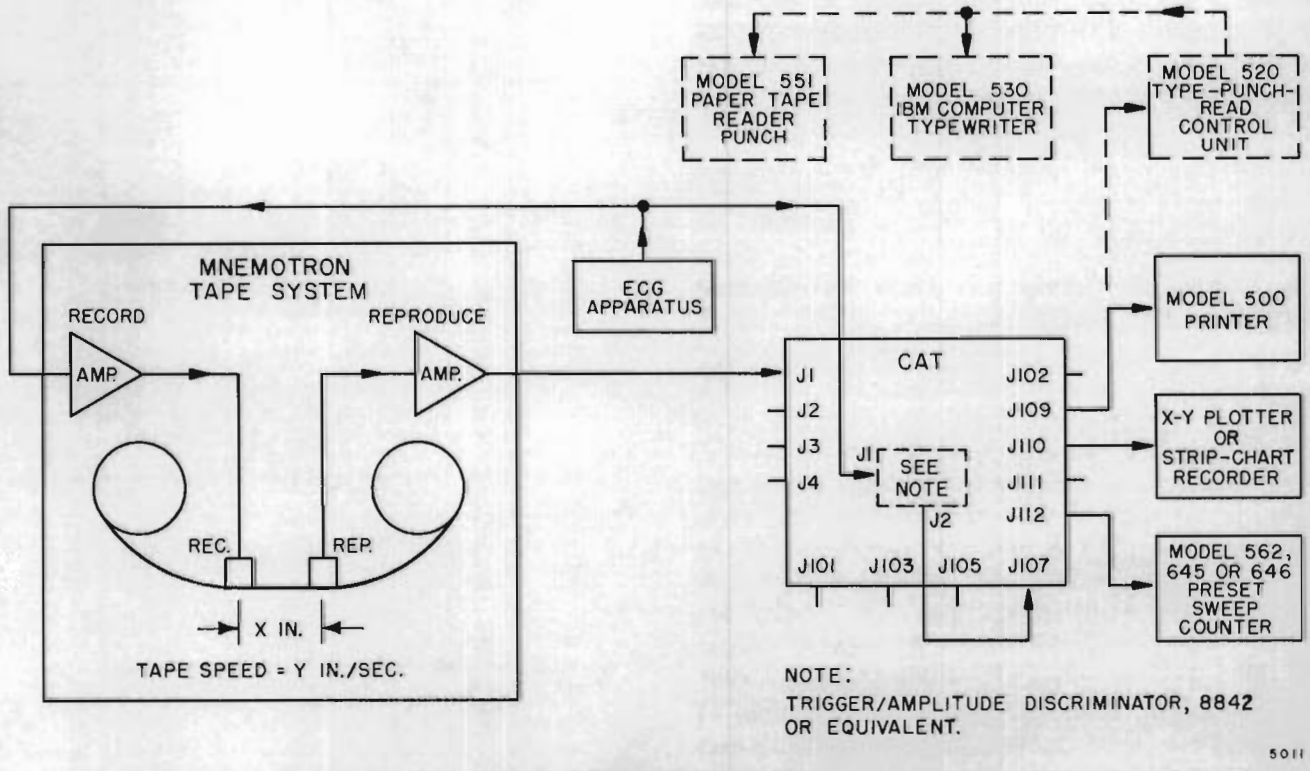


Figure 6–12. ECG Application, Block Diagram.

b. Connect the properly amplified output signal of the ECG apparatus to the INPUT jack (J1) of the Trigger/Amplitude Discriminator Circuit Card (2L), or to the input of any Schmitt trigger circuit. Connect the output of the Trigger/Amplitude Discriminator Card (J2) (or the output of the Schmitt trigger circuit) to the EXT TRIG. input (J107) of the CAT.

c. Connect the same output signal of the ECG apparatus to the input connector of a magnetic tape recording system having separate record and reproduce heads, and having the feature of simultaneously reproducing while recording.

d. Connect the output of the magnetic tape system to the first input connector of the CAT (J1).

e. Set the TRIGGER switch (S8) to EXT.

After depressing the START pushbutton and starting the tape system, an averaging process will take place which will include the complete P–Q–R–S–T complex of the electrocardiogram. This is accomplished through the use of the magnetic tape delay $\frac{X}{Y}$ where X is the distance between the record and reproduce heads in inches and Y is the speed of the tape device in inches per second. The delay will be determined in seconds through the above equation. When simultaneous or subsequent X–Y plotting is desired, connect the analog output of the CAT from OUTPUT connector (J110) at the rear of the CAT to the input of an X–Y plotter. When calibration of the plotting device is necessary, follow the procedure outlined in paragraph 6.1.2.

6.1.3.4 Averaging NMR Signals

In the field of Nuclear Magnetic Resonance, trace quantities or samples of extremely high dilution are sometimes masked by background noise having a Gaussian random distribution. To detect resonance peaks, the CAT averages successive sweeps through the spectrum and the averaged results are plotted on associated X–Y instrumentation. The reference resonance peak is created by the inclusion of a known substance, usually tetramethylesilane (TMS). If the spectrum of the sample to be measured succeeds the spectrum of the reference substance, averaging with the CAT is easily accomplished. If the TMS reference line does not immediately precede that portion of the spectrum, special techniques are required. One method is to use a sideband technique through use of an audio oscillator, adjusted to place the sidebanded TMS line just before the area of interest in the spectrum. The audio oscillator should be shut off immediately after triggering occurs in order to prevent overlapping spectra.

For averaging data processing utilizing the CAT, proceed as follows (see figure 6–13):

a. Connect the output of the NMR detector to the INPUT jack (J1) of the Trigger/Amplitude Discriminator Circuit Card 8842 (2L) on the left hand side of the CAT. Any Schmitt trigger circuit may be used if desired.

b. Adjust the Trigger/Amplitude Discriminator for the reference peak amplitude. Refer to paragraph 4.1.7 for proper adjustment procedure.

c. Connect the same output to the input of the CAT (J1).

d. Connect the output of the Trigger/Amplitude Discriminator OUTPUT jack (J2) to the EXT TRIG. BNC connector (J107) on the rear of the CAT.

e. Connect the analog output of the CAT from the ANALOG connector (J110) at the rear of the CAT to the input of the associated X–Y plotter. Calibration is necessary. Follow the procedure outlined in paragraph 6.1.2.

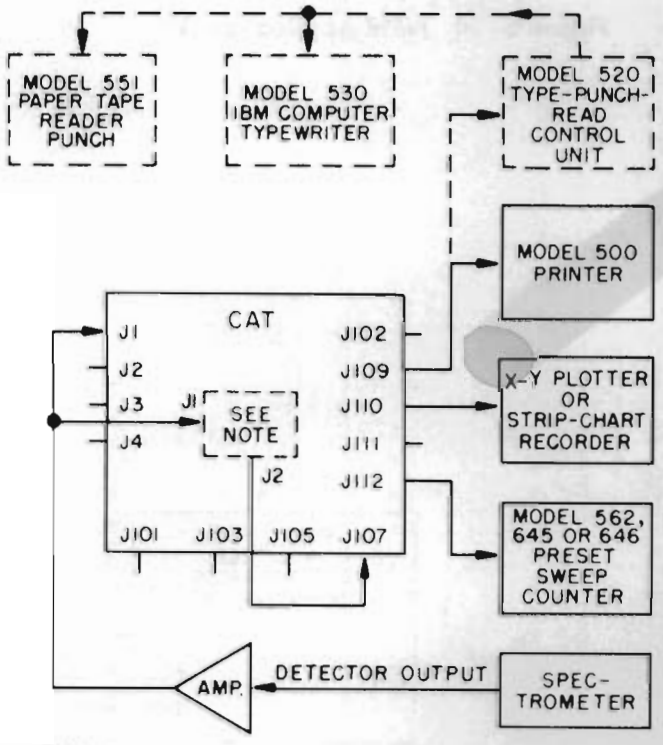


Figure 6–13. NMR Application, Block Diagram.

After depressing the START pushbutton, the complete NMR spectrum will occupy the 400 addresses of the CAT (see figure 6–14). When the analysis sweep has been terminated, the spectrometer controls must be repositioned to start the next sweep. Automatic repositioning can be accomplished through relays which operate the spectrometer controls. The relays are controlled by limit switches at the beginning and end points of the portion of the spectrum of interest.

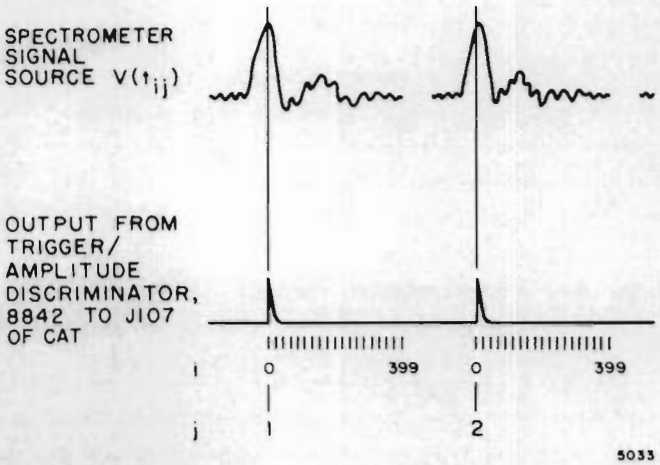


Figure 6–14. NMR Application, Waveforms.

6.1.4 SEQUENTIAL AMPLITUDE OR TIME INTERVAL COUNTING FUNCTIONS USING PROGRAM C

6.1.4.1 General

As a result of its unique averaging capabilities, the CAT is ideal for use as a 400 channel counting device. Provisions for precisely controlling the number of counts stored in each address can be accomplished by means of external shaping devices. One such shaping device is the MNEMOTRON Model 605 Amplitude Discriminator which has been specifically designed for operation with the Computer of Average Transients. Using program C (with the PROGRAM switch S103 at the C position) the CAT is capable of providing on-line computation reflecting any change in signal amplitude or time interval of sequential events.

6.1.4.2 Stimulus Related Time Interval Sequence

To record the interval between successive events after subject stimulation, the CAT has the capability of producing the data in an interval curve which can be viewed on the CRT or transmitted to ancillary readout equipment. An example of the sequential stimulus related time interval sequence is the study of nerve action potentials. To obtain the stated curve, proceed as follows (see figure 6–15):

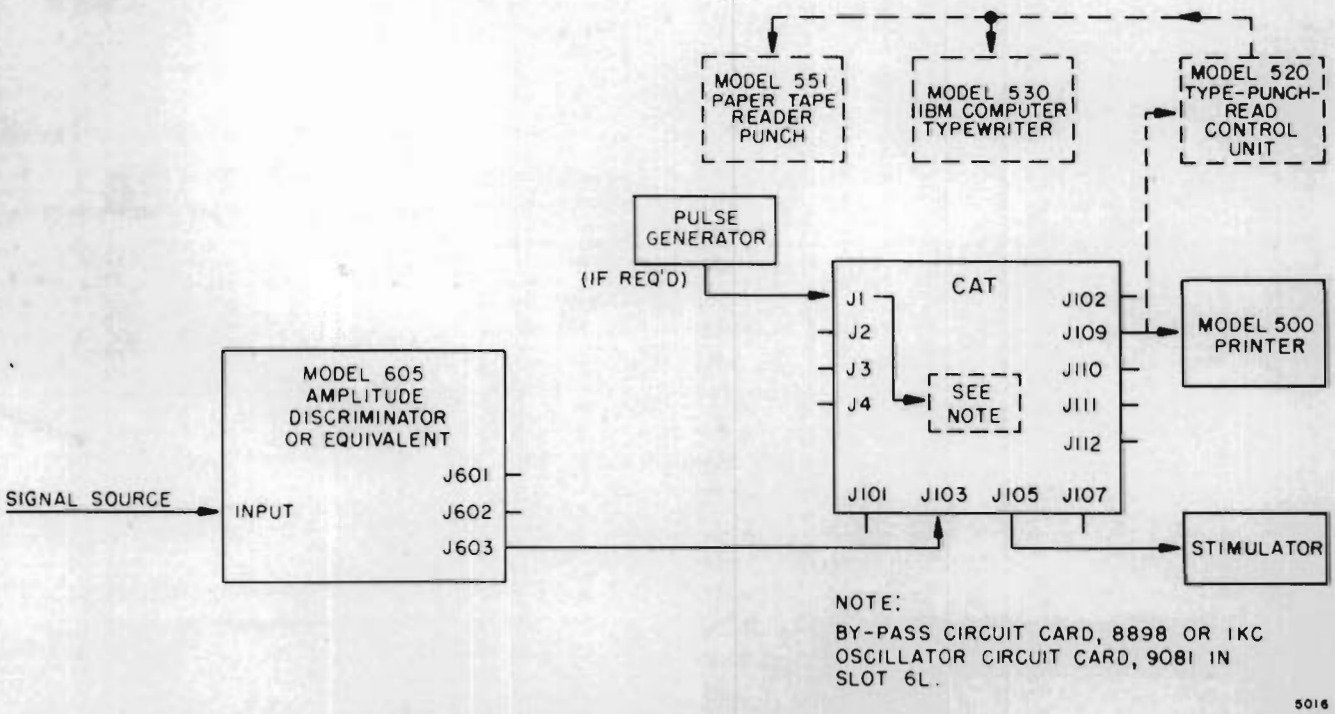


Figure 6–15. Stimulus Related Time Interval Sequence, Block Diagram.

a. Remove the Modulator Circuit Card 6L on the left hand side of the CAT.

b. Insert a 1 KC Oscillator Circuit Card 9081 in slot 6L, or

c. Insert a Modulator By-Pass Circuit Card 8898 in slot 6L when an external pulse generator (Tektronix 162 or equivalent) is used to feed pulses of at least +1 volt to the input of the CAT (J1).

d. Connect the output of the signals under investigation to the INPUT connector of the MNEMOTRON Model 605 Amplitude Discriminator or other shaping circuit.

e. Set the BASELINE vernier of the Model 605 Amplitude Discriminator to a desired amplitude level which will discriminate against unwanted noise signals.

f. Connect the output of Model 605 via EXT. ADD. ADV. jack (J603) or a +2 volts, 10 microseconds rise time signal from shaping circuit to ADDR. ADV. connector (J103) at the rear of the CAT.

g. Connect the stimulus pulse from the STIM. connector (J105) on the CAT to an external stimulator (+50 volts from Model 400B, +15 volts from other CAT Models).

h. Set the TRIGGER switch (S8) at INT. Change to EXT. after analysis sweep commences.

i. Set the ANALYSIS TIME SEC. switch (S2) at EXT.

j. Set STIMULUS switch (S9) at PROMPT.

After depressing the START pushbutton, the 1 KC Oscillator Card or the external pulse gencrator deposits counts into the first address of the CAT memory until the first stimulated event occurs. The first event advances the memory one address. As a result, the number of counts in the first address is proportional to the time interval between the stimulus pulse and the occurrence of the first event. After the first event, counts are deposited into the second address until the second event occurs. The CAT memory is then advanced one address and the number of counts in the second address is proportional to the time interval between the first and second events resulting from the initial single stimulus. As each successive event occurs, the addresses are advanced by one, and the number of counts stored in each address is proportional to the time interval between events (see figure 6–16). To accurately indicate the number of counts in each address, a MNEMOTRON Model 500 Printer is used (see figure 6–15). This provides a numerical readout of the number of counts in the CAT addresses. The Printer permits the determination of the time interval in milliseconds to be obtained from the CAT memory. This is accomplished by dividing the number of counts obtained from the Printer by the frequency in kilocycles (pps) of either the 1 KC Oscillator or the external pulse generator and adding 0.036 (storage cycle time).

Therefore interval time (ms) $= \frac{\text{counts}}{\text{freq(KC)}} + 0.036$

NOTE

If experiment consists of less than 400 events, turn POWER switch at rear of CAT off and on. CAT may now continue normal operation. This releases the electronic interlock allowing CAT to be released from START mode of operation.

6.1.4.3 Non-Stimulus Related Time Interval Sequence

The non-stimulus related time interval sequence follows the same procedure as outlined in paragraph 6.1.4.2 except that a pushbutton device is used to initiate the events under investigation in place of the STIM. (J105) signal from the CAT. In this configuration, the first address of the CAT is not utilized.

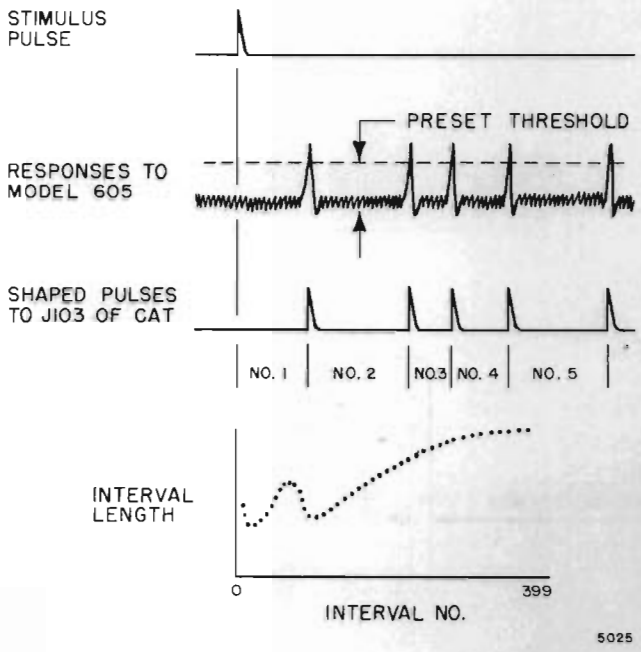


Figure 6–16. Stimulus Related Time Interval Sequence, Waveforms.

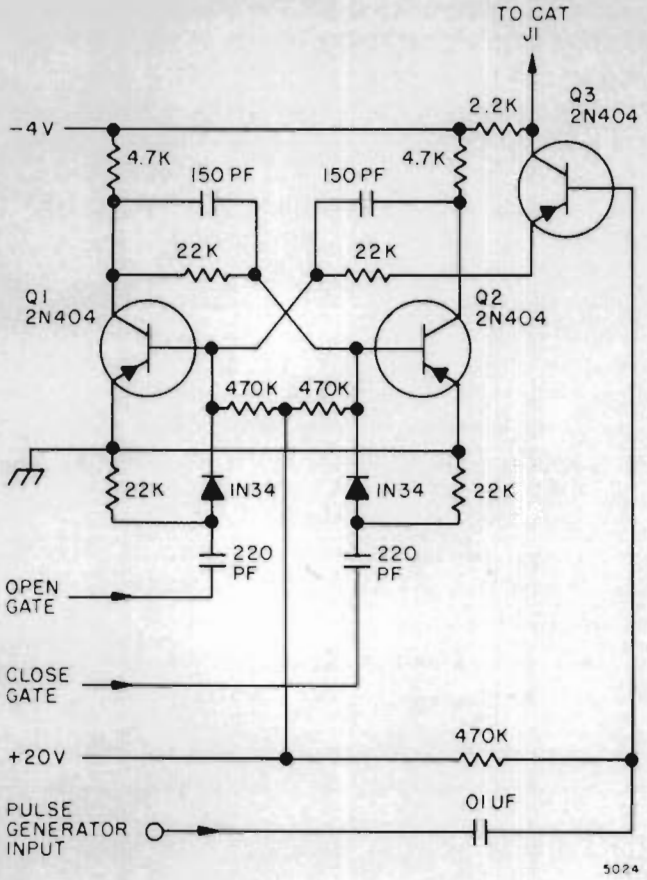


Figure 6–17. Gate Circuit Diagram.

6.1.4.4 Stimulus Related Latency Sequence

When investigative processes require a record of the reaction time between patient stimulation and subsequent response, as in the case of nerve conduction velocity experiments, the CAT performs these experiments with the use of external equipment. The external equipment includes a MNEMOTRON Model 605 Amplitude Discriminator or equivalent, and a gate circuit configuration as shown in figure 6–17 (see figure 6–18).

A positive pulse from the stimulator opens the gate at the time of stimulation. Pulses from the generator are then passed into the input of the CAT, where they are counted.

The first signal pulse is fed to the discriminator circuit which generates an output pulse to the gate to close it. This initiates the storage of the accumulated counts into the CAT memory and advances the address register to the next address. The next pulse from the stimulator again opens the gate and counts are again accumulated until the input signal from the patient via the discriminator closes the gate and initiates the storage cycle.

To process a stimulus related latency sequence, proceed as follows:

a. Remove the Modulator Circuit Card from slot 6L on the left hand side of the CAT.

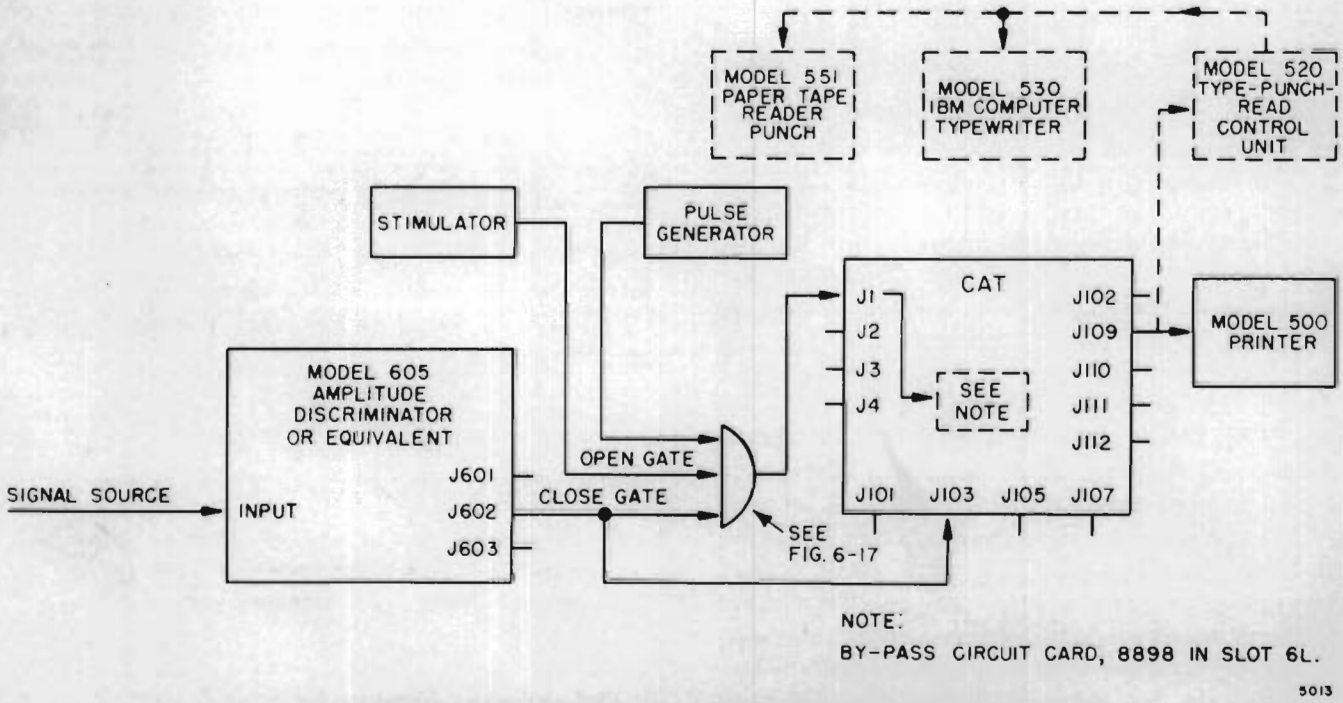


Figure 6–18. Stimulus Related Latency Sequence, Block Diagram.

b. Place a Modulator By-Pass Circuit Card 8898 in slot 6L.

c. Connect the output of the signal under investigation to the INPUT connector of the MNEMOTRON Model 605 Amplitude Discriminator.

d. Set the BASELINE vernier of the Model 605 Amplitude Discriminator to a desired amplitude level which will discriminate against unwanted noise signals.

e. Connect the output of the Amplitude Discriminator via the EXT. TRIG jack (J602) to CLOSE GATE input of the external gate circuitry.

f. Also connect the output of the Amplitude Discriminator via EXT. TRIG jack (J602) to the ADDR. ADV. jack (J103) at the rear of the CAT.

g. Connect the sync output of the external stimulator to the OPEN GATE input of the external gate circuitry.

h. Connect the external pulse generator to the PULSE GEN. IN input of the external gate circuitry. (Amplitude −2 volts, frequency determined by the intervals encountered and the resolution required.)

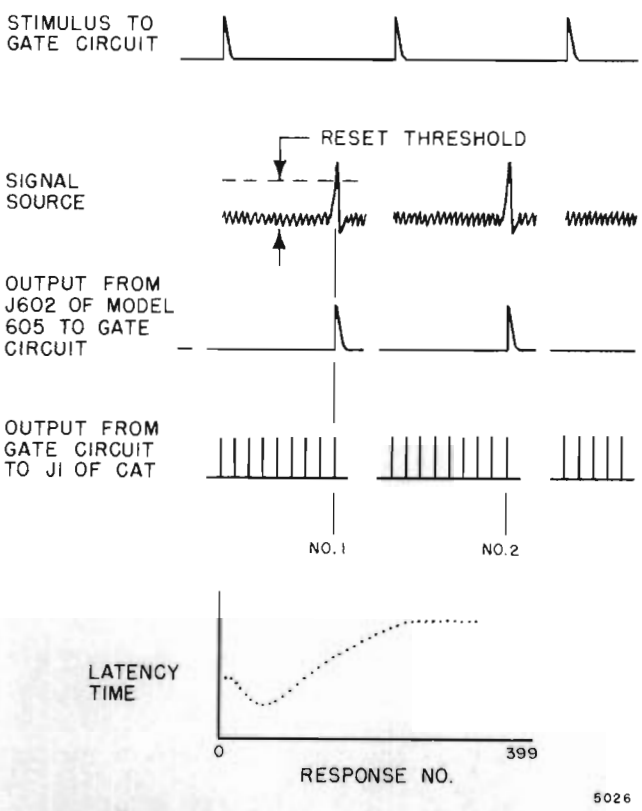


Figure 6–19. Stimulus Related Latency Sequence, Waveforms.

i. Connect the TO CAT INPUT output of the external gate circuitry to the first input connector of the CAT.

j. Set the TRIGGER switch (S8) at INT. Change to EXT. after analysis sweep commences.

k. Set the ANALYSIS TIME SEC. switch (S2) at EXT.

After depressing the START pushbutton, the initial stimulation will begin the stimulus related latency sequence (see figure 6–19). The number of pulses stored in each address are proportional to the elapsed time between stimulation and the occurrence of the first elicited response. This time may be calculated as

$$t = \frac{n}{f}$$

where f = frequency of pulses in kilocycles-per-second

n = number of stored pulses in each address

t = elapsed time in milliseconds

6.1.4.5 Non-Stimulus Related Dwell Time Sequence

When a record is required of the period of time during which a signal exceeds a preset threshold, as in the case of pulse width modulation studies, the CAT performs these investigations with the aid of the MNEMOTRON Model 605 Amplitude Discriminator. To obtain a non-stimulus related dwell time sequence, proceed as follows (see figure 6–20):

a. Connect the output of the signal under investigation to the INPUT connector of the Model 605 Amplitude Discriminator.

b. Connect the output of the Amplitude Discriminator via the EXT. TRIG jack (J602) to the OPEN GATE input of the external gate circuitry (see figure 6–17).

c. Connect the output of the Amplitude Discriminator via the ADDR. RESET jack (J601) to the CLOSE GATE input of the external gate circuitry.

d. Also connect the output of the Amplitude Discriminator via ADDR. RESET jack (J601) to thet ADDR. ADV. jack (J103) at the rear of the CAT.

e. Connect external pulse generator to the PULSE GEN. IN input of the external gate circuitry.

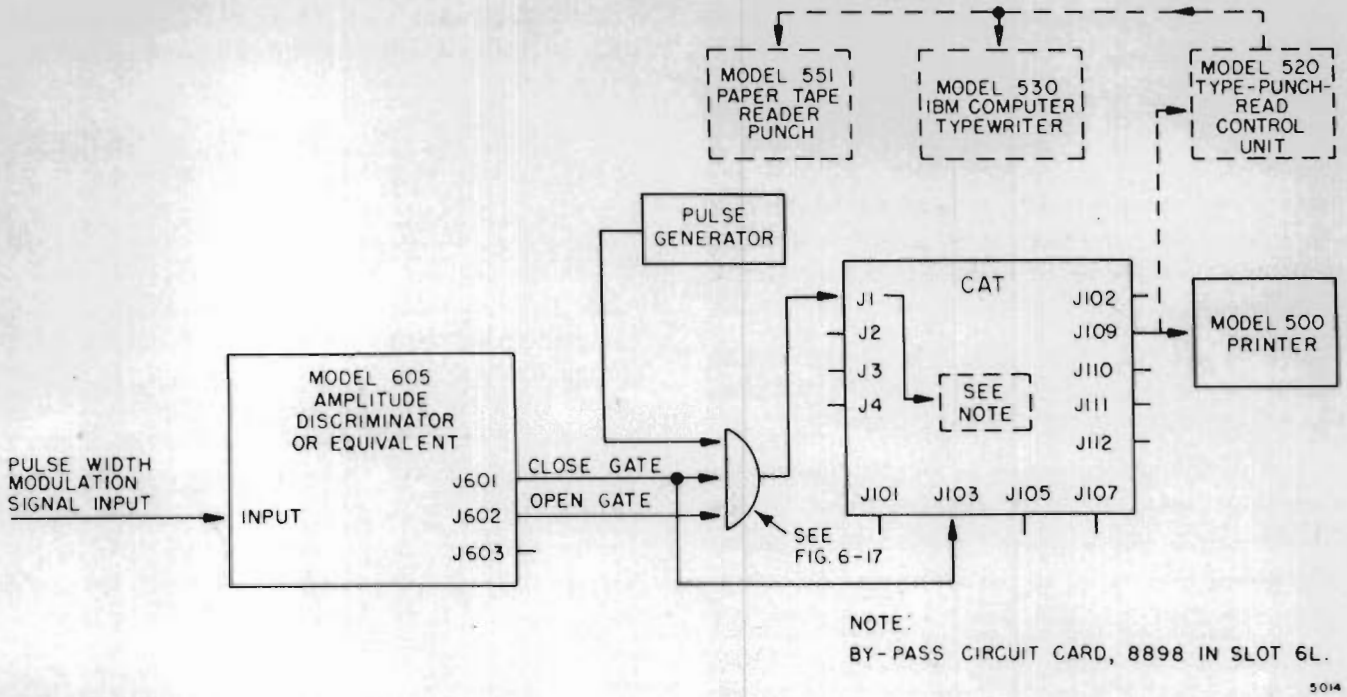


Figure 6–20. Non-Stimulus Related Dwell Time Sequence, Block Diagram.

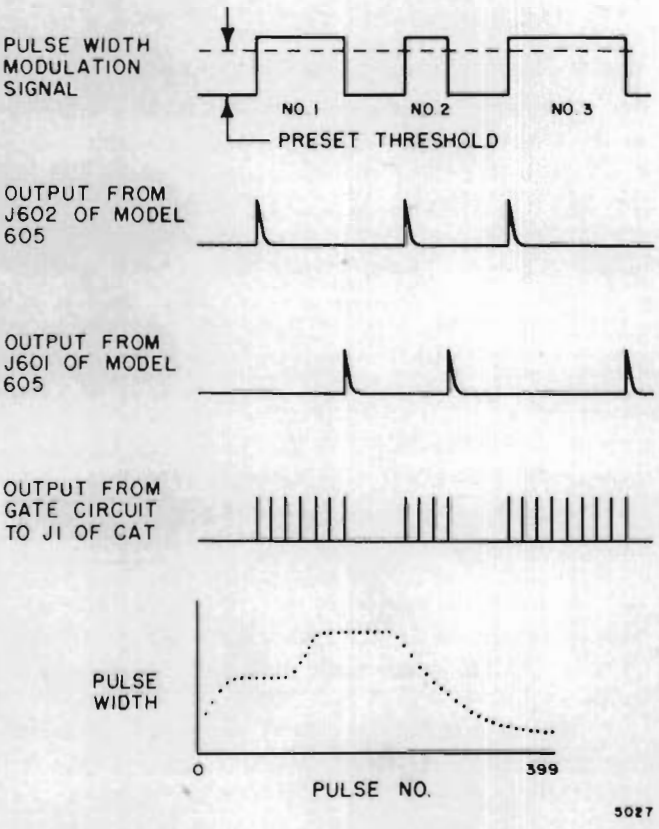


Figure 6–21. Non-Stimulus Related Dwell Time Sequence, Waveforms.

f. Connect the TO CAT INPUT of the external gate circuitry to the first input connector of the CAT.

g. Remove the Modulator Circuit Card from slot 6L on the left hand side of the CAT.

h. Place a Modulator By-Pass Circuit Card 8898 in slot 6L.

i. Set the desired threshold level on the Amplitude Discriminator by adjusting the BASELINE vernier (0 to +10 volts).

j. Set CAT ANALYSIS TIME SEC. switch (S2) at EXT.

k. Set CAT TRIGGER switch (S8) at EXT.

After depressing the START pushbutton, the signal which exceeds the threshold level will open the gate circuitry to allow the pulse generator to accumulate counts. When the signal falls below the threshold level, the counts being deposited in the channel addressed will be stopped and the address register will advance one address. This provides the investigator with an accurate measurement of the time period that the input signal has exceeded the preselected level (see figure 6–21).

6.1.4.6 Non-Stimulus Related Amplitude Sequence

When a record is required of the amplitude of sequential pulse events, such as the examination of scintillation pulses from radioactive materials, the CAT performs these investigations with the aid of the MNEMOTRON Model 606 Amplitude-to-Time Converter. To obtain non-stimulus related amplitude sequence, proceed as follows (see figure 6–22):

a. Connect the input pulses from the signals under investigation to the INPUT jack of the Model 606 Amplitude-to-Time Converter.

b. Connect the output of the Amplitude-to-Time Converter via the EXT. TRIG jack (J602) to the OPEN GATE input of the external gate circuitry (see figure 6–17).

c. Connect the output of the Amplitude-to-Time Converter via the EXT. ADD. RESET jack (J601) to the CLOSE GATE input of the external circuitry.

d. Connect a second output of the Amplitude-to-Time Converter via the EXT. ADD. RESET jack (J601) to the ADDR. ADV. jack (J103) at the rear of the CAT.

e. Connect the external pulse generator to the PULSE GEN. IN input of the external gate circuitry. (−2 volts amplitude).

f. Connect the TO CAT INPUT of the external gate circuitry to the first input connector of the CAT.

g. Remove the Modulator Circuit Card from slot 6L on the left hand side of the CAT.

h. Place a Modulator By-Pass Circuit Card 8898 in slot 6L.

i. Set analysis time to EXT.

j. Set TRIGGER switch to INT. Change to EXT. after analysis sweep commences.

After depressing the START pushbutton, a pulse from the scintillation detector to the Amplitude-to-Time Converter will generate a signal to open the gate circuitry (see figure 6–17) allowing the pulse generator to deposit counts in the CAT. A second pulse, proportional in time to the amplitude of the input signal, from the Amplitude-to-Time Converter, will close the gate and stop the accumulation of counts. The channel addressed at that time will store the counts and the address register will advance one address. The number of counts in each address will accurately reflect the amplitude of the input pulse signals under investigation (see figure 6–23).

In the Model 606 Amplitude-to-Time Converter, a 500 microsecond interval corresponds to an input

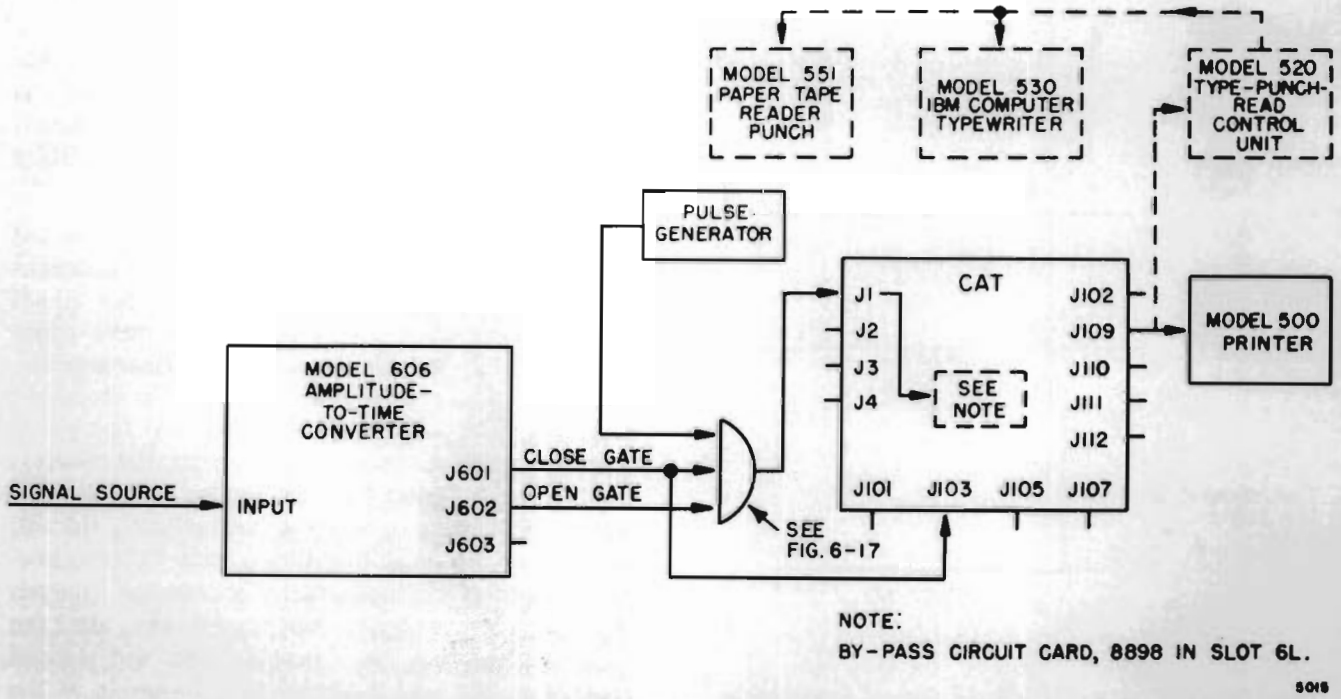


Figure 6–22. Non-Stimulus Related Amplitude Sequence, Block Diagram.

amplitude of 10 volts, 250 microseconds to 5 volts, 125 microseconds to 2.5 volts, etc. The conversion equation from counts to volts is

$$\text{Amplitude (in volts)} = \frac{n}{f(KC)} \times 20$$

where n = counts

f = pulse frequency in KC

From this it can be seen that f should be 200 KC or more for adequate resolution.

6.2 APPLICATIONS OF THE CAT USING PROGRAM H

The basic feature of program H is the requirement of only an address reset pulse. The application of the pulse stops the CAT address advance, deposits one count in the channel addressed, resets that address to zero and, after 50 microseconds, automatically starts a new analysis sweep. The Model 605 Amplitude Discriminator is the only accessory required. Using program H, CAT analysis sweeps are triggered externally, regardless of the front panel position of the TRIGGER switch (S8).

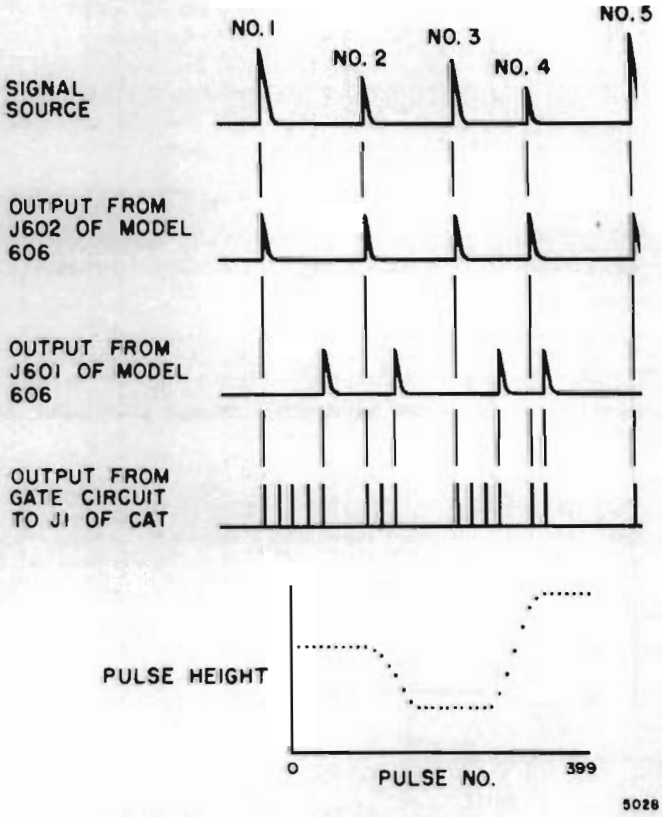


Figure 6–23. Non-Stimulus Related Amplitude Sequence, Waveforms.

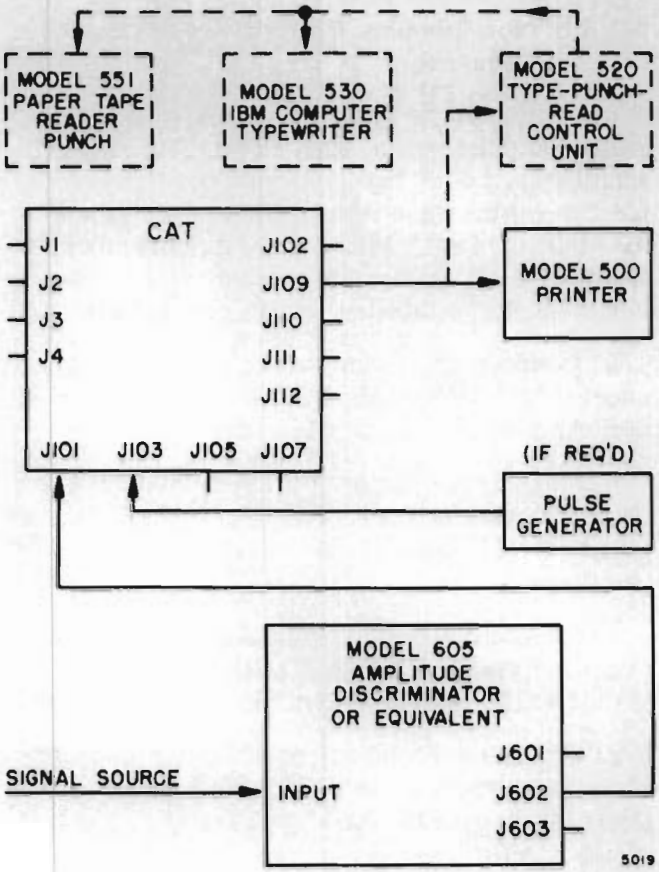


Figure 6–24. Non-Sequential Period Distribution Curve, Block Diagram.

6.2.1 NON-SEQUENTIAL PERIOD DISTRIBUTION CURVE

Non-sequential period distribution curves have application in the investigation of frequency analysis of speech waveform patterns. In this application, it is of interest to determine whether they have preferential frequencies.

The input signal under investigation is connected to the input of the Model 605 Amplitude Discriminator. A pulse is emitted when the input signal exceeds a preset threshold level. This pulse starts the CAT analysis sweep and each successive pulse, as a result of an input signal exceeding the threshold level, stops the address register, deposits one count in the channel addressed, and resets the address register to zero. After 50 microseconds for a storage cycle, a new analysis sweep is automatically started. If, however, the time duration of one pulse following another is longer than the preselected analysis time, the address register will reset to zero after the 400th address has been reached and will deposit a count in the zero address. It will remain at the zero address until the next pulse finally arrives.

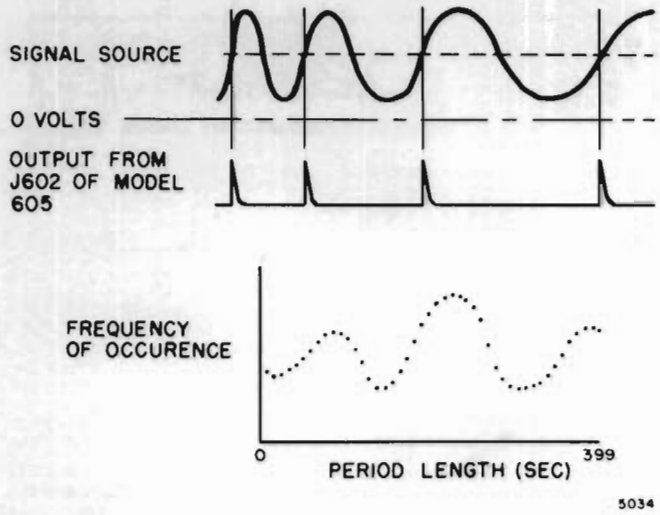


Figure 6–25. Non-Sequential Period Distribution Curve, Waveforms.

To obtain a non-sequential period curve using program H, proceed as follows (see figure 6–24):

a. Check that the PROGRAM switch (S103) at the rear of the CAT is set at the H position.

b. Connect the input signal under investigation to the INPUT jack of the Model 605 Amplitude Discriminator or external shaping circuit.

c. Set the BASELINE vernier of the Model 605 Amplitude Discriminator to a desired amplitude level which will discriminate against unwanted noise signals.

d. Connect the output of the Amplitude Discriminator via the EXT. TRIG jack (J602) to the ADDR. RESET jack (J101) at the rear of the CAT.

e. If the addresses are to be advanced externally:

1) Connect an external pulse generator to the ADDR. ADV. jack (J103) (+2 volts).

2) Set the ANALYSIS TIME SEC. switch (S2) at EXT.

After depressing the START pushbutton, the first signal pulse will start an analysis sweep. The second pulse stops the sweep, deposits one count in the channel addressed, and resets the address register to zero (see figure 6–25).

After 50 microseconds, another analysis sweep will start until the third pulse stops that sweep to repeat the process. This supplies the investigator with a record of the distribution of time intervals of each cycle of a speech waveform pattern.

6.2.2 NON-SEQUENTIAL INTERVAL DISTRIBUTION CURVE

This application of the CAT using program H involves a non-sequential interval distribution curve. This application might be useful for analysis of the distribution of nerve action potential intervals where very long or very short analysis time durations are desired. With the use of a MNEMOTRON Model 605 Amplitude Discriminator or external shaping circuit, the first signal pulse derived from the input signal exceeding the preset threshold level starts an analysis sweep and subsequent pulses stop accumulation in the CAT address register, deposit one count in the channel addressed, and reset the address register to zero. After 50 microseconds for a storage cycle, an analysis sweep is automatically started again. If, however, the time duration of one pulse following another is longer than the preselected analysis time duration, the address register will reset to zero after the 400th address has been reached and a count of one is stored in address zero. It will remain at the zero address until the next pulse arrives which will start the sweep again.

To obtain a non-sequential interval distribution curve, proceed as follows (see figure 6–24):

a. Check that the PROGRAM switch (S103) at the rear of the CAT is set at the H position.

b. Connect the input signal under investigation to the INPUT jack of the Model 605 Amplitude Discriminator or external shaping circuit.

c. Set the BASELINE vernier of the Model 605 Amplitude Discriminator to a desired amplitude level which will discriminate against unwanted noise signals.

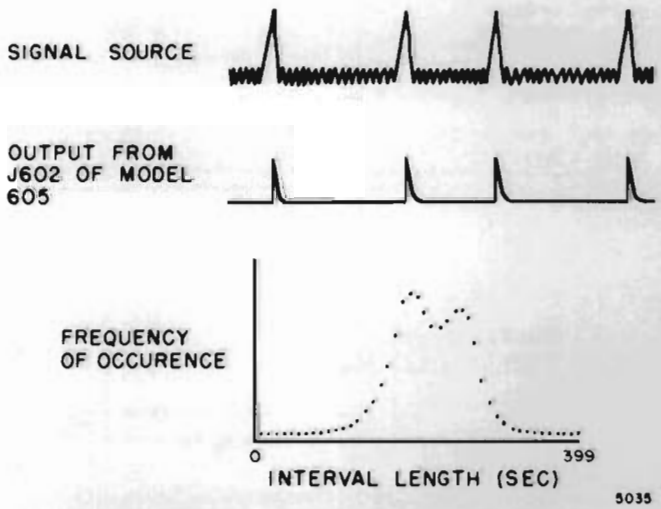


Figure 6–26. Non-Sequential Interval Distribution Curve, Waveforms.

d. Connect the output of the Amplitude Discriminator via the EXT. TRIG jack (J602) to the ADDR. RESET jack (J101) at the rear of the CAT.

e. If the addresses are to advance externally:

1) Connect an external pulse generator to the ADDR. ADV. jack (J103) (+2 volts).

2) Set the ANALYSIS TIME SEC. switch (S2) at EXT.

After depressing the START pushbutton, the first signal pulse will start an analysis sweep. The second pulse stops the sweep and deposits a count in the channel addressed, and resets the address register to zero (see figure 6–26).

After 50 microseconds, another analysis sweep will start until the third pulse stops that sweep to repeat the process. This supplies the investigator with a record of the distribution time intervals between signal responses into the CAT.

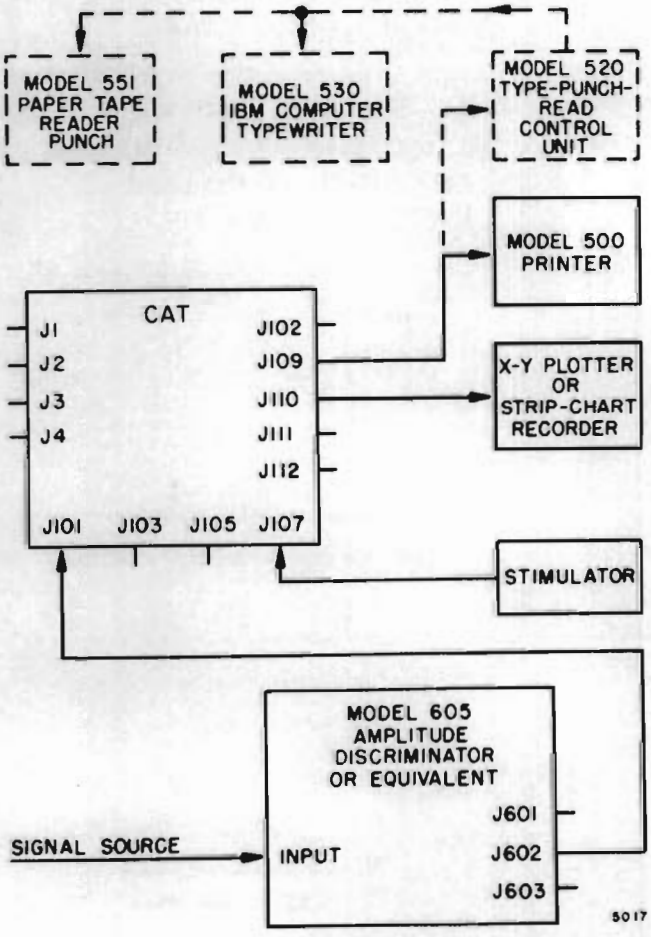


Figure 6–27. Non-Sequential Stimulus Related Latency Distribution Curve, Block Diagrams.

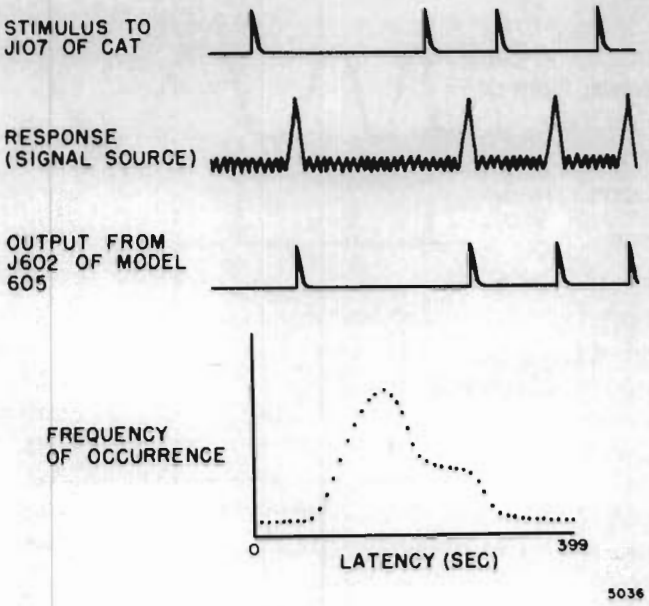


Figure 6–28. Non-Sequential Stimulus Related Latency Distribution Curve, Waveforms.

6.3 APPLICATIONS OF THE CAT USING PROGRAM D

6.3.1 NON-SEQUENTIAL STIMULUS RELATED LATENCY DISTRIBUTION CURVES

When a distribution curve is required of the time interval between stimulation and the occurrence of the first signal pulse, the CAT provides a latency distribution curve using program D. Using this program, the PROGRAM switch (S103) at the rear of the CAT is at the D position. The curve is obtained with an external stimulator which starts the analysis sweep followed by the companion signal pulse which stops the address register, deposits one count in the channel addressed, and resets the address register to zero. The next stimulation again starts the analysis sweep and its companion pulse repeats the operation. Only the first pulse after stimulation is processed; all subsequent pulses, if any, are not accumulated by the CAT.

To obtain a non-sequential stimulus related latency distribution curve, proceed as follows (see figure 6–27):

a. Connect the input signal under investigation to the INPUT jack of the Model 605 Amplitude Discriminator or external shaping circuit.

b. Set the BASELINE vernier of the Model 605 Amplitude Discriminator to a desired amplitude level which will discriminate against unwanted noise signals.

c. Connect the output of the Amplitude Discriminator via EXT. TRIG jack (J602) to the ADDR. RESET connector (J101) at the rear of the CAT.

d. Connect the sync output of the external stimulator to the EXT TRIG. connector (J107) at the rear of the CAT.

e. Check that the PROGRAM switch (S103) is at the D position.

After depressing the START pushbutton, the stimulation pulse will start an analysis sweep. The first signal pulse following stimulation will stop the address register, deposit one count in the channel addressed, and reset the address register to zero. This provides the investigator with an accurate indication of the distribution of time intervals between stimulation and the subsequent response (see figure 6–28).

6.3.2 NON-SEQUENTIAL NON-STIMULUS RELATED DWELL TIME DISTRIBUTION CURVES

When a distribution curve is required of the time interval during which an analog signal exceeds a preset voltage level, the CAT utilizes the MNEMOTRON Model 605 Amplitude Discriminator to provide a dwell time distribution curve. A typical application of dwell time distribution curves using program D is in signal pulse width determination.

To obtain non-sequential non-stimulus related dwell time curves, proceed as follows (see figure 6–29):

a. Connect the signal under investigation to the INPUT jack of the Model 605 Amplitude Discriminator.

b. Connect the output of the Amplitude Discriminator via the EXT. TRIG jack (J602) to the EXT TRIG. connector (J107) at the rear of the CAT.

c. Connect the output of the Amplitude Discriminator via the ADDR. RESET jack (J601) to the ADDR. RESET connector (J101) at the rear of the CAT.

d. Set the BASELINE vernier of the Amplitude Discriminator to the desired level (0 to +10 volts).

After depressing the START pushbutton, when the output signal exceeds the preset value, an analysis sweep will start. When the signal falls below the preset value, one count will be deposited in the channel addressed, the address register will reset to zero waiting for the next time a signal exceeds the threshold level. This provides the investigator with a non-sequential distribution curve indicating the time interval during which the signals exceeded the preselected level (see figure 6–30).

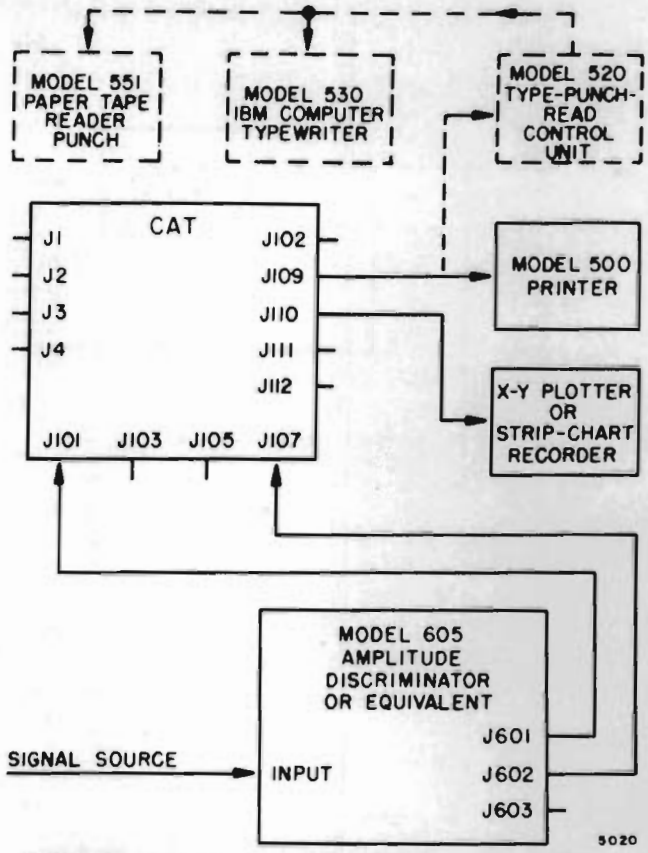


Figure 6–29. Non-Sequential Non-Stimulus Related Dwell Time Distribution Curve, Block Diagram.

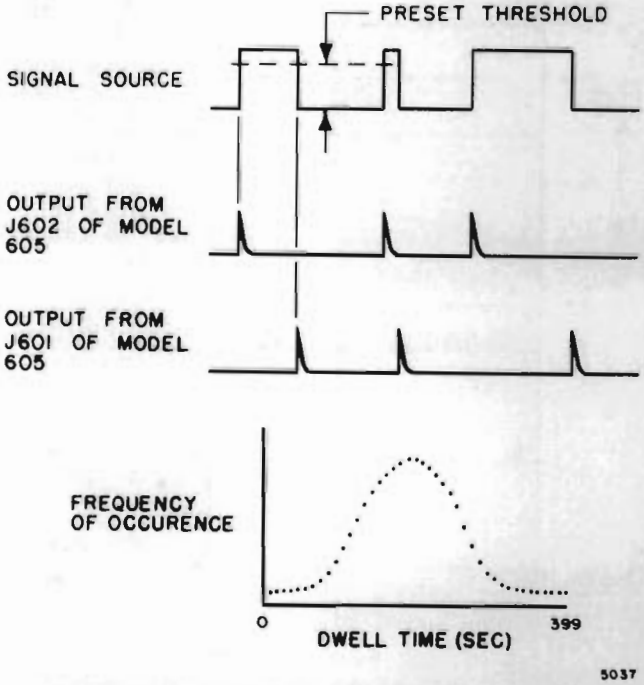


Figure 6–30. Non-Sequential Non-Stimulus Related Dwell Time Distribution Curve, Waveforms.

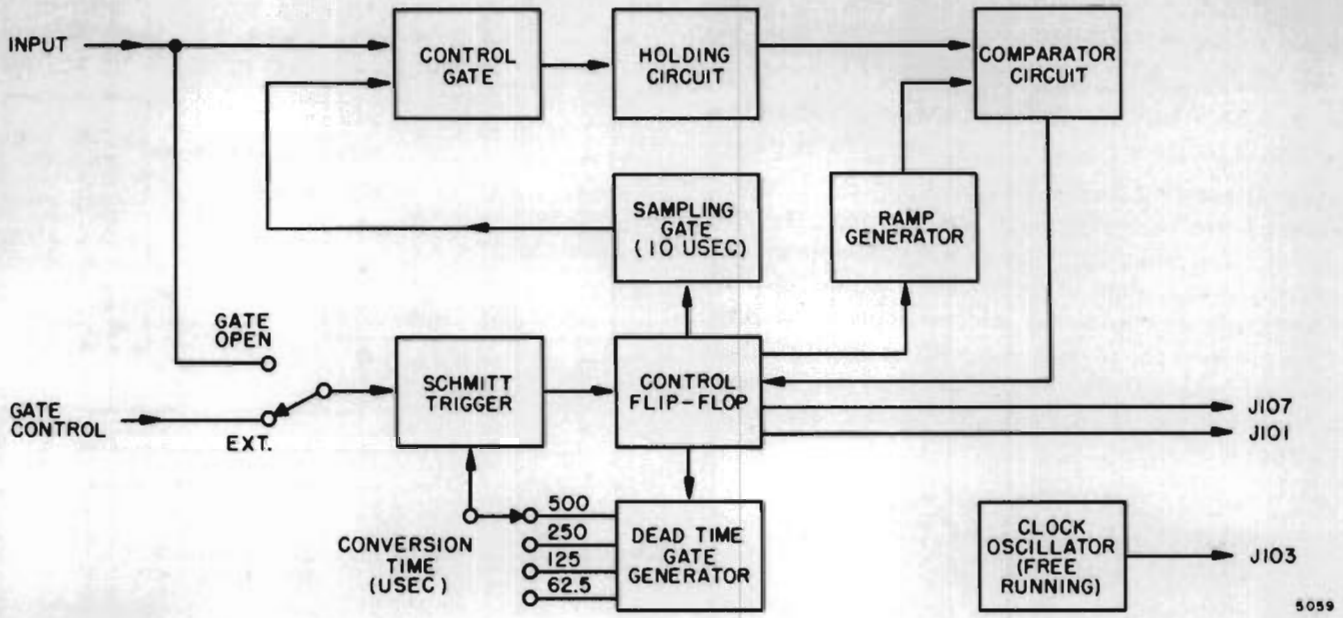


Figure 6–31. Model 606 Amplitude-to-Time Converter, Block Diagram.

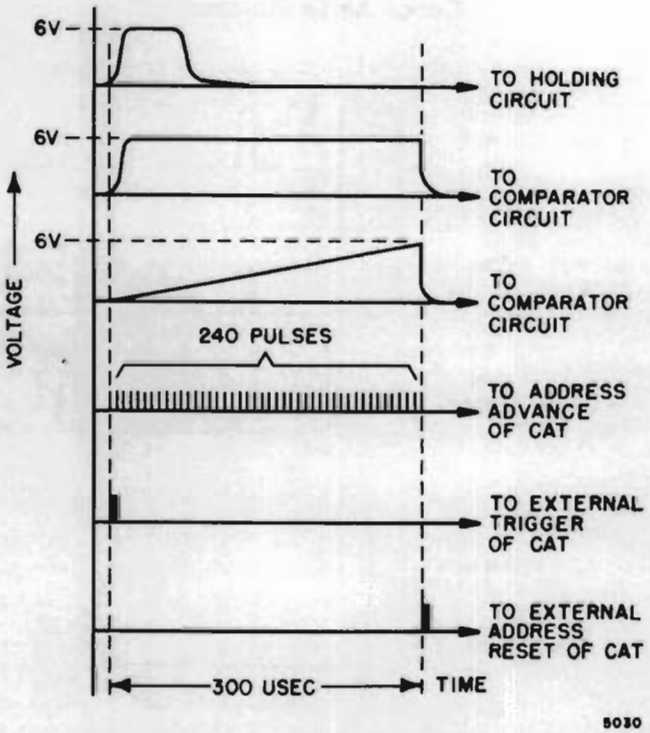


Figure 6–32. Model 606 Amplitude-to-Time Converter, Internal Direct Pulse, Waveforms.

6.3.3 NON-SEQUENTIAL NON-STIMULUS RELATED AMPLITUDE DISTRIBUTION CURVES

6.3.3.1 Pulse Amplitude Distribution Curves

When a distribution curve is required of the amplitude of signal pulses, the CAT utilizes the MNEMOTRON Model 606 Amplitude-to-Time Converter in the direct pulse input configuration. This method provides a trigger pulse to the CAT when the input pulse is received at the Amplitude-to-Time Converter. This is fed to a holding circuit which retains the peak signal amplitude, starts an analysis sweep, and initiates a ramp function. After the signal peak is matched to the ramp, the analysis sweep stops, a count is deposited in the channel addressed, and the address register is reset to zero (see figures 6–31 and 6–32).

To obtain a non-sequential non-stimulus related pulse amplitude curve, proceed as follows (see figure 6–33):

a. Connect the input pulse under investigation to the INPUT jack of the Model 606 Amplitude-to-Time Converter (0 to +10 volts).

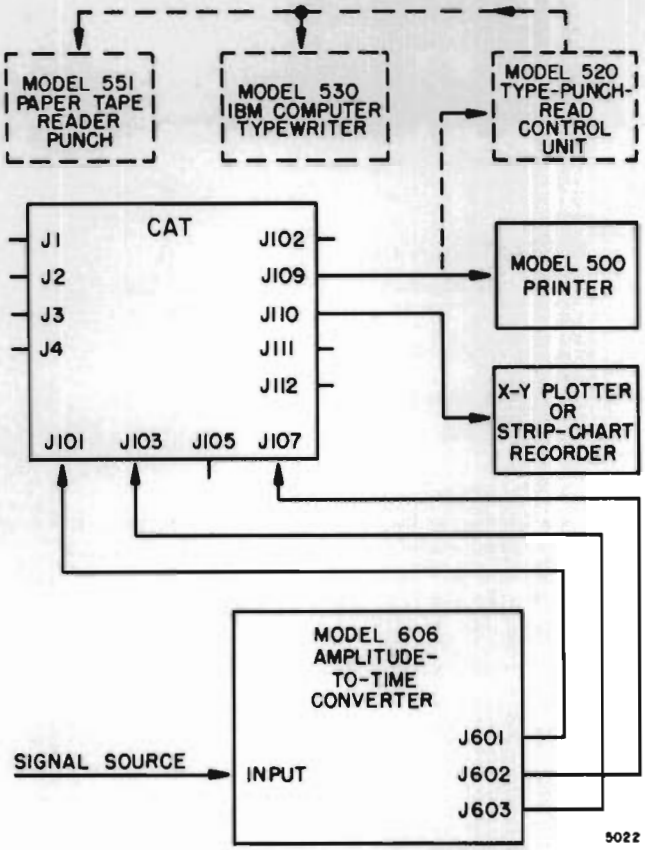


Figure 6–33. Non-Sequential Non-Stimulus Related Amplitude Distribution Curve, Direct Pulse Input, Block Diagram.

b. Connect the output of the Amplitude-to-Time Converter via the EXT. TRIG jack (J602) to the EXT TRIG. connector (J107) at the rear of the CAT.

c. Connect the output of the Amplitude-to-Time Converter via the ADDR. RESET jack (J601) to the ADDR. RESET connector (J101) at the rear of the CAT.

d. Connect the output of the Amplitude-to-Time Converter via the EXT. ADD. ADV. jack (J603) to the ADDR. ADV. connector (J103) at the rear of the CAT.

e. Set the CONVERSION TIME selector switch of the Amplitude-to-Time Converter at the desired setting.

f. Set the GATE OPEN/EXT. switch at the GATE OPEN position.

After depressing the START pushbutton, a signal pulse will deposit one count in an address proportional to the amplitude of the signal. This provides the investigator with a distribution curve reflecting the amplitudes of pulse signals under investigation (see figure 6–34).

6.3.3.2 Amplitude Density Distribution Curves

When a distribution curve is required of the distribution of sampled analog amplitudes, the Model 606 Amplitude-to-Time Converter operates in the external control input configuration. This method provides a 10 microsecond period in which the analog signal is sampled for ultimate transmission to the CAT addresses (see figure 6–35). As in the case

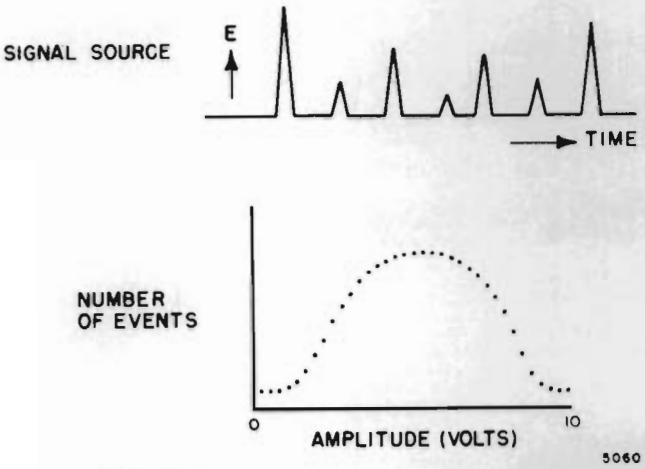


Figure 6–34. Non-Sequential Non-Stimulus Related Amplitude Distribution Curve, Direct Pulse Input, Waveforms.

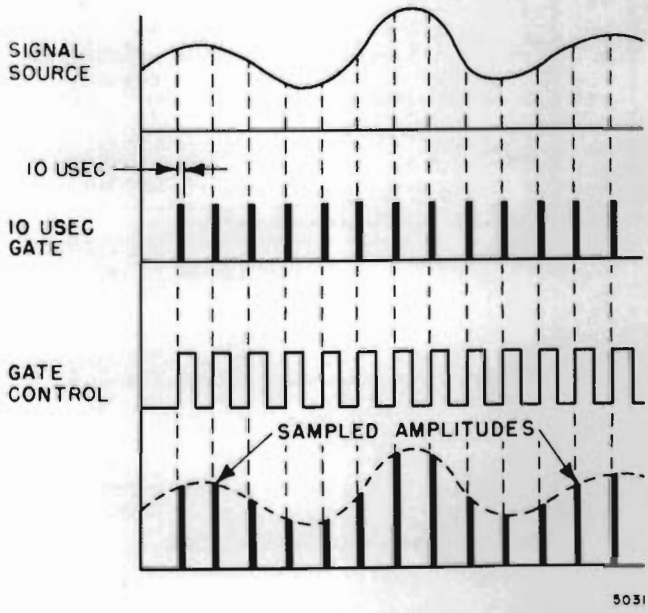


Figure 6–35. Model 606 Amplitude-to-Time Converter, Internal Analog Waveforms.

of the Direct Pulse Input, the signals received at the Amplitude-to-Time Converter provide a trigger to start an analysis sweep. This is followed by an address reset signal which determines the address proportional to the signal amplitude in which a count is deposited.

To obtain a non-sequential non-stimulus related amplitude density curve, proceed as follows (see figure 6–36):

a. Connect the input signal under investigation to the INPUT jack of the Model 606 Amplitude-to-Time Converter (0 to +10 volts).

b. Connect external gating pulses to the GATE CONTROL jack of the Amplitude-to-Time Converter (0 to +50 volts).

c. Connect the output of the Amplitude-to-Time Converter via the EXT. TRIG jack (J602) to the EXT TRIG. connector (J107) at the rear of the CAT.

d. Connect the output of the Amplitude-to-Time Converter via the ADDR. RESET jack (J601) to the ADDR. RESET connector (J101) at the rear of the CAT.

e. Connect the output of the Amplitude-to-Time Converter via the EXT. ADD. ADV. jack (J603) to the ADDR. ADV. connector (J103) at the rear of the CAT.

f. Set the CONVERSION TIME selector switch of the Amplitude-to-Time Converter at the desired setting.

g. Set the GATE OPEN/EXT. switch at EXT.

After depressing the START pushbutton, an analog signal will deposit one count in an address proportional to the amplitude of the signal at the sampling time (see figure 6–37). This supplies the investigator with a distribution curve of the sampled amplitudes of the input signal to determine preferential amplitudes of interest.

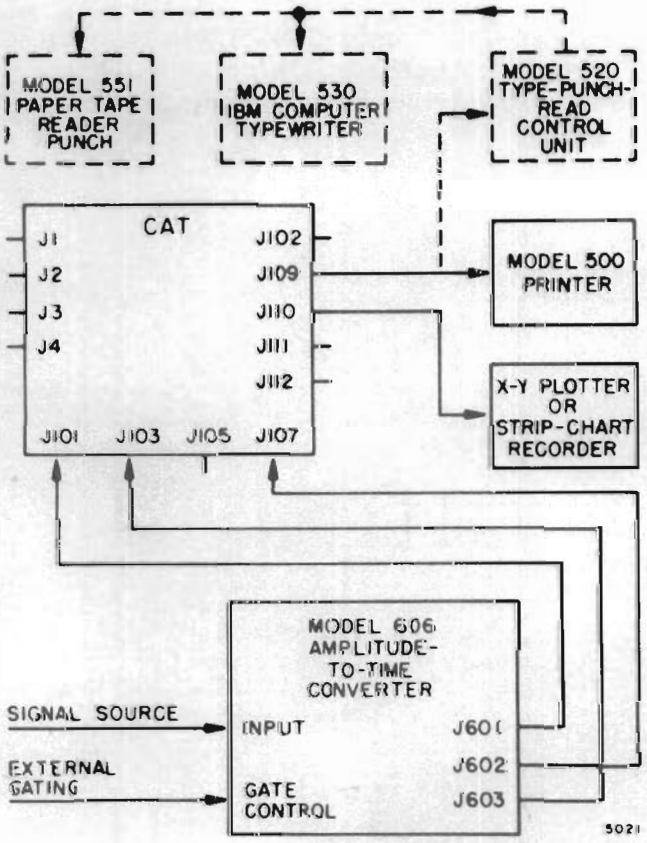


Figure 6–36. Non-Sequential Non-Stimulus Related Amplitude Distribution Curve, External Control Input, Block Diagram.

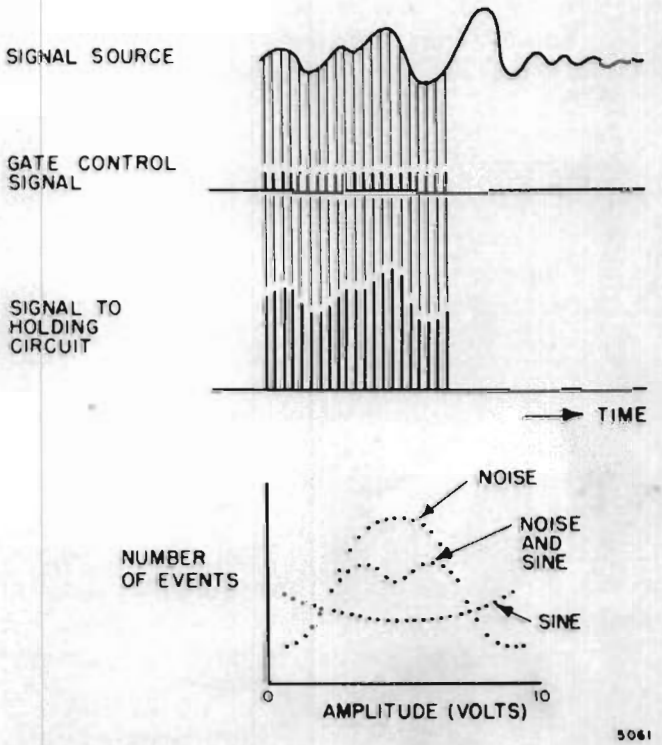


Figure 6–37. Non-Sequential Non-Stimulus Related Amplitude Distribution Curve, External Control Input, Waveforms.

SECTION VII
CIRCUIT DIAGRAMS

7.0 OPERATIONAL DIAGRAMS

Drawing No.	*Nomenclature*
WFB8974	Memory Timing Accumulate Mode of Operation
WFB8442	Memory Timing Display Mode of Operation
WFB8445	Memory Timing Readout Mode of Operation
WFB8975	Accumulate Waveforms One Input in Use
WFB8976	Accumulate Waveforms Two Inputs in Use
WFB8977	Accumulate Waveforms Four Inputs in Use
B8916	Memory Location Logic Diagram

7.1 CONTROLS, INDICATORS, AND CONNECTORS

Drawing No.	*Nomenclature*
B8834	Input Connectors (J1, J2, J3, J4)
B8831	Rear Panel Connectors (J101, J102, J103, J104, J105, J106, J107, J108, J109, J110, J111, J112)
B1432	Inputs in Use Switch (S1)
B1431	Analysis Time Switch (S2)
B9012	Display Range Switch (S3)
B9014	Front Panel Attachments—1 (SL1, SL2, SL3, SL4, S4, S5, S6, S7)
B1433	Front Panel Attachments—2 (R1, R2, R3, R4, R5, R9, R10, R11, S9, S10, R6)
B1574	Input Switches (S11, S12, S13, S14) and Scale Illumination Control
B1575	Rear Panel Controls (S102, S103)
B8832	Rear Panel Attachments (Q101, Q102, Q103, Q104, Q105, T101, TS101, Z101)
B9013	CRT Socket Connections
SCB8468-1	CRT Control Circuit Schematic (RV105-2, RV254-1)

7.2 LEFT HAND SIDE PLUG-IN CIRCUIT CARDS

PC & Card No.	*Nomenclature*	*Drawing No.*
2L	Trigger/Amplitude Discriminator Circuit	SCB8847
3L, 4L, 5L, 6L	Modulator Circuit	SCB8897
3L, 4L, 5L, 6L	500 KC Modulator Circuit	SCB8836
3L, 4L, 5L, 6L	Modulator By-Pass Circuit	SCB8898
6L	1 KC Oscillator	SCB9081
7L	Modulator Power Supply Circuit	SCB8896
8L	Modulator Gate Control Circuit	SCB8895
9L	Modulator Gates Circuit	SCB8894
10L	Trigger Generator Circuit	SCB8999
11L	Stimulus Pulse Generator Circuit	SCB8892-2
12L	External Address Control Circuit	SCB8998
13L	Delay Control Flip-Flop Circuit	SCB8890
14L, 15L, 16L	Scale of 16 Circuit	SCB8889

PC & Card No.	Nomenclature	Drawing No.
17L	51.2 KC Oscillator and Shaper Circuit	SCB8888-2
17L	12.8 KC Oscillator and Shaper Circuit	SCB8888
18L	CRT High Voltage Power Supply Circuit	SCB8492
19L, 20L, 21L, 23L	Complete Supply Circuit Diagram	SCB8425
19L	−4, +4, +20 Voltage Regulator Circuit	SCB8493
20L	−20, −12 Voltage Regulator Circuit	SCB8494
21L	Power Supply Filter and Rectifier No. 1 Circuit	SCB8495
23L	Power Supply Filter and Rectifier No. 2 Circuit	SCB8496

7.3 RIGHT HAND SIDE PLUG-IN CIRCUIT CARDS

PC & Card No.	Nomenclature	Drawing No.
1R	Control Logic Circuit	SCB8500
2R	Auto Data Transfer Circuit	SCB8501
3R	Read Cycle Generator Circuit	SCB8502-1
3R	Read Cycle Generator Circuit	SCB8502-2
4R	Memory Current Generator Circuit	SCB8503
5R	Write Cycle Generator Circuit	SCB8504
6R, 8R	Second Address Decade Circuit	SCD8507-2
7R, 9R	4 X 5 Memory Decoder Circuit	SCB8506
10R	Scale of Four/Memory Location Circuit	SCB8508
11R	Digital-to-Analog Converter and Deflection Amplifier Circuit	SCB8509
12R	Selective Centering Circuit	SCB8887
13R	Shift Logic Circuit	SCB8511
14R, 16R, 18R, 20R, 22R, 24R	Arithmetic Decade Circuit	SCC8512
15R, 17R, 19R, 21R, 23R, 25R	Sense and Inhibit Amplifiers Circuit	SCB8513
26R	Filter Board Circuits	B8833

7.4 INTERCONNECTION BOARD KEYS

Nomenclature	Drawing No.
Left Hand	D1420
Right Hand	D1419