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This Technical Newsletter provides replacement pages for the subject publication. Pages to be inserted and/or removed are:

2-3 through 2-6
2-11, 2-12
2-51, 2-52
2-57 through 2-60
2-67, 2-68
2-75, 2-76
2-81, 2-82

A technical change to the text or to an illustration is indicated by a vertical line to the left of the change.

Summary of Amendments

- Request in bus lines 4 through 15 have been changed from "Unused" to "Reserved" lines.
- Classification has been provided for poll identifier bit 1 and 2.

Note. Please file this cover letter at the back of the manual to provide a record of changes.

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Signal Line Groups

The I/O channel signal lines are shown, by group, in Figures 2-1 and 2-2.

Note: The direction is shown for each line with the assumption that the I/O channel originates on the left and the I/O attachments are on the right.

Service Group Signal Lines

The signal lines associated with the service group are shown in Figure 2-1.

Signal name	*Direction*	*Number of lines*
Address bus bits 0–15	⟷	16
Address bus bit 16	→	1
Data bus	⟷	18
Address gate	→	1
Address gate return	←	1
Service gate	→	1
Service gate return	←	1
Condition code in bus	←	3
Cycle input indicator	←	1
Cycle byte indicator	←	1
Status bus	→	4
Data strobe	→	1
Initiate IPL	→	1
IPL	←	1
Halt or MCHK (machine check)	→	1
System reset	→	1
Power on reset	→	1
Total number of lines		54

Figure 2-1. Service group signal lines

Poll Group Signal Lines

The signal lines associated with the poll group are shown in Figure 2-2.

Signal name	*Direction*	*Number of lines*
Request in bus	←	4
Cycle steal request in	←	1
Poll identifier	→	5
Poll	→	1
Poll prime	→	1
Poll propagate	→	1
Poll return	←	1
Burst return	←	1
Total number of lines		15

Figure 2-2. Poll group signal lines

Functional Subsets of the Signal Lines

The I/O channel signal lines can have subsets, depending on the level of function required by the I/O attachment. In order of increasing level of function, these subsets are:

- Basic subset
- Interrupt subset
- Cycle-steal/IPL subset

Attachment to a subset is a prerequisite for attachment to the next higher level subset.

Basic Subset

The basic subset consists of the buses and tags to support functions initiated by the processor; for example, direct program control (DPC) commands. This includes the data transfers associated with the DPC command itself. The basic subset supports DPC devices that do not interrupt. I/O signal lines in the basic subset are shown in Figure 2-3.

Service group signal lines

Signal name	*Direction*	*Number of lines*
Address bus bits 0–15 (Note 1)	→	16
Address bus bit 16	→	1
Data bus (Note 2)	→	18
Address gate	→	1
Address gate return	←	1
Condition code in bus	←	3
Data strobe	→	1
Halt or MCHK	→	1
System reset	→	1
Power on reset	→	1

Poll group signal lines

Poll (Note 3)	→	1
Poll prime (Note 3)	→	1
Poll propagate (Note 3)	→	1

Notes:

1. Address bus bits 0–15 need only be received in this subset.
2. Bidirectional data bus capability is assumed for this subset; however, if the direction of data flow within a device is fixed (specifically, a read-only device attachment with no write or interrupt capability), the device need not implement bidirectional data drivers and receivers. In this case, the device must reject all commands requiring a transfer in other than the direction implemented by the device. For the interrupt subset (described in "Interrupt Subset" in this chapter), the device must implement bidirectional data bus drivers and receivers.
3. 'Poll' and "poll prime' need only be received, logically ANDed, and redriven on the 'poll propagate' line to maintain continuity of the serial poll mechanism. Any card installed on the channel, even though it does not operate on the channel, must propagate 'poll' and 'poll prime.'

Figure 2-3. Basic subset

Interrupt Subset

The interrupt subset consists of control buses and tags to support an interrupting source on the I/O channel. This subset provides the means to: (1) present interrupt requests to the processor, (2) resolve contention, (3) acknowledge an interrupt, and (4) accept an interrupt.

The interrupt subset, in conjunction with the basic subset, supports DPC devices that are interrupting sources. The I/O signal lines in the interrupt subset are shown in Figure 2-4.

Service group signal lines

Signal name	*Direction*	*Number of lines*
Service gate	→	1
Service gate return	←	1

Poll group signal lines

Signal name	*Direction*	*Number of lines*
Request in bus	←	4
Poll identifier	→	5
Poll	→	1
Poll prime	→	1
Poll propagate	→	1
Poll return	←	1

Figure 2-4. Interrupt subset

Cycle-Steal/IPL Subset

The cycle-steal/IPL subset consists of control buses and tags to support cycle-steal, burst transfer, and IPL operations. This subset provides the means to present cycle-steal requests to the processor, to resolve contention, and to service the cycle-steal transfers. The cycle-steal/IPL subset, in conjunction with the basic and the interrupt subsets, supports devices that cycle-steal and DPC devices capable of IPL. The I/O signal lines in the cycle-steal/IPL subset are shown in Figure 2-5.

Service group signal lines

Signal name	*Direction*	*Number of lines*
Address bus bits 0–15 (Note 1)	←	16
Cycle input indicator	←	1
Cycle byte indicator	←	1
Status bus	→	4
Initiate IPL (Note 2)	→	1
IPL (Note 2)	←	1

Poll group signal lines

Signal name	*Direction*	*Number of lines*
Cycle steal request in	←	1
Burst return (Note 3)	←	1

Notes:

1. Address bits 0–15 must have full bidirectional capability for this subset.
2. Required only for devices supporting IPL. Initiate IPL is not required for devices that only support IPL from a host system.
3. Required only if burst cycle-steal transfers are supported by the device.

Figure 2-5. Cycle-steal/IPL subset

Halt or MCHK. This is an outbound tag received by all I/O devices. The tag means that either: (1) a Halt I/O command has been issued by the program or (2) a machine-check class interrupt (excluding a storage parity check) has occurred. When this tag is detected by an I/O device, the device must disable selection, block poll propagation, and clear any status, states, requests, interface control logic, and registers, with the following exceptions:

- Residual address
- Prepare level and I-bit
- DI, DO, AI, and AO settings
- Timer values
- Those registers not addressable by the software
- Two-channel switch operation monitors

The receiver for the 'halt or MCHK' tag is always enabled.

System Reset. This is an outbound tag received by all I/O devices. The tag is singular in nature and meaning. When the tag is detected, the I/O device must disable selection, block poll propagation, and clear any status, states, requests, registers, and interface control logic, with the following exceptions:

- Residual address
- DI, DO, AI, and AO settings
- Timer values
- Those registers not addressable by the software

During IPL sequences, one system reset has a unique function, as described in "Processor-Initiated IPL" under "Design Considerations for Operational Sequences" in this chapter.

The receiver for this tag is always enabled.

Power On Reset. This is an outbound control line from the power supply to all system components, and is activated on all power on/off sequences. While the line is active, all system components are held in a system reset state. The residual address; DI, DO, AI, and AO settings; timer values; and operation monitors are also reset. The receiver for this line is always enabled.

Each processor and I/O expansion unit on the I/O channel has a self-contained unit power-on reset. These power-on resets are not electrically connected among units.

Poll Group Line Definitions

Request In Bus. This is a 4–bit inbound bus used by an I/O device to request an interrupt. Bits 0–3 of the 'request in bus' are used by I/O devices to request interrupts on levels 0–3, respectively. The level on which the device is to interrupt corresponds to the encoded value in the level field in the Prepare command.

Cycle Steal Request In. This is an inbound tag used by a cycle-stealing device when an access to storage is required.

Poll Identifier. This is a five-bit outbound bus used by the channel to indicate the nature of the poll presently being propagated to the I/O devices. 'Poll identifier' is always recognizable by I/O devices that are capable of cycle-stealing and/or presenting interrupts to the processor. The channel places a value on the poll identifier bus prior to raising the 'poll' tag and holds it valid until a 'poll return' or 'burst return' is received.

The significance of the poll identifier bits is as follows (poll ID bits are shown using logical representation for active/inactive):

Poll identifier bits *0 1 2 3 4*	**Meaning**
0 0 0 0 0	Poll for interrupt level 0
0 0 0 0 1	Poll for interrupt level 1
0 0 0 1 0	Poll for interrupt level 2
0 0 0 1 1	Poll for interrupt level 3
1 0 0 0 0	Quiescent value
1 X X 0 1	Reserved
1 X X 1 0	Reserved
1 X X 1 1	Poll for cycle-steal

The poll identifiers for interrupt levels 4–15 are not used on current processors.

The 4952, 4953, and 4955 processors do not use poll identifier bits 1 and 2; these bits are reserved for future use.

Line name	Direction	I/O pin assignment	Processor driver receiver type	Active level	4952/4953 quiescent level	4955 quiescent level
Address bus bit 0	⟷	B02	C-A	Minus	Note 1	Plus
Address bus bit 1	⟷	B03	C-B	Minus	Note 1	Plus
Address bus bit 2	⟷	B04	C-B	Minus	Note 1	Plus
Address bus bit 3	⟷	B05	C-B	Minus	Note 1	Plus
Address bus bit 4	⟷	B07	C-B	Minus	Note 1	Plus
Address bus bit 5	⟷	B08	C-B	Minus	Note 1	Plus
Address bus bit 6	⟷	B09	C-B	Minus	Note 1	Plus
Address bus bit 7	⟷	B10	C-B	Minus	Note 1	Plus
Address bus bit 8	⟷	B12	C-B	Minus	Note 1	Plus
Address bus bit 9	⟷	D02	C-B	Minus	Note 1	Plus
Address bus bit 10	⟷	D04	C-B	Minus	Note 1	Plus
Address bus bit 11	⟷	D05	C-B	Minus	Note 1	Plus
Address bus bit 12	⟷	D06	C-B	Minus	Note 1	Plus
Address bus bit 13	⟷	D07	C-B	Minus	Note 1	Plus
Address bus bit 14	⟷	D09	C-B	Minus	Note 1	Plus
Address bus bit 15	⟷	D10	C-B	Minus	Note 1	Plus
Address bus bit 16	→	D11	C-D	Minus	Plus	Plus
Address gate	→	M08	C-D	Minus	Plus	Plus
Address gate return	←	M09	C-E	Minus	Plus	Plus
Burst return	←	P04	C-E	Minus	Plus	Plus
Condition code in bit 0	←	D12	C-E	Minus	Plus	Plus
Condition code in bit 1	←	D13	C-E	Minus	Plus	Plus
Condition code in bit 2	←	B13	C-E	Minus	Plus	Plus
Cycle byte indicator (Note 2)	←	P10	C-E (Note 2)	Minus	Plus	Plus
Cycle input indicator (Note 2)	←	P09	C-E (Note 2)	Minus	Plus	Plus
Cycle steal request in	←	M02	C-E	Minus	Plus	Plus
Data bus bit 0	⟷	G02	C-C	Minus	Note 1	Plus
Data bus bit 1	⟷	G03	C-C	Minus	Note 1	Plus
Data bus bit 2	⟷	G04	C-C	Minus	Note 1	Plus
Data bus bit 3	⟷	G05	C-C	Minus	Note 1	Plus
Data bus bit 4	⟷	G07	C-C	Minus	Note 1	Plus
Data bus bit 5	⟷	G08	C-C	Minus	Note 1	Plus
Data bus bit 6	⟷	G09	C-C	Minus	Note 1	Plus
Data bus bit 7	⟷	G10	C-C	Minus	Note 1	Plus
Data bus bit P0	⟷	G12	C-C	Minus	Note 1	Minus
Data bus bit 8	⟷	J02	C-C	Minus	Note 1	Plus
Data bus bit 9	⟷	J04	C-C	Minus	Note 1	Plus
Data bus bit 10	⟷	J05	C-C	Minus	Note 1	Plus
Data bus bit 11	⟷	J06	C-C	Minus	Note 1	Plus
Data bus bit 12	⟷	J07	C-C	Minus	Note 1	Plus
Data bus bit 13	⟷	J09	C-C	Minus	Note 1	Plus
Data bus bit 14	⟷	J10	C-C	Minus	Note 1	Plus
Data bus bit 15	⟷	J11	C-C	Minus	Note 1	Plus
Data bus bit P1	⟷	J12	C-C	Minus	Note 1	Minus

Figure 2-21 (Part 1 of 2). Channel drivers/receivers types and levels

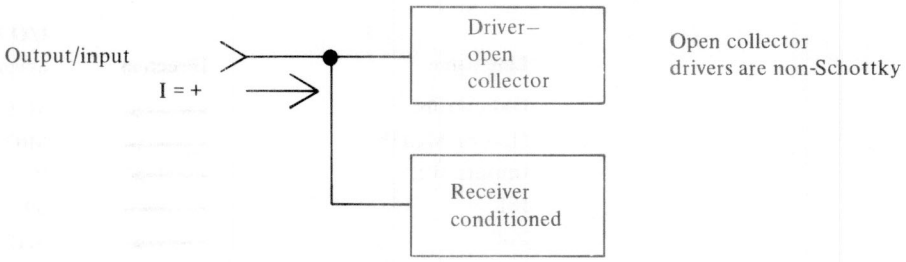
Line name	Direction	I/O pin assignment	Processor driver receiver type	Active level	4952/4953 quiescent level	4955 quiescent level
Data strobe	→	M10	C-D	Minus	Plus	Plus
Halt or MCHK	→	M07	C-D	Minus	Plus	Plus
Initiate IPL	→	P07	C-D	Minus	Plus	Plus
IPL	←	S04	C-E	Minus	Plus	Plus
Poll	→	M12	C-D	Plus	Minus	Minus
Poll identifier bit 0	→	P11	C-D	Minus	Minus	Minus
Poll identifier bit 1	→	S02	Unused	Minus	Plus (Note 3)	Plus (Note 3)
Poll identifier bit 2	→	S03	Unused	Minus	Plus (Note 3)	Plus (Note 3)
Poll identifier bit 3	→	P12	C-D	Minus	Plus	Plus
Poll identifier bit 4	→	P13	C-D	Minus	Plus	Plus
Poll prime	→	M13	C-D (Note 4)	Plus	Minus	Minus
Poll propagate	→	M11		Plus	Minus	Minus
Poll return	←	M04	C-E	Minus	Plus	Plus
Power on reset	→	S05	Note 5	Minus	Plus	Plus
Request in bus bit 0	←	S07	C-E	Minus	Plus	Plus
Request in bus bit 1	←	S08	C-E	Minus	Plus	Plus
Request in bus bit 2	←	S09	C-E	Minus	Plus	Plus
Request in bus bit 3	←	S10	C-E	Minus	Plus	Plus
Reserved	←	S12			Note 6	
Reserved	←	S13			Note 6	
Reserved	←	U02			Note 6	
Reserved	←	U04			Note 6	
Reserved	←	U05			Note 6	
Reserved	←	U06			Note 6	
Reserved	←	U07			Note 6	
Reserved	←	U09			Note 6	
Reserved	←	U10			Note 6	
Reserved	←	U11			Note 6	
Reserved	←	U12			Note 6	
Reserved	←	U13			Note 6	
Service gate	→	P05	C-D	Minus	Plus	Plus
Service gate return	←	P06	C-E	Minus	Plus	Plus
Status bus bit 0	→	J13	C-D	Minus	Plus	Plus
Status bus bit 1	→	G13	C-D	Minus	Plus	Plus
Status bus bit 2	→	M03	C-D	Minus	Plus (Note 7)	Plus
Status bus bit 3	→	P02	C-D	Minus	Plus	Plus
System reset	→	M05	C-D	Minus	Plus	Plus

Figure 2-21 (Part 2 of 2). Channel drivers/receivers types and levels

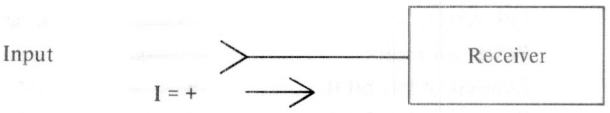
Line name	Direction	I/O Pin assignment	I/O driver/receiver type
Data strobe	→	M10	A-D
Halt or MCHK	→	M07	A-D
Initiate IPL	→	P07	A-D
IPL	←	S04	A-E
Poll	→	M12	A-G
Poll identifier bit 0	→	P11	A-D
Poll identifier bit 1	→	S02	A-D
Poll identifier bit 2	→	S03	A-D
Poll identifier bit 3	→	P12	A-D
Poll identifier bit 4	→	P13	A-D
Poll prime	→	M13	A-G
Poll propagate	→	M11	A-F
Poll return	←	M04	A-E
Power on reset	→	S05	A-D
Request in bus bit 0	←	S07	A-E
Request in bus bit 1	←	S08	A-E
Request in bus bit 2	←	S09	A-E
Request in bus bit 3	←	S10	A-E
Reserved	←	S12	
Reserved	←	S13	
Reserved	←	U02	
Reserved	←	U04	
Reserved	←	U05	
Reserved	←	U06	
Reserved	←	U07	
Reserved	←	U09	
Reserved	←	U10	
Reserved	←	U11	
Reserved	←	U12	
Reserved	←	U13	
Service gate	→	P05	A-D
Service gate return	←	P06	A-E
Status bus bit 0	→	J13	A-D
Status bus bit 1	→	G13	A-D
Status bus bit 2	→	M03	A-D
Status bus bit 3	→	P02	A-D
System reset	→	M05	A-D

Figure 2-24 (Part 2 of 2). Unit-load driver/receiver types

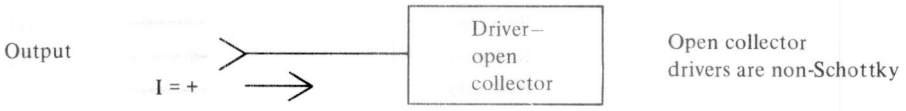
Types A-A, A-B, A-C



Type A-D



Type A-E



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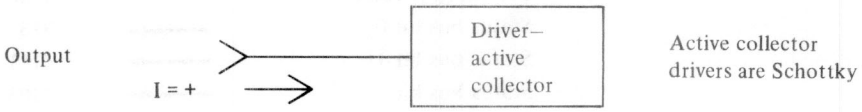

Type A-G

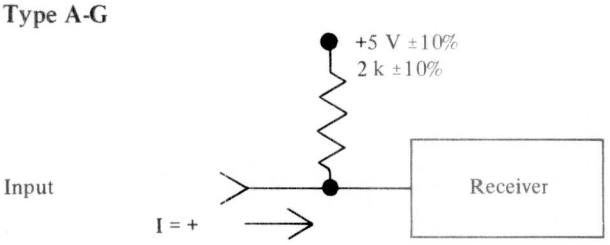

Figure 2-25. Unit-load driver/receiver classification

Type and element	Parameter	Test condition (volts) at node	General unit load-current (mA)		TTL unit load-current (mA)	
			min	max	min	max
A-A driver	High-level output	2.4		+0.110		+0.250
	Low-level output	0.45 (Note 1)	+20		+20	
A-A receiver (conditioned)	High-level input	2.4		+0.04		+0.04
	Low-level input-conditioned inactive	0.2 (Note 2)		−0.1		−0.2
	Low-level input-conditioned active	0.4 (Note 3) 0		−0.75 −0.93		−1.6
A-B, A-C driver	High-level output	2.4		+0.110		+0.250
	Low-level output	0.45 (Note 1)	+16		+16	
A-B, A-C receiver (conditioned)	High-level input	2.4		+0.04		+0.04
	Low-level input-conditioned inactive	0.2 (Note 2)		−0.2		−0.4
	Low-level input-conditioned active	0.4 (Note 3) 0		−0.75 −0.93		−1.6

Figure 2-26 (Part 1 of 2). Unit-load driver/receiver specifications

Type and element	Parameter	Test condition (volts) at node	General unit load-current (mA)		TTL unit load-current (mA)	
			min	max	min	max
A-D receiver	High-level input	2.4		+0.03		+0.04
	Low-level input	0.4 (Note 3) 0		−0.75 −0.93		−1.6
A-E driver	High-level output	2.4		+0.150		+0.250
	Low-level output	0.45 (Note 1)	+16		+16	
A-F driver	High-level output	2.4		−0.4		−0.4
	Low-level output	0.6 (Note 1)	+16		+16	
A-G receiver (without resistor)	High-level input	2.4		+0.04		+0.04
	Low-level input	0.4		−1.6		−1.6

Notes: The information in this section describes the specifications for a unit load on the channel. The specifications apply to an operating range of 0°C to 70°C. Each unit driver and receiver must be no more than one physical element. For example, two half-unit load receivers should not be used in lieu of a one-unit load receiver. Test conditions assume that the supply voltage (V_{CC}) is at maximum or minimum value to produce worst-case conditions. The operating limits of V_{CC} are ±10 percent.

1. Test conditions of less than the listed voltage, with the specified sink capability, also satisfies the specification.
2. The unit-load current versus test-condition voltage is highly nonlinear. Types A-A, A-B, and A-C receivers need not be conditioned if the receiver always satisfies the conditioned inactive unit-load current for a test condition of from 0.0 to 0.45 volt. See "Receiver Conditioning" in this section for further explanation of conditioning.
3. The general unit-load current may be computed at any other test-condition voltage by linear extrapolation, using the two points given.

Figure 2-26 (Part 2 of 2). Unit-load driver/receiver specifications

Each cable carries twenty signal lines, which are arranged so that cable #1 plugs into the top of the A-socket and cable #4 plugs into the bottom of the A-socket.

Line name	Direction	I/O pin assignment	I/O channel cable assignment #1	#2	#3	#4
Address bus bit 0	⟷	B02	B02			
Address bus bit 1	⟷	B03	B03			
Address bus bit 2	⟷	B04	B04			
Address bus bit 3	⟷	B05	B05			
Address bus bit 4	⟷	B07	B07			
Address bus bit 5	⟷	B08	B08			
Address bus bit 6	⟷	B09	B09			
Address bus bit 7	⟷	B10	B10			
Address bus bit 8	⟷	B12	B12			
Address bus bit 9	⟷	D02	D02			
Address bus bit 10	⟷	D04	D04			
Address bus bit 11	⟷	D05	D05			
Address bus bit 12	⟷	D06	D06			
Address bus bit 13	⟷	D07	D07			
Address bus bit 14	⟷	D09	D09			
Address bus bit 15	⟷	D10	D10			
Address bus bit 16	→	D11	D11			
Address gate	→	M08			B08	
Address gate return	←	M09			B09	
Burst return	←	P04			D04	
Condition code in bit 0	←	D12	D12			
Condition code in bit 1	←	D13	D13			
Condition code in bit 2	←	B13	B13			
Cycle byte indicator	←	P10			D10	
Cycle input indicator	←	P09			D09	
Cycle steal request in	←	M02			B02	
Data bus bit 0	⟷	G02		B02		
Data bus bit 1	⟷	G03		B03		
Data bus bit 2	⟷	G04		B04		
Data bus bit 3	⟷	G05		B05		
Data bus bit 4	⟷	G07		B07		
Data bus bit 5	⟷	G08		B08		
Data bus bit 6	⟷	G09		B09		
Data bus bit 7	⟷	G10		B10		
Data bus bit P0	⟷	G12		B12		
Data bus bit 8	⟷	J02		D02		
Data bus bit 9	⟷	J04		D04		
Data bus bit 10	⟷	J05		D05		
Data bus bit 11	⟷	J06		D06		
Data bus bit 12	⟷	J07		D07		
Data bus bit 13	⟷	J09		D09		
Data bus bit 14	⟷	J10		D10		
Data bus bit 15	⟷	J11		D11		
Data bus bit P1	⟷	J12		D12		

Figure 2-28 (Part 1 of 2). I/O channel pin and cable assignments—signal lines

Line name	Direction	I/O pin assignment	I/O channel cable assignment #1	#2	#3	#4
Data strobe	→	M10			B10	
Halt or MCHK	→	M07			B07	
Initiate IPL	→	P07			D07	
IPL	←	S04				B04
Poll	→	M12			B12	
Poll identifier bit 0	→	P11			D11	
Poll identifier bit 1	→	S02				B02
Poll identifier bit 2	→	S03				B03
Poll identifier bit 3	→	P12			D12	
Poll identifier bit 4	→	P13			D13	
Poll prime	→	M13			B13	
Poll propagate	→	M11				
Poll return	←	M04			B04	
Power on reset (see Note)	→	S05				B05
Request in bus bit 0	←	S07				B07
Request in bus bit 1	←	S08				B08
Request in bus bit 2	←	S09				B09
Request in bus bit 3	←	S10				B10
Reserved	←	S12				B12
Reserved	←	S13				B13
Reserved	←	U02				D02
Reserved	←	U04				D04
Reserved	←	U05				D05
Reserved	←	U06				D06
Reserved	←	U07				D07
Reserved	←	U09				D09
Reserved	←	U10				D10
Reserved	←	U11				D11
Reserved	←	U12				D12
Reserved	←	U13				D13
Service gate	→	P05			D05	
Service gate return	←	P06			D06	
Status bus bit 0	→	J13		D13		
Status bus bit 1	→	G13		B13		
Status bus bit 2	→	M03			B03	
Status bus bit 3	→	P02			D02	
System reset	→	M05			B05	

Note: 'Power-on reset' at an I/O socket is the 'power-on reset' from the unit power supply powering the I/O socket. Pin S05 on the 4955 processor A-socket is not connected and is jumpered from S05 of the B-socket when an I/O attachment or repower feature is installed. 'Power-on reset' in the I/O channel cable is the unit 'power-on reset' from the next outboard I/O expansion unit.

Figure 2-28 (Part 2 of 2). I/O channel pin and cable assignments—signal lines

Line name	Direction	I/O pin assignment	TCC pin no.
Address bus bit 0	⟷	B02	W22
Address bus bit 1	⟷	B03	W23
Address bus bit 2	⟷	B04	W24
Address bus bit 3	⟷	B05	W25
Address bus bit 4	⟷	B07	W27
Address bus bit 5	⟷	B08	W28
Address bus bit 6	⟷	B09	W29
Address bus bit 7	⟷	B10	W30
Address bus bit 8	⟷	B12	W32
Address bus bit 9	⟷	D02	W02
Address bus bit 10	⟷	D04	W04
Address bus bit 11	⟷	D05	W05
Address bus bit 12	⟷	D06	W06
Address bus bit 13	⟷	D07	W07
Address bus bit 14	⟷	D09	W09
Address bus bit 15	⟷	D10	W10
Address bus bit 16	→	D11	W11
Address gate	→	M08	Y28
Address gate return	←	M09	Y29
Burst return	←	P04	Y04
Condition code in bit 0	←	D12	W12
Condition code in bit 1	←	D13	W13
Condition code in bit 2	←	B13	W33
Cycle byte indicator	←	P10	Y10
Cycle input indicator	←	P09	Y09
Cycle steal request in	←	M02	Y22
Data bus bit 0	⟷	G02	X22
Data bus bit 1	⟷	G03	X23
Data bus bit 2	⟷	G04	X24
Data bus bit 3	⟷	G05	X25
Data bus bit 4	⟷	G07	X27
Data bus bit 5	⟷	G08	X28
Data bus bit 6	⟷	G09	X29
Data bus bit 7	⟷	G10	X30
Data bus bit P0	⟷	G12	X32
Data bus bit 8	⟷	J02	X02
Data bus bit 9	⟷	J04	X04
Data bus bit 10	⟷	J05	X05
Data bus bit 11	⟷	J06	X06
Data bus bit 12	⟷	J07	X07
Data bus bit 13	⟷	J09	X09
Data bus bit 14	⟷	J10	X10
Data bus bit 15	⟷	J11	X11
Data bus bit P1	⟷	J12	X12

Figure 2-33 (Part 1 of 2). Channel repower feature pin assignments

Line name	Direction	I/O pin assignment	TCC pin no.
Data strobe	→	M10	Y30
Halt or MCHK	→	M07	Y27
Initiate IPL	→	P07	Y07
IPL	←	S04	Z24
Poll	→	M12	Y32
Poll identifier bit 0	→	P11	Y11
Poll identifier bit 1	→	S02	Z22
Poll identifier bit 2	→	S03	Z23
Poll identifier bit 3	→	P12	Y12
Poll identifier bit 4	→	P13	Y13
Poll prime	→	M13	Y33
Poll propagate	→	M11	--
Poll return	←	M04	Y24
Power on reset (see Note)	→	S05	Z25
Request in bus bit 0	←	S07	Z27
Request in bus bit 1	←	S08	Z28
Request in bus bit 2	←	S09	Z29
Request in bus bit 3	←	S10	Z30
Reserved	←	S12	Z32
Reserved	←	S13	Z33
Reserved	←	U02	Z02
Reserved	←	U04	Z04
Reserved	←	U05	Z05
Reserved	←	U06	Z06
Reserved	←	U07	Z07
Reserved	←	U09	Z09
Reserved	←	U10	Z10
Reserved	←	U11	Z11
Reserved	←	U12	Z12
Reserved	←	U13	Z13
Service gate	→	P05	Y05
Service gate return	←	P06	Y06
Status bus bit 0	→	J13	X13
Status bus bit 1	→	G13	X33
Status bus bit 2	→	M03	Y23
Status bus bit 3	→	P02	Y02
System reset	→	M05	Y25

Note: 'Power on reset' at the top-card connector pin Z25 is the 'power-on reset' from the next outboard I/O expansion unit. Neither this 'power-on reset' nor the 'power-on reset' at the bottom of the card are repowered (both of these resets are used in the card for control logic).

Figure 2-33 (Part 2 of 2). Channel repower feature pin assignments

Line name	Direction	I/O pin assignment	Customer card socket
Data strobe	→	M10	B28
Halt or MCHK	→	M07	B25
Initiate IPL	→	P07	D27
IPL	←	S04	B34
Poll	→	M12	B30
Poll identifier bit 0	→	P11	D30
Poll identifier bit 1	→	S02	B32
Poll identifier bit 2	→	S03	B33
Poll identifier bit 3	→	P12	D31
Poll identifier bit 4	→	P13	D32
Poll prime	→	M13	B31
Poll propagate	→	M11	B29
Poll return	←	M04	B23
Power on reset	→	S05	B35
Request in bus bit 0	←	S07	B36
Request in bus bit 1	←	S08	D33
Request in bus bit 2	←	S09	D35
Request in bus bit 3	←	S10	D36
Reserved	←	S12	N-C
Reserved	←	S13	N-C
Reserved	←	U02	N-C
Reserved	←	U04	N-C
Reserved	←	U05	N-C
Reserved	←	U06	N-C
Reserved	←	U07	N-C
Reserved	←	U09	N-C
Reserved	←	U10	N-C
Reserved	←	U11	N-C
Reserved	←	U12	N-C
Reserved	←	U13	N-C
Service gate	→	P05	D25
Service gate return	←	P06	D26
Status bus bit 0	→	J13	D22
Status bus bit 1	→	G13	B20
Status bus bit 2	→	M03	B22
Status bus bit 3	→	P02	D23
System reset	→	M05	B24

Note:
Customer card socket pin D02 provides +5 volts dc; pins D07 and D34 provide ground.

Figure 2-36 (Part 2 of 2). Channel socket adapter pin assignment translation