IBM

Series/1

GA34-0033-3

File No. S1-01

IBM Series/1 User's Attachment Manual

Fourth Edition (September 1979)

This is a major revision of, and obsoletes, GA34-033-2 and Technical Newsletter GN34-0448. This revision includes editorial and technical changes, which incorporate information about the IBM 4952 Processor and the IBM General Purpose Interface Bus (GPIB) Adapter. Because of the extensive changes, revision bars have been omitted; this manual should be reviewed in its entirety.

Use this publication only for the purpose stated in the Preface.

Changes are periodically made to the information herein; any such changes will be reported in subsequent revisions or Technical Newsletters.

It is possible that this material may contain reference to, or information about, IBM products (machines and programs), programming, or services which are not announced in your country. Such references or information must not be construed to mean that IBM intends to announce such IBM products, programming, or services in your country.

Publications are not stocked at the address given below. Requests for copies of IBM publications should be made to your IBM representative or the IBM branch office serving your locality.

This publication could contain technical inaccuracies or typographical errors. A form for readers' comments is provided at the back of this publication. If the form has been removed, address your comments to IBM Corporation, Systems Publications, Department 27T, P.O. Box 1328, Boca Raton, Florida 33432. IBM may use and distribute any of the information you supply in any way it believes appropriate without incurring any obligation whatever. You may, of course, continue to use the information you supply.

Preface

This publication provides reference information to aid in designing logic for communicating with an IBM Series/1 processor through the input/output channel and several designated user attachment features. This information is intended primarily for experienced engineers or technicians. This publication is also useful to customers who need detailed information for connecting their instruments and devices to the various attachment features.

The reader should have a working knowledge of the information in the appropriate IBM Series/1 processor and processor features description manual.

The processor I/O channel architecture, or any aspect of the I/O interfaces described in this publication, may be altered from time to time by IBM or may be withdrawn by IBM in part or in whole.

This manual is organized as follows:

Chapter 1. Introduction describes the I/O channel and the user attachment features.

Chapter 2. Processor I/O Channel describes the channel direct program control (DPC) operations, cycle-steal (CS) operations, interrupts, and initial program load (IPL).

Chapter 3. Timer Feature describes the timer feature, including signal lines, interrupts, electrical characteristics, and physical characteristics.

Chapter 4. Teletypewriter Adapter Feature describes the teletypewriter adapter feature, including interface options, timing sequences, electrical characteristics, and physical characteristics.

Chapter 5. Integrated Digital Input/Output Feature describes the integrated digital input/output feature, including operational, electrical, and physical characteristics.

Chapter 6. Customer Direct Program Control (DPC) Adapter Feature describes the customer direct program control adapter feature, including operational, electrical, and physical characteristics.

Appendix A. General Purpose Interface Bus Adapter, RPQ D02118, describes the Series/1 implementation of the digital interface contained in IEEE Standard 488, including the commands and functions used by the General Purpose Interface Bus (GPIB) Adapter.

Note: Installation instructions are shipped with each system order. These instructions contain the information required for selecting options and device addresses on the I/O attachment feature cards.

Related Publications

Additional publications are listed in the *IBM Series/1 Graphic Bibliography*, GA34-0055.

Contents

Chapter 1. Introduction

A variety of interfaces are provided for attachment of the user's own input/output (I/O) devices and instruments to an IBM Series/1 processor. Serial and parallel data paths, and a multifunction timer are provided. The user may choose one of the I/O adapter features or design an I/O adapter to communicate directly with the processor I/O channel.

Figure 1-1 shows the various methods of attachment and the available attachment features. Each attachment is described in subsequent sections of this chapter.

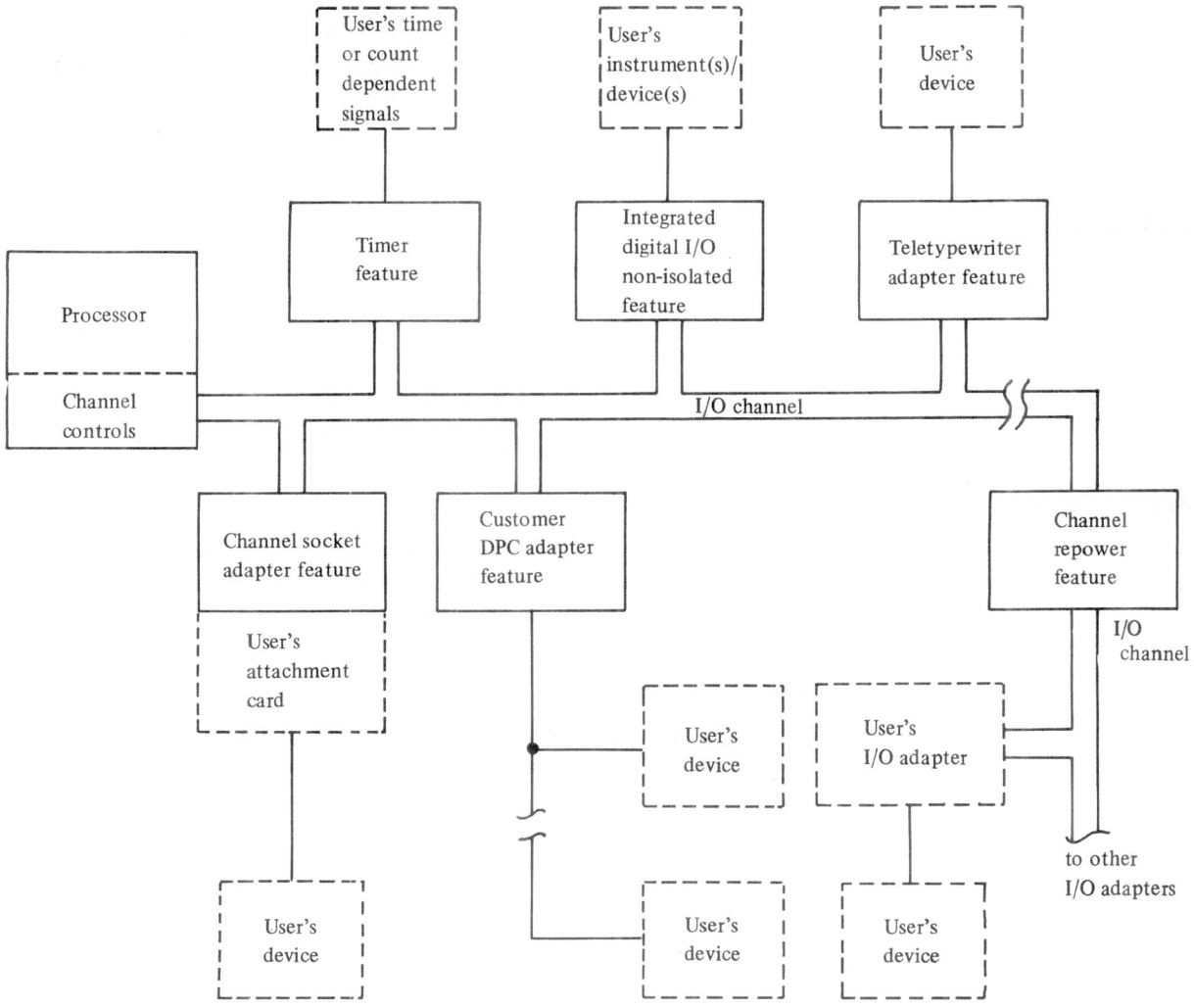


Figure 1-1. Relationship of user attachments to the processor I/O channel

Processor I/O Channel

Input/output devices are attached to the processor through the I/O channel. The channel, which can accommodate 256 device addresses, (1) directs the flow of information between the I/O devices and main storage and (2) contains the facilities for the control of the I/O operations. The channel is asynchronous, with multidropped lines that link the processor resource to its external facilities. I/O channel architecture includes address, control, and data signal lines.

Channel Repower Feature

The channel repower feature isolates and redrives the I/O channel signal and tag lines. The feature is used to extend the channel beyond the processor enclosure.

Channel Socket Adapter Feature

The channel socket adapter feature consists of an IBM printed circuit card that plugs into the backpanel of an IBM Series/1 processor or the IBM 4959 I/O Expansion Unit. The top edge of the IBM printed circuit card has an industry-standard connector that accepts the user's I/O adapter card. To power the user's circuits, +5 volts dc at 3 amperes, maximum, is available at the connector.

I/O Attachment Features

The following I/O attachment features are available:

- Timer feature
- Teletypewriter adapter feature
- Integrated digital I/O nonisolated feature
- Customer direct program control (DPC) adapter feature

Timer Feature

The timer feature card has two separately addressable 16-bit timers. If desired, time base and gating signals can be supplied, by the user, through a connector on the top of the card.

Each timer can generate periodic or aperiodic interrupts with or without the external gate.

Each timer can operate as an interval timer or pulse counter, or it can operate as a self-contained pulse duration counter with end interrupt.

Teletypewriter Adapter Feature

The teletypewriter adapter feature card provides a way of attaching a serial I/O device. This feature provides a logical subset of the Electronic Industries Association (EIA) RS232-C interface. Full-duplex operation and initial program load (IPL) are supported by the adapter.

Attachment to a teletypewriter is by a dc-current loop (isolated or nonisolated). Two other attachment options are offered: a TTL-compatible interface and an EIA voltage-level interface.

Integrated Digital Input/Output (I/O) Nonisolated Feature

The integrated digital I/O nonisolated feature card contains:

- Two 16-point groups of nonisolated digital input/process interrupt (DI/PI)
- Two 16-point groups of nonisolated digital output (DO)

Each group of DI/PI and DO has a 'ready' and a 'sync' line for synchronizing operations with attached devices. The digital points for each group and their associated 'ready' and 'sync' lines are available at three top-card connectors.

Customer Direct Program Control (DPC) Adapter Feature

The direct program control (DPC) adapter feature card supplies a logical subset of the I/O channel architecture. This feature provides a convenient means of attaching I/O devices and subsystems to an IBM Series/1 processor, The interface circuits are TTL compatible. The adapter is designed to perform direct program control functions only. The feature card can be configured to accommodate 4, 8, or 16 I/O device addresses. The adapter allows for interrupt vectoring of 16 interrupt sources.

There are 75 signal lines. These include: 18 data bus out, 18 data bus in, 16 interrupt request in, three function bits, four modifier bits, four device address bits, and 12 control and response lines. The data flow is always 16 bits without parity option or 18 bits with parity option (two parity bits). User attachment is through three top-card connectors.

Customer Access Panel (CAP) Feature

The customer access panel (CAP) feature provides an assembly for mounting optional, quick-disconnect-type connectors for I/O equipment. The assembly can accommodate one timer connector, one teletypewriter connector, and up to four connectors for either the integrated digital I/O feature or the customer direct program control (DPC) feature.

The assembly mounts to the standard EIA RS310B rack-mounting screw holes at the rear of the enclosure frame.

General Purpose Interface Bus Adapter Feature

The IBM Series/1 General Purpose Interface Bus (GPIB) Adapter, RPQ D02118, provides a 65K-byte cycle-steal interface for attaching up to 14 digital I/O devices to an IBM Series/1 processor. The devices attached via the GPIB adapter must conform to the requirements described in IEEE Standard 488-1978.

Chapter 2. Processor I/O Channel

Introduction

Input/output devices communicate with the processor and main storage devices through the processor I/O channel. Attachment of the devices to the channel is through an I/O adapter or I/O attachment logic card.

The channel directs the flow of information between the I/O devices, the processor, and main storage. A maximum of 256 devices can be logically addressed.

The processor I/O channel supports the following basic types of operations:

- Direct program control (DPC) operations—an immediate data transfer is made between main storage and the device for each Operate I/O instruction. The data may consist of one byte or one word. The operation may or may not terminate with an interrupt.
- Cycle-steal operations—an Operate I/O instruction can initiate cycle-stealing data transfers of up to 65,535 bytes (per device control block) between main storage and the device. Cycle-steal operations are overlapped with processing operations. Word or byte transfers, device control block (DCB) chaining, burst mode, and program-controlled interrupts can be supported.
- Interrupt servicing operations—four preemptive priority interrupt levels are available to facilitate device service. The device-interrupt level is assignable by the program, and the device-interrupt capability can be masked under program control.
- Initial program load (IPL) operations—a record consisting of initial instructions for the processor is read into storage from either a local I/O device or from a host system.

The channel provides comprehensive error checking, including time-outs, sequence checking, and parity checking. Reporting of errors, exceptions, and status is accomplished by (1) recording condition codes in the processor during execution of Operate I/O instructions, and (2) recording condition codes and an interrupt information byte (IIB) in the processor during interrupt acceptance. Additional status words may be used by the device, as necessary, to describe its status.

The I/O channel is asynchronous and multidropped. Asynchronous means that there are no timing restrictions inherent in the architecture. The response from a given I/O device triggers the next sequential action rather than a specified timing condition. (Time-out conditions for error detection are not excluded.) An asynchronous channel allows the attachment of devices that have various speeds and technologies over a wide range of distances or delays.

All I/O channel signal lines are TTL-level compatible. This allows the user freedom in the design of I/O channel attachments.

The I/O channel signal lines are distributed internally via the processor backpanel board to each I/O attachment card socket. Distribution of the channel signal lines can be continued by connecting cables or a channel repower feature from a processor I/O socket (usually the A-socket) to an adjacent I/O expansion unit, as the particular processor or configuration requires. Refer to the *IBM Series/1 Configurator*, GA34-0042, for details about the requirements for the use of the repower feature.

IBM I/O attachment cards plug directly into the backpanel sockets. External I/O devices are connected to the attachment cards via top-card connectors.

Two features are available for connecting non-IBM devices directly to the channel: the channel socket adapter feature and the channel repower feature.

- Channel socket adapter feature—this feature consists of an IBM printed circuit card that plugs into the backpanel of the processor unit or I/O expansion unit. An industry-standard connector on the top edge of the IBM printed circuit card accepts the user's I/O adapter card. For further information, see "Socket Adapter Feature" in this chapter.
- Channel repower feature—this feature is a logic card that repowers and isolates the channel signal lines. This card can be installed in any I/O socket, as the last series element on the channel, to allow connection of additional I/O adapters or controllers. For further information, see "Channel Repower Feature" in this chapter.

If the user connects directly to the channel at the backpanel sockets instead of through one of the available features, the unit load, the power, and the physical requirements must be considered. These and other requirements are discussed in subsequent sections of this chapter.

CAUTION: To achieve adequate results, good design practices—both electrical and mechanical—must be adhered to. IBM bears *NO RESPONSIBILITY* for customer logic or hardware.

Functional Description of I/O Channel Signal Lines

The I/O channel consists of 81 signal lines divided into two physical groups: the *service* group and the *poll* group. Each group can operate concurrently and asynchronously with the other group; however, the initiation of sequences on the channel is interdependent.

The service group supports:

- Data and control information transfers
- IPL initiation
- Reset functions

The poll group supports:

- Cycle-steal requests from the devices
- Interrupt requests from the devices
- Acknowlegement of both types of requests

Signal Line Groups

The I/O channel signal lines are shown, by group, in Figures 2-1 and 2-2.

Note: The direction is shown for each line with the assumption that the I/O channel originates on the left and the I/O attachments are on the right.

Service Group Signal Lines

The signal lines associated with the service group are shown in Figure 2-1.

Signal name	*Direction*	*Number of lines*
Address bus bits 0–15	⟷	16
Address bus bit 16	→	1
Data bus	⟷	18
Address gate	→	1
Address gate return	←	1
Service gate	→	1
Service gate return	←	1
Condition code in bus	←	3
Cycle input indicator	←	1
Cycle byte indicator	←	1
Status bus	→	4
Data strobe	→	1
Initiate IPL	→	1
IPL	←	1
Halt or MCHK (machine check)	→	1
System reset	→	1
Power on reset	→	1
Total number of lines		54

Figure 2-1. Service group signal lines

Poll Group Signal Lines

The signal lines associated with the poll group are shown in Figure 2-2.

Signal name	*Direction*	*Number of lines*
Request in bus	←	16
Cycle steal request in	←	1
Poll identifier	→	5
Poll	→	1
Poll prime	→	1
Poll propagate	→	1
Poll return	←	1
Burst return	←	1
Total number of lines		27

Figure 2-2. Poll group signal lines

Functional Subsets of the Signal Lines

The I/O channel signal lines can have subsets, depending on the level of function required by the I/O attachment. In order of increasing level of function, these subsets are:

- Basic subset
- Interrupt subset
- Cycle-steal/IPL subset

Attachment to a subset is a prerequisite for attachment to the next higher level subset.

Basic Subset

The basic subset consists of the buses and tags to support functions initiated by the processor; for example, direct program control (DPC) commands. This includes the data transfers associated with the DPC command itself. The basic subset supports DPC devices that do not interrupt. I/O signal lines in the basic subset are shown in Figure 2-3.

Service group signal lines

Signal name	*Direction*	*Number of lines*
Address bus bits 0–15 (Note 1)	→	16
Address bus bit 16	→	1
Data bus (Note 2)	→	18
Address gate	→	1
Address gate return	←	1
Condition code in bus	←	3
Data strobe	→	1
Halt or MCHK	→	1
System reset	→	1
Power on reset	→	1

Poll group signal lines

Poll (Note 3)	→	1
Poll prime (Note 3)	→	1
Poll propagate (Note 3)	→	1

Notes:

1. Address bus bits 0–15 need only be received in this subset.
2. Bidirectional data bus capability is assumed for this subset; however, if the direction of data flow within a device is fixed (specifically, a read-only device attachment with no write or interrupt capability), the device need not implement bidirectional data drivers and receivers. In this case, the device must reject all commands requiring a transfer in other than the direction implemented by the device. For the interrupt subset (described in "Interrupt Subset" in this chapter), the device must implement bidirectional data bus drivers and receivers.
3. 'Poll' and "poll prime' need only be received, logically ANDed, and redriven on the 'poll propagate' line to maintain continuity of the serial poll mechanism. Any card installed on the channel, even though it does not operate on the channel, must propagate 'poll' and 'poll prime.'

Figure 2-3. Basic subset

Interrupt Subset

The interrupt subset consists of control buses and tags to support an interrupting source on the I/O channel. This subset provides the means to: (1) present interrupt requests to the processor, (2) resolve contention, (3) acknowledge an interrupt, and (4) accept an interrupt.

The interrupt subset, in conjunction with the basic subset, supports DPC devices that are interrupting sources. The I/O signal lines in the interrupt subset are shown in Figure 2-4.

Service group signal lines

Signal name	*Direction*	*Number of lines*
Service gate	→	1
Service gate return	←	1

Poll group signal lines

Signal name	*Direction*	*Number of lines*
Request in bus	←	16
Poll identifier	→	5
Poll	→	1
Poll prime	→	1
Poll propagate	→	1
Poll return	←	1

Figure 2-4. Interrupt subset

Cycle-Steal/IPL Subset

The cycle-steal/IPL subset consists of control buses and tags to support cycle-steal, burst transfer, and IPL operations. This subset provides the means to present cycle-steal requests to the processor, to resolve contention, and to service the cycle-steal transfers. The cycle-steal/IPL subset, in conjunction with the basic and the interrupt subsets, supports devices that cycle-steal and DPC devices capable of IPL. The I/O signal lines in the cycle-steal/IPL subset are shown in Figure 2-5.

Service group signal lines

Signal name	*Direction*	*Number of lines*
Address bus bits 0–15 (Note 1)	←	16
Cycle input indicator	←	1
Cycle byte indicator	←	1
Status bus	→	4
Initiate IPL (Note 2)	→	1
IPL (Note 2)	←	1

Poll group signal lines

Signal name	*Direction*	*Number of lines*
Cycle steal request in	←	1
Burst return (Note 3)	←	1

Notes:

1. Address bits 0–15 must have full bidirectional capability for this subset.
2. Required only for devices supporting IPL. Initiate IPL is not required for devices that only support IPL from a host system.
3. Required only if burst cycle-steal transfers are supported by the device.

Figure 2-5. Cycle-steal/IPL subset

Address Bus Bits 0–15. This is a 16-bit bidirectional bus that is received by all I/O devices. The bus is used on direct program control (DPC) sequences to select and pass commands to the I/O devices. On DPC sequences, address bus bits 0–15 are logically equal to the contents of bits 0–15 of the first word of the IDCB. The channel select bit (IDCB bit 0) on address bus bit 0 can be ignored for device selection.

The address bus is also used on cycle-stealing sequences to present main storage addresses to the channel controls. On cycle-steal service sequences, address bits 0–15, which are driven by the I/O device, correspond to storage address bits 0–15 of the data to be transferred.

Address bus bits 0–15 are not used on interrupt-service sequences.

Address Bus Bit 16. This bit is an outbound tag received by all I/O devices. When active, this tag signals a DPC sequence to the I/O devices. The receiver for this tag is always enabled.

Data Bus. This is an 18-bit bidirectional bus with 16 bits of data and two parity bits (odd parity by byte). The data bus transfers data and control information: (1) between the processor and the I/O devices on DPC and interrupt-service sequences, and (2) between cycle-stealing devices and main storage on cycle-steal service sequences.

On *DPC write sequences*, data bus bits 0–15 are logically equal to the contents of bits 16–31 (second word) of the IDCB. If a single byte is to be transferred to the device, the byte is transferred from bits 24–31 of the IDCB; bits 16–23 should all be 0's. DPC write sequences are specified by address bus bit 1 (IDCB bit 1) equal to a logical 1.

Parity is always maintained for both bytes of the data bus on DPC write sequences; however, certain relaxations of the requirement to check parity on both bytes are allowed if a DPC device is byte-oriented. A *byte-oriented device* is a DPC device that does not use bits 16–23 of the IDCB for any DPC write or control function as specified in bits 1–3 of the IDCB. In this case, the device does not need to examine or parity check data bus bits 0–7 on DPC write or control sequences. A device that uses bits 16–23 of the IDCB for at least one DPC write sequence is not a byte-oriented device. Cycle-stealing devices cannot be byte-oriented devices because they implement the start functions.

On *DPC read sequences*, data bus bits 0–15 are driven by the device, and correspond to bits 16–31 of the IDCB. If a single byte is to be transferred from the device, the byte is transferred on data bus bits 8–15 with data bus bits 0–7 equal to logical 0's. DPC read sequences are specified by address bus bit 1 (IDCB bit 1) equal to logical 0. Parity must be maintained on both bytes of the data bus on DPC read sequences.

On *interrupt-service sequences*, the data bus is used to pass the interrupt ID word to the processor. Data bus bits 0–15 are driven by the device, and correspond to bits 0–15 of the interrupt ID word. The first byte of the interrupt ID word (bits 0–7) is the interrupt information byte; the second byte (bits 8–15) is the device address of the device being serviced.

Parity must be maintained on both bytes of the data bus on interrupt service sequences.

On *cycle-steal service sequences*, the data bus bits have the following meanings:

- *Output, word transfer*—data bus bits 0–15 are logically equal to the contents of the word at the storage address presented by the device; this storage address must be even. The device indicates an output word transfer by presenting 'cycle input indicator' equal to logical 0 and 'cycle byte indicator' equal to logical 0.
- *Input, word transfer*—data bus bits 0–15 are driven by the device and correspond to the word to be placed at the storage address presented by the device; this storage address must be even. The device indicates an input word transfer by presenting 'cycle input indicator' equal to logical 1 and 'cycle byte indicator' equal to logical 0.
- *Output, byte transfer*—the main storage address presented by the device determines the alignment of the byte on the data bus. If the storage address is even, data bus bits 0–7 are logically equal to the contents of the byte at the storage address. If the storage address is odd, data bus bits 8–15 are logically equal to the contents of the byte at the storage address. The device indicates an output byte transfer by presenting 'cycle input indicator' equal to logical 0 and 'cycle byte indicator' equal to logical 1.
- *Input, byte transfer*—the device must align the byte on the data bus according to the storage address being presented. If the storage address is even, data bus bits 0–7 are driven by the device and correspond to the byte to be placed at the storage address. If the storage address is odd, data bus bits 8–15 are driven by the device and correspond to the byte to be placed at the storage address. The device indicates an input by presenting 'cycle input indicator' equal to logical 1 and 'cycle byte indicator' equal to logical 1.

The I/O architecture allows both byte and word cycle-steal data transfers during the execution of a given cycle-steal operation. For example, an operation transferring an even number of bytes into a data table on an odd storage boundary could transfer one byte, then a number of words, and then end with a byte transfer.

Parity is maintained on both bytes of the data bus during cycle-steal output transfers. I/O devices must check both bytes of the data bus regardless of whether a word or byte is being transferred. Parity must be maintained on both bytes of the data bus on cycle-steal input transfers.

During byte transfers, the channel or device must maintain a stable data bus and parity for purposes of parity checking by the receiver of the data. However, the logical value of the particular byte not being used does not have to be specified because it is parity checked only. For output byte transfers, the value of the unused byte may be different on each transfer and may be different among the Series/1 processors. For input byte transfers, most device attachments, as a matter of practice, have found it simplest to zero out the unused byte and force the parity bit accordingly.

Address Gate. This is an outbound tag used during DPC sequences. This tag signals a device that it can respond to initial selection and begin execution of the command specified by bits 0–7 of the address bus.

Address Gate Return. This is an inbound tag used by the selected device during a DPC sequence. This tag signals: (1) the reception of 'address gate,' (2) the activation of 'condition code in bus,' and (3) the activation of 'data bus' for a read sequence.

Service Gate. This outbound tag signals the device *that last captured a poll* that a cycle-steal or interrupt-service sequence can begin. The I/O device detects the leading edge of this tag following a poll capture to begin the sequence; this is called service gate capture.

Service Gate Return. This is an inbound tag used by a device to signal a service gate capture and activation of 'address bus' (on a cycle-steal sequence), 'data bus,' 'condition code in bus,' and other tags as required by the particular cycle-steal or interrupt-service sequence.

Condition Code In Bus. This is a three-bit, binary encoded inbound bus used by the I/O device on DPC, interrupt, and cycle-steal sequences.

On DPC and interrupt-service sequences, the 'condition code in bus' corresponds to the condition code indicators in the level status register (LSR) as follows:

Condition code in bit	LSR indicator
0	Even
1	Carry
2	Overflow

On cycle-steal service sequences, the 'condition code in bus' is used by the device to pass the address key to the channel. On cycle-steal data transfers, condition code bits 0–2 are logically equal to the cycle-steal address key. This key is bits 5–7 of the DCB control word previously fetched by the device. During cycle-steal transfers for fetching the DCB and for reporting residual status, a value of logical 0 is used for the address key. During IPL cycle-steal transfers, a value of logical 0 is also used for the address key.

Cycle Input Indicator. This is an inbound tag used by the device on a cycle-steal service sequence. This tag signals the channel that the cycle-steal is either: (1) an output from storage or (2) an input to storage. When the indicator is a logical 0, an output from storage is indicated; when the indicator is a logical 1, an input to storage is indicated.

Cycle Byte Indicator. This is an inbound tag used by the device on a cycle-steal service sequence. This tag signals the channel that the cycle-steal is either: (1) a word transfer or (2) a byte transfer. When the indicator is a logical 0, a word transfer is indicated; when the indicator is a logical 1, a byte transfer is indicated.

Status Bus. This is an outbound four-bit bus used by the channel on a cycle-steal service sequence. The bus signals the device being serviced of any errors that the channel has detected. The bus is bit-significant, as follows:

Status bus bit	Meaning	IPL meaning
0	Storage data check	Primary device
1	Invalid storage address	Alternate device
2	Protect check	
3	Interface data check	

If an error is indicated on cycle-steal service sequences that are not a part of IPL, the device retains this information for presentation to the software via ISB bits 4–7 at interruption time. Cycle-steal operations are terminated and an exception interrupt is presented. If an error is indicated on IPL cycle-steal sequences, the device terminates cycle-steal operations, but remains in an IPL state with the 'IPL' line active and does not present an end interrupt. Therefore, it is not necessary that status bus bits be recorded during IPL for later presentation. DPC devices supporting IPL should especially note this.

Bits 0 and 1 of the status bus are also used to select the primary and alternate IPL source, respectively. The appropriate bit of the status bus is activated with the 'initiate IPL' signal to accomplish this selection. Only one device can be configured as a primary IPL source and only one device can be configured as an alternate IPL source at any one time on the I/O channel attached to the processor.

Data Strobe. This is an outbound tag to the I/O device on: DPC, interrupt, or cycle-steal service sequences. This tag can be used by I/O devices to: (1) accomplish control actions, (2) register data on outbound transfers, and (3) accomplish appropriate data resets on inbound transfers. 'Data strobe' always occurs on normal DPC write, cycle-steal, and interrupt-service sequences. On DPC read sequences, 'data strobe' is not activated if the channel detects a parity error.

Initiate IPL. This is an outbound tag from the channel to the IPL source when the IPL is initiated by the processor Load key. The 'initiate IPL' tag is singular in nature and meaning, and signals the IPL source that the processor requires an IPL. The receiver for this tag is always enabled.

Bits 0 and 1 of the status bus are used for selecting the primary and alternate sources, respectively; see "Status Bus" in this section.

IPL. This is an inbound tag (1) from the IPL source, activated in response to the 'initiate IPL' tag or (2) from a host system, to signal the processor that the host is initiating an IPL action. The storage load itself takes place via the cycle-steal mechanism from the selected device or from the host system.

Halt or MCHK. This is an outbound tag received by all I/O devices. The tag means that either: (1) a Halt I/O command has been issued by the program or (2) a machine-check class interrupt (excluding a storage parity check) has occurred. When this tag is detected by an I/O device, the device must disable selection, block poll propagation, and clear any status, states, requests, interface control logic, and registers, with the following exceptions:

- Residual address
- Prepare level and I-bit
- DI, DO, AI, and AO settings
- Timer values
- Those registers not addressable by the software
- Two-channel switch operation monitors

The receiver for the 'halt or MCHK' tag is always enabled.

System Reset. This is an outbound tag received by all I/O devices. The tag is singular in nature and meaning. When the tag is detected, the I/O device must disable selection, block poll propagation, and clear any status, states, requests, registers, and interface control logic, with the following exceptions:

- Residual address
- DI, DO, AI, and AO settings
- Timer values
- Those registers not addressable by the software

During IPL sequences, one system reset has a unique function, as described in "Processor-Initiated IPL" under "Design Considerations for Operational Sequences" in this chapter.

The receiver for this tag is always enabled.

Power On Reset. This is an outbound control line from the power supply to all system components, and is activated on all power on/off sequences. While the line is active, all system components are held in a system reset state. The residual address; DI, DO, AI, and AO settings; timer values; and operation monitors are also reset. The receiver for this line is always enabled.

Each processor and I/O expansion unit on the I/O channel has a self-contained unit power-on reset. These power-on resets are not electrically connected among units.

Request In Bus. This is a 16-bit inbound bus used by an I/O device to request an interrupt. Bits 0–15 of the 'request in bus' are used by I/O devices to request interrupts on levels 0–15, respectively. Only levels 0–3 are used on current processors. The level on which the device is to interrupt corresponds to the encoded value in the level field in the Prepare command.

Cycle Steal Request In. This is an inbound tag used by a cycle-stealing device when an access to storage is required.

Poll Identifier. This is a five-bit outbound bus used by the channel to indicate the nature of the poll presently being propagated to the I/O devices. 'Poll identifier' is always recognizable by I/O devices that are capable of cycle-stealing and/or presenting interrupts to the processor. The channel places a value on the poll identifier bus prior to raising the 'poll' tag and holds it valid until a 'poll return' or 'burst return' is received.

The significance of the poll identifier bits is as follows (poll ID bits are shown using logical representation for active/inactive):

Poll identifier bits *0 1 2 3 4*	Meaning
0 0 0 0 0	Poll for interrupt level 0
0 0 0 0 1	Poll for interrupt level 1
0 0 0 1 0	Poll for interrupt level 2
0 0 0 1 1	Poll for interrupt level 3
0 0 1 0 0	Poll for interrupt level 4
0 0 1 0 1	Poll for interrupt level 5
0 0 1 1 0	Poll for interrupt level 6
0 0 1 1 1	Poll for interrupt level 7
0 1 0 0 0	Poll for interrupt level 8
0 1 0 0 1	Poll for interrupt level 9
0 1 0 1 0	Poll for interrupt level 10
0 1 0 1 1	Poll for interrupt level 11
0 1 1 0 0	Poll for interrupt level 12
0 1 1 0 1	Poll for interrupt level 13
0 1 1 1 0	Poll for interrupt level 14
0 1 1 1 1	Poll for interrupt level 15
1 0 0 0 0	Quiescent value
1 0 1 0 0	Reserved
1 1 0 0 0	Reserved
1 1 1 0 0	Reserved
1 X X 0 1	Reserved
1 X X 1 0	Reserved
1 X X 1 1	Poll for cycle-steal

The poll identifiers for interrupt levels 4–15 are not used on current processors.

Poll and Poll Prime. The 'poll' tag is a serially propagated tag generated by the channel to resolve contention between multiple devices requesting interruptions on the same level and cycle-steal requests. Each I/O device receives the 'poll' tag and redrives it to the next device on the I/O channel via its 'poll propagate' output line.

The 'poll' and 'poll prime' tags are always recognizable by an I/O device that is capable of presenting interrupts or cycle-stealing. An I/O device recognizes a poll as the leading edge of the logical AND of 'poll' and 'poll prime.' The device does a logical compare between the poll ID bits on the interface and the ID bits in its prepare register. An equal compare of the poll ID Bits ANDed with 'poll' and 'poll prime' is called poll capture. Once the poll is captured, an I/O device can then respond with 'poll return' or 'burst return.' If the poll capture does not occur, the 'poll' tag is propagated to the next device on the I/O channel.

Because of the serial nature of the poll mechanism, the relative physical position of I/O attachments on the channel is a major determinant of the priority for servicing contending cycle-steal requests and for servicing contending interrupt requests on the same interrupt level. Those attachments located in positions nearer to the processor are the first elements on the serial poll chain and are effectively of higher priority.

To facilitate the removal of an I/O attachment card from the I/O channel without interrupting the poll propagation, a bypass mechanism is provided (refer to Figure 2-6). The 'poll prime' tag received by I/O attachment card N+2 is the same line that I/O attachment card N+1 receives as its 'poll' tag. If I/O attachment card N is removed, the 'poll' tag input to attachment card N+1 and the 'poll prime' input to attachment card N+2 appear as a logical 1. The 'poll prime' input to attachment card N+1 then follows the 'poll propagate' output of attachment card N-1.

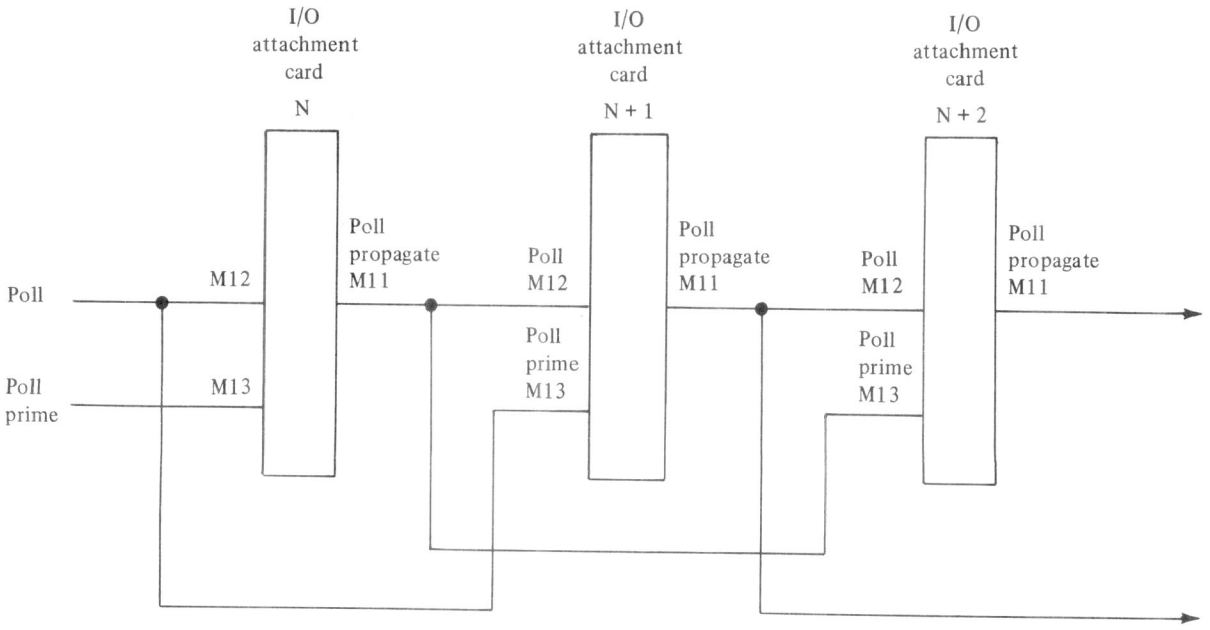


Figure 2-6. Poll bypass mechanism

If an I/O device does not present interrupt or cycle-steal requests, the 'poll' and 'poll prime' tags are received, logically ANDed, and then redriven to the 'poll propagate' output. Cards that use an I/O slot on the channel, but are never logically connected to the channel as a device attachment, must also implement this logical ANDing and redrive capability.

Notes:

1. The poll bypass function applies on and between the processor and I/O expansion units.
2. The cable slots and repower card are not considered to be an I/O attachment for purposes of the poll bypass mechanism (it is not permissible to leave an empty I/O slot on each side of the repower card).

Poll Propagate. This outbound tag is sent by an I/O device when it receives a poll that it has not captured.

Poll Return. This is an inbound tag sent by an I/O device to signal the channel that a poll capture for an interrupt poll or for a non-burst cycle-steal service poll has taken place. It is not used to signify that a burst transfer is required.

Burst Return. This is an inbound tag sent by an I/O device to signal the channel that a poll capture (cycle-steal only) has taken place and that a burst transfer is required. Once 'burst return' is activated, the next leading edge of a 'service gate' tag signals the beginning of the burst transfer. During the burst operation, all other channel-attached devices are precluded from using the channel. 'Service gate'/'service gate return' "handshaking," between the channel and the I/O device, continues until the 'burst return' tag is dropped. An I/O device deactivates the 'burst return' tag at the rise of the 'service gate' tag for the last transfer. Under program control, burst mode is used only if so specified in the DCB control word. A device capable of supporting burst mode must also be capable of non-burst operations. (DCB fetching is always done in non-burst mode.) Burst mode is not precluded for IPL transfers.

Processor I/O Channel Operational Characteristics

Operational Sequences on the Channel

Operations on the processor I/O channel are performed by the following major signal sequences, utilizing either the service group, the poll group, or a combination of both:

- DPC sequence (service group)—a write or read transfer initiated by an Operate I/O instruction. The sequence terminates after one byte or one word is transferred.
- Interrupt-service sequence (service group)—initiated by a poll capture following an interrupt request from an I/O device. The sequence is terminated after the interrupt ID word is transferred.
- Cycle-steal service sequence (service group)—an input or output transfer initiated by a poll capture after a cycle-steal request from the I/O device. The sequence terminates after one byte- or word-transfer unless burst mode is active.
- Poll sequence (poll group)—initiated by either an interrupt request or a cycle-steal request. The poll is either propagated or captured by an I/O device. If the poll is captured, the I/O device returns a 'poll return' tag to indicate either (1) the capture of an interrupt poll or (2) a single cycle-steal transfer. The device returns the 'burst return' tag for multiple cycle-steal transfers.
- Processor-initiated IPL sequence (service and poll group)—initiated when the Load key on the console is pressed. The sequence terminates when the I/O device has transferred the complete IPL record.
- Host-initiated IPL sequence (service and poll groups)—initiated by a signal from the I/O attachment that connects the I/O channel to the host processor. The sequence terminates when the complete IPL record has been transferred.
- Reset sequences—(1) initiated by the 'halt or MCHK' tag when a Halt I/O command is issued or when a machine-check interrupt occurs, or (2) initiated when the system Reset key on the console is pressed.

The service and poll groups operate concurrently and asynchronously to each other. This characteristic is a major operational and design consideration. However, some of the sequences occurring on the I/O channel are interdependent. Figure 2-7 is a block diagram illustrating the architectural interdependencies of the major channel sequences from the viewpoint of a group of devices in normal operation. This diagram does not attempt to show contention resolution in the channel or provide a system level description. The IPL and reset sequences are of a special nature. IPL sequences use the poll and service groups in combination and involve operations with only one specific device and with no other device active. Resets are entirely asynchronous and affect operations on both groups.

The inputs on the left side of the diagram are:

1. A processor interrupt poll request and a cycle-steal request to the poll group. The processor generates a request for an interrupt poll only after the priority interrupt algorithm is satisfied and the processor can accept the interrupt. The cycle-steal request is generated by I/O devices on the channel itself.
2. A processor DPC request to the service group, which is done inline with the execution of an Operate I/O instruction.

Although the poll group and service group resources can be active simultaneously, each group can have only one of its possible transactions active at a time. Therefore, the inputs (requests) to each group must be mutually exclusive at the instant in time the group becomes free to gate another transaction. If the sources of the inputs are running asynchronously, then contention among the requests must be resolved. Although input relationships and contention resolutions are not shown in the diagram, the following can be assumed:

- The processor interrupt poll request and the processor DPC requests are mutually exclusive. This occurs because the processor cannot perform priority interrupt acceptance and execute an Operate I/O instruction at the same time.
- Contention is resolved between processor interrupt poll and cycle-steal requests at the input to the poll group at the time the poll group becomes free to gate another transaction.
- Contention is resolved between processor DPC and poll group requests at the input to the service group at the time the service group becomes free to gate another transaction block.

For example, assume that a processor interrupt poll request becomes active and is gated into the "poll for interrupt" block. This starts the polling sequence. When the poll for interrupt sequence is complete, the poll group resource is waiting for the service group. When the service group beocmes available, the interrupt acceptance block is gated, thus tying up the service group. However, as soon as the interrupt acceptance block is gated, the poll group is free to do further polling concurrent with the service group.

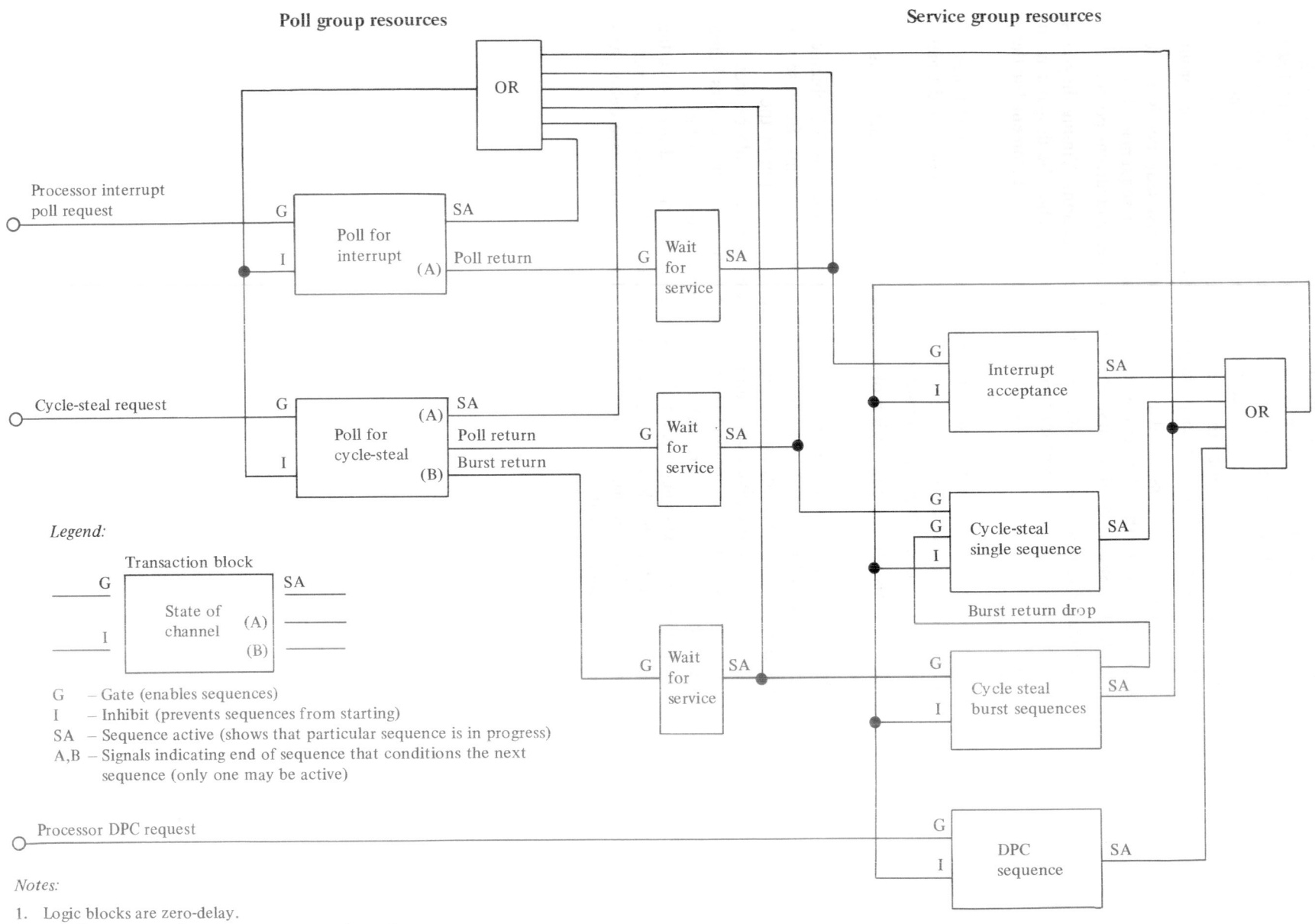
As another example, assume that the cycle-steal burst sequence is active. Figure 2-7 shows that this sequence degates all other sequences. Note also that the last sequence of a burst operation enables concurrent polling.

Each major sequence is described in subsequent sections. Timing diagrams are used to show the important timing relationships that the designer needs to adhere to (or be aware of) when designing an I/O attachment for the I/O channel.

The designer has no control over, but must be aware of, channel times (CT). The designer does have control of the attachment-controlled times (T-times), because these are considered dependent times.

The diagrams use the convention of an up level to denote an active tag or a valid bus value.

The designer should ensure that the signals presented to the I/O channel meet the specified T-times, as shown on the timing diagrams. Because the designer does not control the loading, as seen at the output of the interface drivers in a given configuration, these timings should be met, assuming the maximum loading permissible for the particular drivers being used. There are cases where differences in driver delays must be considered. For example, certain signals must be deactivated prior to a tag being dropped at the device adapter interface. In such cases, one driver can be considered at nominal delay and the other at worst-case delay, with both at maximum load.



Notes:

1. Logic blocks are zero-delay.
2. A poll sequence and service sequence may be active simultaneously, when allowed.

Figure 2-7. Channel sequence interdependencies

DPC Sequence Description

Refer to Figure 2-8. DPC write and DPC read sequences are executed as follows:

1. 'Address bus bits 0–15' and 'address bus bit 16' (and 'data bus' on write sequences) are activated by the channel. These buses are held valid until the fall of 'address gate return,' as seen at the processor channel input.

   The activation of address bus bit 16 causes all I/O attachments to compare address bus bits 8–15 (the device address) with the attachment's assigned device address(es). An equal comparison constitutes DPC selection of the device. Upon selection, the device examines the command in address bus bits 0–7 (and the data bus, for proper parity on write sequences), and applicable device internal conditions necessary for determining command acceptance and I/O instruction condition code reporting. No specific device action or state change must occur as a result of the selection and examination of conditions relative to the command itself until: (1) 'address gate' is recognized by the selected device for write sequences, or (2) 'data strobe' is recognized by the selected device for read sequences. For write sequences, the device should not change state until 'data strobe' is recognized, except during execution of a Device Reset command. If an I/O device has an interrupt request active on the interface and executes a Device Reset or Prepare command, the device, as appropriate, drops its request or alters its requested level prior to the deactivation of 'data strobe,' as seen at the device interface.

2. 'Address gate' is deskewed and activated on the channel. The deskew time, CT1, between the last valid signal of 'address bus' (and 'data bus' on write sequences) and the activation of 'address gate,' measured at the device interface, is 200 nanoseconds, minimum. Upon recognition of the 'address gate' by the selected device, the device activates the 'condition code in bus' (and the 'data bus' on read sequences) and then activates 'address gate return.'

   The 'condition code in bus' (and 'data bus' on read sequences) must be activated prior to 'address gate return,' as seen at the device interface. These buses must be held valid and must not change in value until the deactivation of 'address gate' and 'data strobe' at the device interface.

   The permissible delay, T2, from 'address gate' to 'address gate return,' as seen at the device interface, is 3 microseconds, maximum. 'Address gate return' is timed out by the channel. If 'address gate return' does not become active at the processor channel input within the time-out period, condition code 0 (device not attached) is returned by the channel to the I/O instruction, and the sequence is terminated as follows: 'address gate' and 'address bus' (and 'data bus' on write sequences) are deactivated. 'Data strobe' is not activated. 'Address gate' is deactivated prior to the deactivation of 'address bus,' as seen at the device interface.

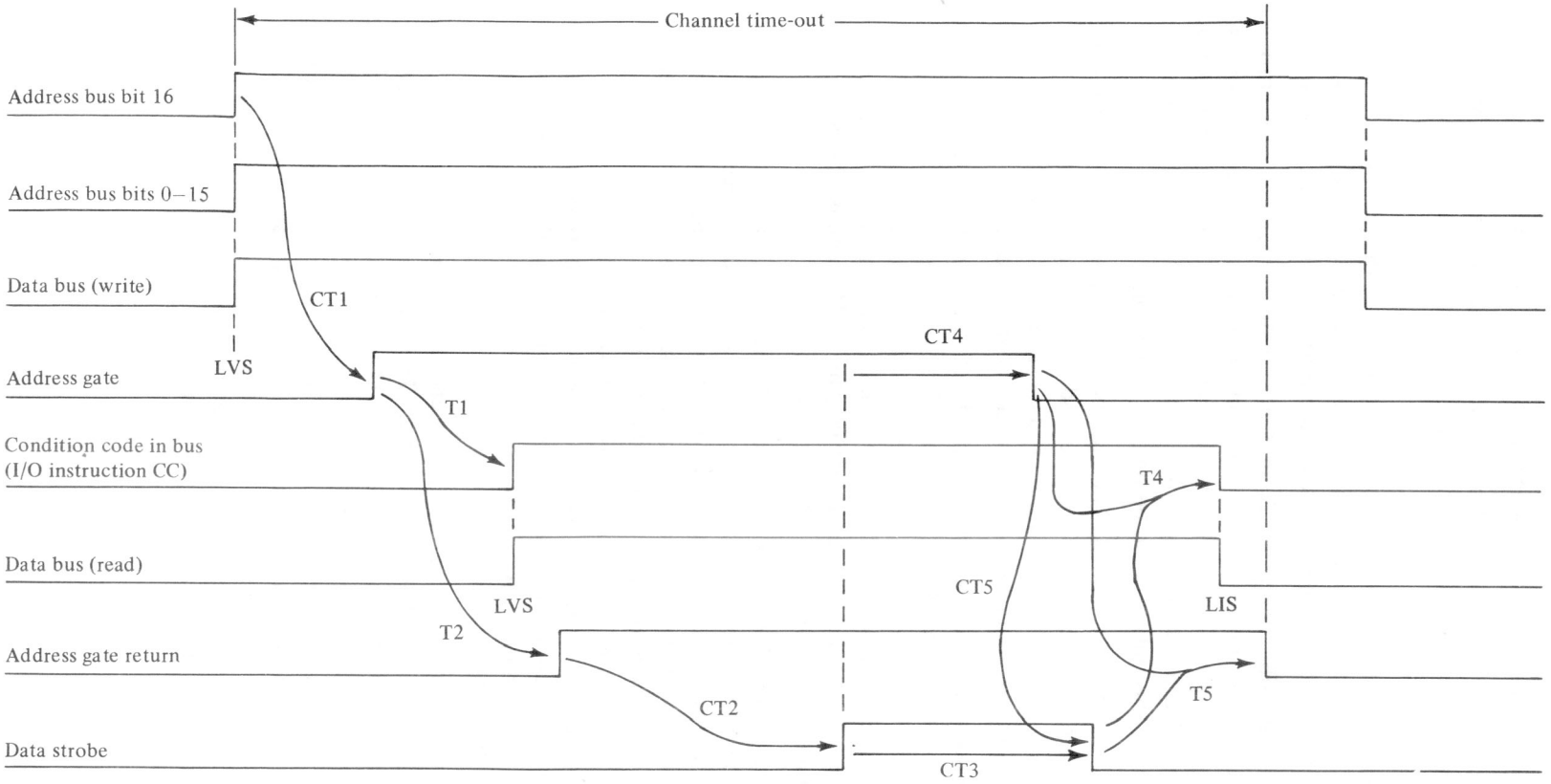
   The permissible delay, T2, allows device attachments further time to resolve conditions for command acceptance or to initiate interlocked activation with further outbound logic. However, unless such functions are necessary, 'address gate return' should be activated as soon as possible for performance reasons.

3. 'Data strobe' is activated. The time between 'address gate return' and 'data strobe' activation, CT2, is 100 nanoseconds, minimum, as seen at the device interface. The duration of 'data strobe,' CT3, as seen at the device interface, is 200 nanoseconds, minimum. If a parity error is detected by the channel during a read sequence, 'data strobe' is not activated.

4. 'Data strobe' (if it has been activated) and 'address gate' are deactivated simultaneously at the processor channel output. As denoted by the relationship of CT3 and CT4 in Figure 2-8, 'data strobe' may extend beyond the active envelope of 'address gate' by 100 nanoseconds, maximum, but the overlap of 'data strobe' and 'address gate' is 100 nanoseconds, minimum, as seen at the device interface.

5. Upon the deactivation of both 'address gate' and 'data strobe,' the device deactivates the 'condition code in bus' (and 'data bus' on read sequences), and 'address gate return.' The 'condition code in bus' (and 'data bus' on read sequences) must be deactivated prior to the deactivation of 'address gate return.' The permissible delay, T5, from the deactivation of both 'address gate' and 'data strobe' to the deactivation of 'address gate return' is 3 microseconds, maximum. This delay allows the device attachments to generate additional strobes, to do additional resetting, and to accomplish interlocked deactivation with outbound logic. However, unless such functions are necessary, 'address gate' should be deactivated as soon as possible for performance reasons. All device actions for the command must take place before deactivating 'address gate return.'

6. The total duration of the DPC sequence is timed out by the channel for error-detection purposes. The total duration is measured as the time from activation of 'address bus bit 16' to the deactivation of 'address gate return.' If 'address gate return' is not deactivated within the time-out, a machine check occurs and the channel activates the 'halt or MCHK' line. Under normal operation, if the device attachment adheres to the specified times over which it has control, the total duration of the sequence is within this channel time-out.



Timings:

$0 \leq T1 < T2 \leq 3\ \mu s$
$0 \leq T4 < T5 \leq 3\ \mu s$
$200\ ns \leq CT1$
$100\ ns \leq CT2$
$200\ ns \leq CT3$
$0 \leq CT5 \leq 100\ ns$

Key:

CT = channel times.
T = attachment-controlled times.
LVS = last valid signal, occurring in time, of a group of signals being activated on the channel. The group is shown linked by short, dotted lines on the timing diagram.
LIS = last invalid signal, occurring in time, of a group of signals being deactivated on the channel. The group is shown linked by short, dotted lines on the timing diagram.

Figure 2-8. DPC sequence timing diagram

Interrupt-Service Sequence Description

Refer to Figure 2-9. An interrupt-service sequence is executed as follows:

1. 'Service gate' is activated. The device detecting the first leading edge of 'service gate' activation following a poll capture is the selected device for the service sequence. This is called service gate capture.

   'Service gate' is propagated outbound from the processor so that the priority is determined by the sequence from the processor for each interrupt level.

2. Upon service gate capture, the device activates the 'condition code in bus,' the 'data bus,' and then 'service gate return.' 'Condition code in bus' and 'data bus' must be activated prior to 'service gate return.'

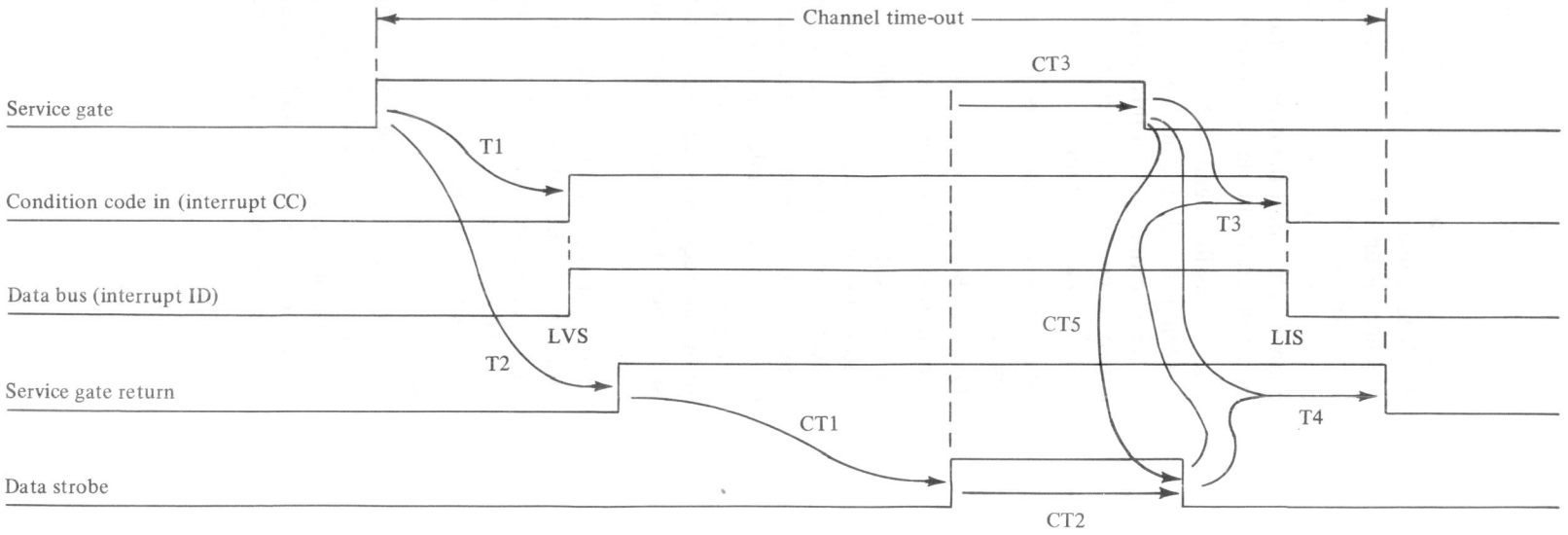
   The permissible delay, T2, from 'service gate' to 'service gate return,' as seen at the device interface, is 3 microseconds, maximum. There is no specific time-out on this delay. As with DPC sequences, this delay is provided for attachment convenience; however, for performance reasons, this delay should be held to a minimum.

3. 'Data strobe' is activated. The time between 'service gate return' and 'data strobe,' CT1, is 100 nanoseconds, minimum, as seen at the device interface. The duration of 'data strobe,' CT2, is 200 nanoseconds, minimum, as seen at the device interface.

4. 'Service gate' and 'data strobe' are deactivated simultaneously at the processor channel output. As denoted by the relationship of CT2 and CT3 in Figure 2-9, 'data strobe' may extend beyond the active envelope of 'service gate' by 100 nanoseconds, maximum, but the overlap of 'data strobe' and 'service gate' is 100 nanoseconds, minimum, as seen at the device interface.

5. Upon the deactivation of both 'service gate' and 'data strobe,' the device deactivates the 'condition code in bus' and 'service gate return.' The 'condition code in bus' and 'data bus' must be deactivated prior to the deactivation of 'service gate return,' as seen at the device interface. The permissible delay, T4, from the deactivation of both 'service gate' and 'data strobe' to the deactivation of 'service gate return' is 3 microseconds, maximum, as seen at the device interface. Again, this delay is for attachment convenience; however, the delay should be held to a minimum. All device action for the service must take place prior to dropping 'service gate return.'

6. The total duration of the interrupt-service sequence is timed out by the channel for error-detection purposes. The total duration is measured from the activation of 'service gate' to the deactivation of 'service gate return.' If, within the time-out, 'service gate return' either: (1) does not become active with 'service gate' active or (2) does not deactivate after it has become active, a machine check occurs and the channel activates the 'halt or MCHK' line. Under normal operation, if the device attachment adheres to the specified times over which it has control, the total duration of the sequence is within this channel time-out.



Timings:

$0 \leq T1 < T2 \leq 3\ \mu s$
$0 \leq T3 < T4 \leq 3\ \mu s$
$100\ ns \leq CT1$
$200\ ns \leq CT2$
$0 \leq CT5 \leq 100\ ns$

Key:

CT = channel times.
T = attachment-controlled times.
LVS = last valid signal, occurring in time, of a group of signals being activated on the channel. The group is shown linked by short, dotted lines on the timing diagram.
LIS = last invalid signal, occurring in time, of a group of signals being deactivated on the channel. The group is shown linked by short, dotted lines on the timing diagram.

Figure 2-9. Interrupt-service sequence timing diagram

Cycle-Steal Service Sequence Description

Refer to Figure 2-10. Cycle-steal input and output sequences are executed as follows:

1. 'Service gate' is activated. The device detecting the first leading edge of the 'service gate' activation following a poll capture is the selected device for the cycle-steal service sequence. This is called service gate capture.

2. Upon service gate capture, the device activates the 'address bus' and, if a byte transfer is to take place, 'cycle byte indicator.' If the sequence is an input transfer, 'data bus' and 'cycle input indicator' are also activated. These signals must be activated prior to the activation of 'service gate return,' and they must be held valid and must not change value until the deactivation of 'service gate' and 'data strobe,' as measured at the device interface.

   The permissible delay, T2, from 'service gate' to 'service gate return,' as seen at the device interface, is 3 microseconds, maximum. There is no specific time-out on this delay. The delay is provided for convenience only; however, for performance reasons, this delay should be held to a minimum.

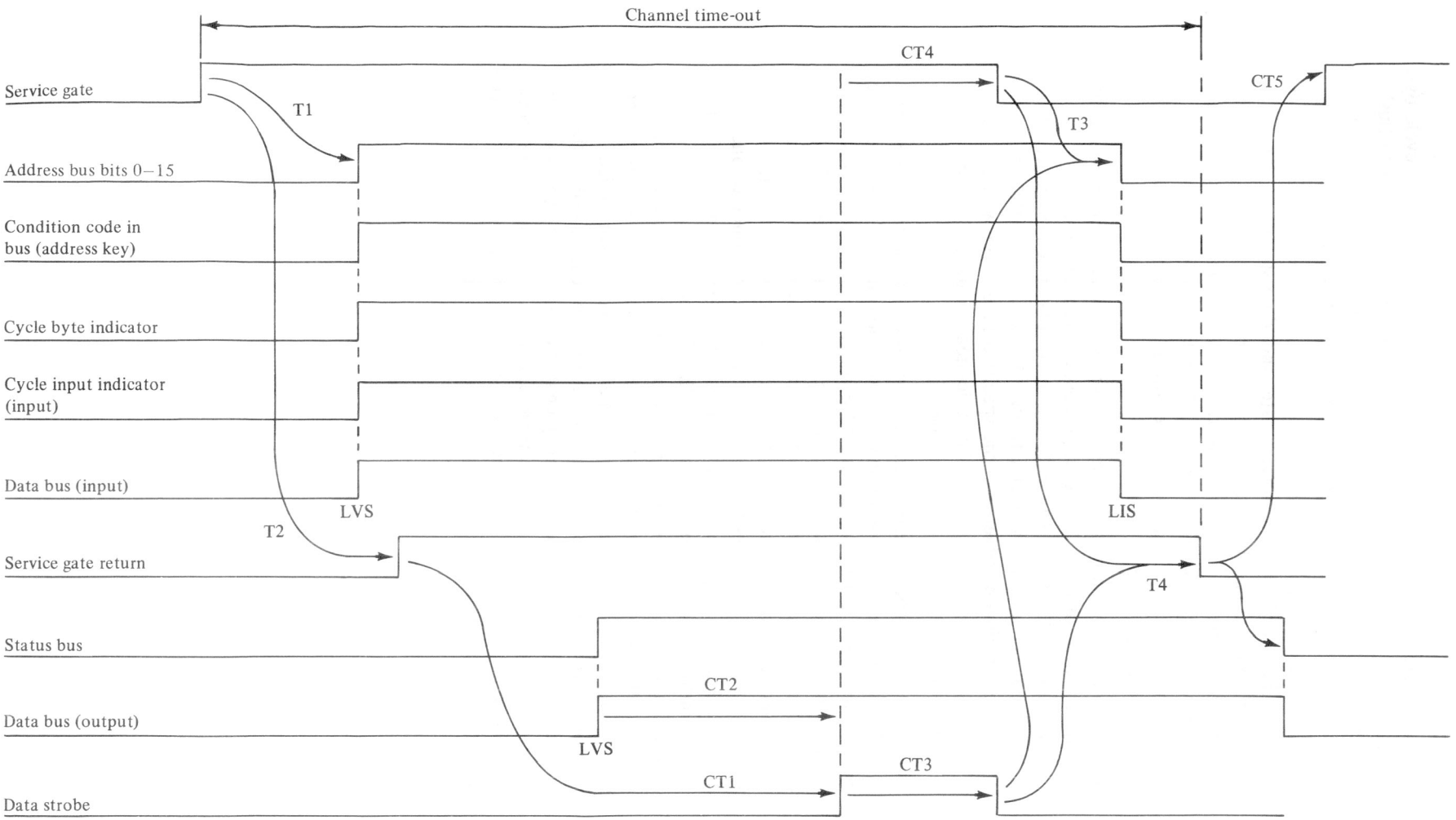
3. 'Status bus' (and 'data bus' on output sequences) is activated by the channel.

4. 'Data strobe' is activated. The duration of 'data strobe,' CT3, is 200 nanoseconds, minimum, as seen at the device interface.

   As denoted by the relationship of, CT1 and CT2 in Figure 2-10, 'status bus' and 'data bus' may be valid only just prior to the activation of 'data strobe' at the device interface; therefore, registration of status and data with the leading edge of 'data strobe' is not recommended unless delays are built into the attachment to allow for trigger conditioning. Because parity must be checked by the device on output sequences, and error status may be posted to the device on 'status bus,' registration of data during 'data strobe' may necessitate double buffering.

   If an error is posted to the device on 'status bus' in a burst-mode transfer (not the last transfer), the device must complete one more service sequence. This additional transfer is a dummy cycle. No device-held parameters are to be updated nor are any additional status bus bits to be accumulated.

5. 'Service gate' and 'data strobe' are deactivated simultaneously at the processor channel output. As denoted by the relationship of CT3 and CT4 in Figure 2-10, 'data strobe' may extend beyond the active envelope of 'service gate' by 100 nanoseconds, maximum, but the overlap of 'data strobe' and 'service gate' is 100 nanoseconds, minimum, as seen at the device interface.



Timings:

$0 \leq T1 \leq T2 \leq 3\ \mu s$
$0 \leq T3 \leq T4 \leq 3\ \mu s$
$100\ ns \leq CT1$
$0 \leq CT2 \leq CT1$
$200\ ns \leq CT3$
$100\ ns \leq CT4 \leq CT3 + 100\ ns$
$0 \leq CT5$ (burst only)

Key:

CT = channel times.
T = attachment-controlled times.
LVS = last valid signal, occurring in time, of a group of signals being activated on the channel. The group is shown linked by short, dotted lines on the timing diagram.
LIS = last invalid signal, occurring in time, of a group of signals being deactivated on the channel. The group is shown linked by short, dotted lines on the timing diagram.

Figure 2-10. Cycle-steal service sequence timing diagram

6. Upon deactivation of both 'service gate' and 'data strobe,' the device deactivates 'address bus bits 0–15,' 'condition code in bus,' 'cycle byte indicator,' and 'cycle input indicator,' as appropriate, and 'data bus' (on an input transfer). These lines must be deactivated prior to the drop of 'service gate return,' as seen at the device interface.

   The device deactivates 'service gate return.' The permissible delay, T4, from the deactivation of 'service gate' and 'data strobe' to the deactivation of 'service gate return,' is 3 microseconds, maximum, as seen at the device interface. This delay is for attachment convenience; however, for performance reasons, the delay should be held to a minimum. All device action for the transfer must be completed prior to dropping 'service gate return.'

7. The total duration of the cycle-steal service sequence is timed out by the channel for error-detection purposes. The total duration is measured in the same way as for an interrupt-service sequence. If the time-out occurs, the channel activates the 'halt or MCHK' line. If the device attachment adheres to the specified times over which it has control, the total duration of the cycle-steal sequence is within the channel time-out under normal operation.

The sequence described here applies to cycle-steal servicing in burst mode, also; however, there is an additional consideration in burst mode, as noted by CT5 in Figure 2-10. 'Service gate' for the next cycle-steal transfer may activate immediately at the device interface after deactivation of 'service gate return.' Therefore, the device does not directly control the demanded rate of servicing in burst mode. (The device does control this demand in normal cycle-steal transfers because one request corresponds to one cycle-steal service sequence.) In burst mode, the device can only exert minor control over the demand made by the channel by indirectly controlling delays of 'service gate return' activation and deactivation; however, this is generally not recommended because there are attendant risks of device underrun and channel time-out. The recommended mechanism for burst mode is to buffer for a size of data equal to the length of the burst. No specific timing characteristics of the channel may be assumed by the device in burst mode operation. The burst mode device must be able to operate with an indefinite delay in the rise of 'service gate' after the deactivation of 'service gate return' (CT5 time).

Poll Sequence Description

Refer to Figures 2-11, 2-12, and 2-13. The poll sequences with 'poll return' or 'burst return' are executed as follows:

1. When the device detects an external interrupting condition, it activates the appropriate bit of the 'request in bus,' as determined by the level field and the I-bit of the Prepare command. The device may activate an interrupt request on the interface only while its I-bit (device mask) is on (equal to a logical 1).

   Once the appropriate bit of the 'request in bus' is activated, that bit must remain active until the device has captured a poll, executed a Prepare command to set the device I-bit off, or received: a Device Reset, 'halt or MCHK,' 'system reset,' or 'power on reset.' If an I/O device has an interrupt request active and executes a Device Reset or Prepare command, the device, as appropriate, drops its request or alters its requested level prior to the deactivation of 'data strobe,' as seen at the device interface.

   When the device requires an access to storage, it activates the 'cycle steal request in' line. Once 'cycle steal request in' has been activated, the line must remain active until the device has captured a poll, or has received a 'halt or MCHK,' 'system reset,' or 'power on reset.' If the device has already activated a cycle-steal request on the interface and detects a device-directed reset, the device must complete the servicing for that cycle-steal request. This servicing is a dummy transfer and is to be an output transfer (read from storage). In the case of burst mode, the dummy transfer must appear as the last transfer of the burst mode. Because the channel is unaware that these are dummy transfers, no device-held parameters are to be updated nor are any status conditions to be recorded or reported by the device.

2. 'Poll ID' is activated by the channel, either as a result of the particular device's request or from other requests previously presented to the channel. 'Poll ID' and a subsequent poll can occur completely asynchronous to the device's request. When the device detects activation of the 'poll ID' bits matching the type of request the device has activated (interrupt level or cycle-steal, regardless of whether or not the device has activated the request on the 'request-in' bus), the device must not allow its state of request to further influence the decision to capture or propagate the 'poll' tag. A time, T1 (measured at the device interface), of 100 nanoseconds after the activation of 'poll ID' and prior to the device request becoming active, on the request in bus is the latest time in which a device may delay the decision to capture or propagate.

3. 'Poll' is activated. The time, CT1, from the activation of the 'poll identifier' to the activation of 'poll,' is 180 nanoseconds, minimum, as measured at the processor channel input. The device interface will see the poll tag delayed from the poll identifier tag by 180 nanoseconds plus the delay at each device propagating the poll. 'Poll' is held valid by the processor channel interface until the activation of 'poll return' or 'burst return' at the processor channel input. When the device detects the leading edge of 'poll,' the device must take action to either capture or propagate the poll.

If the poll is propagated (Figure 2-13):

4. The device activates the 'poll propagate' line to the next device attachment on the channel. The 'poll propagate' output is the image of 'poll,' with a delay, T2, of 100 nanoseconds, maximum. The device must propagate the true DC envelope of the poll without change except for any internal logic delays less than 100 nanoseconds. Once a poll is propagated from the device, the device may take no further action until the activation of the next 'poll.' However, if the device detects a 'halt or MCHK,' 'system reset,' or 'power-on reset,' the 'poll propagate' tag is deactivated at the device output, regardless of the state of the poll at the device input.

If the poll is captured (Figures 2-11 and 2-12):

5. The device activates 'poll return' or 'burst return,' as appropriate, and deactivates the appropriate 'request' line. The 'request' line must be deactivated prior to the activation of 'poll return' or 'burst return.' 'Poll return' or 'burst return' must be activated at a time, T3, of 100 nanoseconds, maximum, from the activation of 'poll,' as seen at the device interface. The processor channel interface will deactivate the poll when it sees the active 'poll return' tag.

6. For interrupt-service sequences, the activation of 'poll return' causes the normal service gate sequence to begin without any intervening DPC sequence. This is necessary to preclude a device reset from occurring between the poll and service sequences and is necessary for proper implementation of device reset. The service gate may occur immediately or may be delayed considerably if another device is finishing a service sequence ($CT3 \geq 0$).

   For cycle-steal operations, service gate may occur immediately or this tag may be delayed considerably if another device is finishing a cycle-steal or DPC sequence.

7. 'Poll' and 'poll ID' are deactivated. The time that 'poll ID' remains at the quiescent value, CT4, is 100 nanoseconds, minimum, as seen at the device interface. However, 'poll ID' cannot be reactivated at the processor channel output prior to the deactivation of 'poll' (or 'burst return') at the processor channel input.

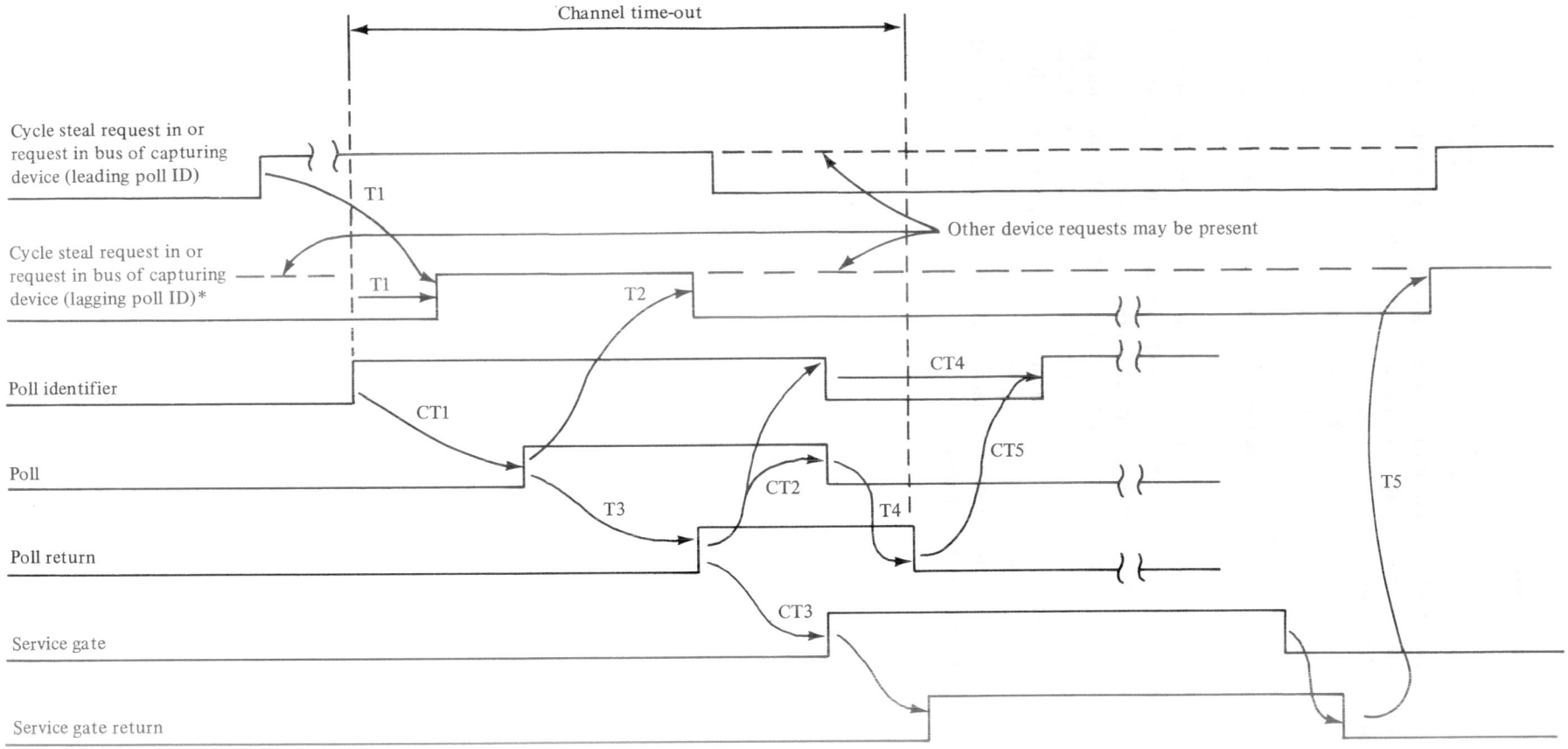
Interrupt or single transfer cycle-steal ('poll return')

8. When 'poll' becomes inactive, 'poll return' must be deactivated within a time, T4, of 100 nanoseconds, as seen at the device interface. The device must not present another 'request in' until 'service gate return' goes inactive, T5.

Burst mode ('burst return') (Figure 2-12):

9. After 'burst return' is activated, the next activation of 'service gate' begins the burst transfer. All other devices on the I/O channel are preempted, and the burst device continues to get service until the burst return is deactivated or an error or time-out condition is detected. 'Burst return' must be deactivated within 100 nanoseconds of the activation of 'service gate' for the last transfer, T4. The I/O device must not present another cycle-steal or interrupt request until 'service gate return' goes inactive for the last transfer, T5. This allows time for the processor to start a new polling sequence and to service a different request, if one is present.

10. In both sequences, (1) with 'poll return' and (2) with 'burst return,' a channel time-out may occur. In the poll sequence with 'poll return,' the time-out occurs if 'poll return' does not go inactive. In the poll sequence with 'burst return,' the time-out occurs if 'poll' does not go inactive. Both of these time-out conditions are indications of a failure at the I/O device, and do not occur under normal operating conditions if the timings in the referenced figures are adhered to. If the channel time-out does occur, it causes a machine check and activates the 'halt or MCHK' line on the channel.



* = cycle steal request in or request in bus of capturing device is lagging poll ID and did not cause poll ID.

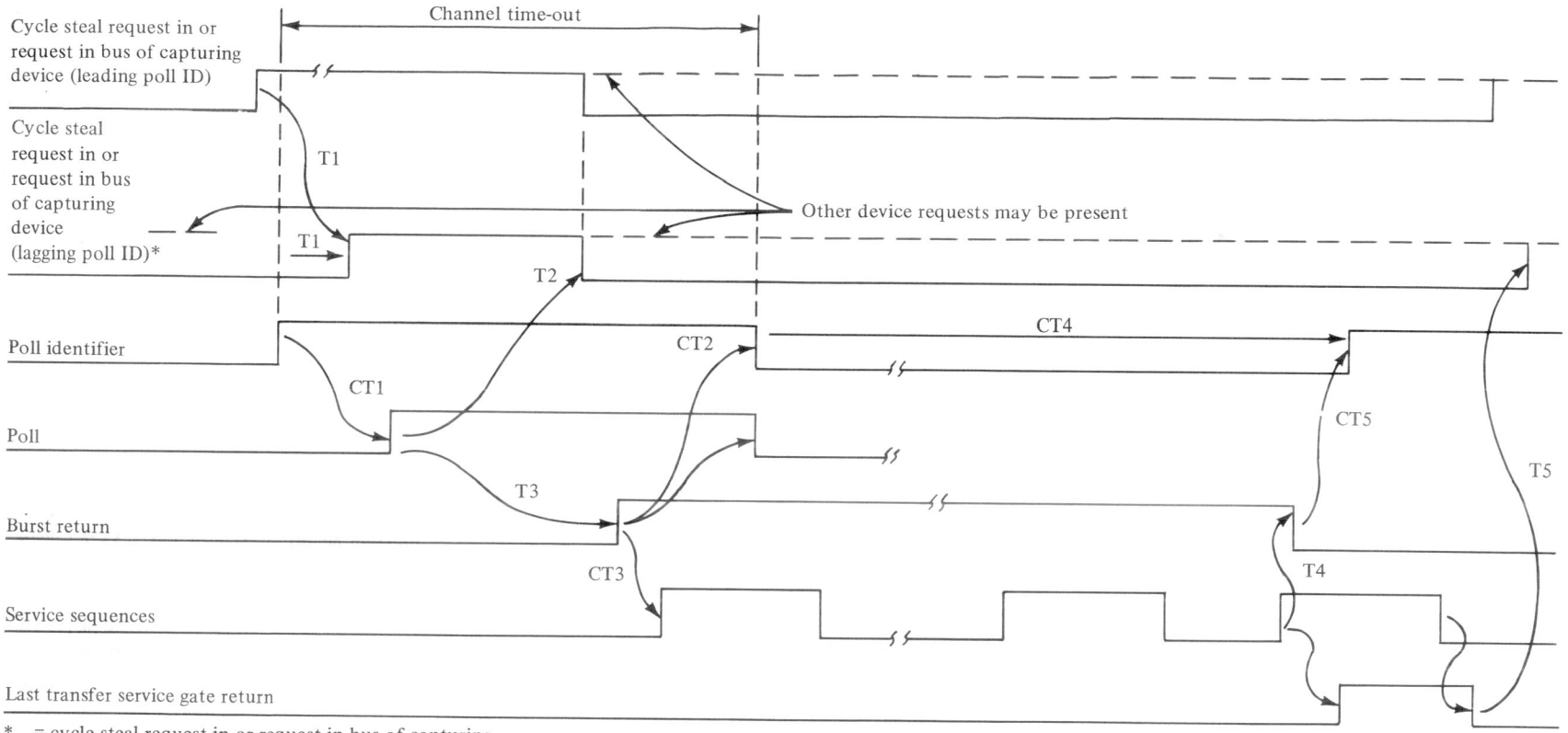
Timings:

T1 ⩽ 100 ns (T1 may be negative)
T2 ⩽ T3 ⩽ 100 ns
T4 ⩽ 100 ns
T5 ⩾ 0
CT1 ⩾ 180 ns
CT2 ⩾ 0
CT3 ⩾ 0
CT4 ⩾ 100 ns + T4
CT5 ⩾ 0

Key:

CT = channel times.
T = attachment-controlled times.

Figure 2-11. Poll sequence with 'poll return' timing diagram



* = cycle steal request in or request in bus of capturing device is lagging poll ID and did not cause poll ID.

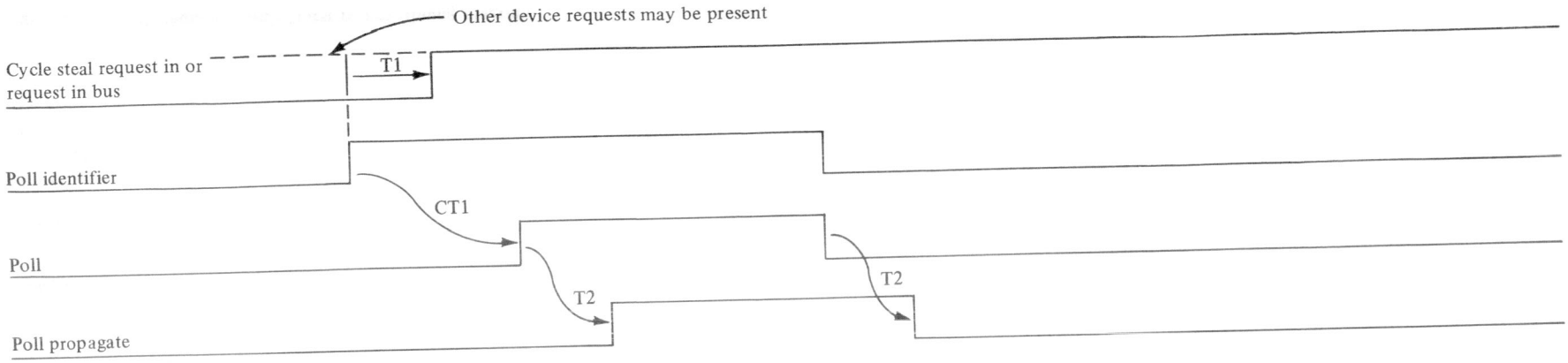
Timings:

T1 ⩽ 100 ns (T1 may be negative)
T2 ⩽ T3 ⩽ 100 ns
T4 ⩾ 100 ns
T5 > 0
CT1 ⩾ 180 ns
CT2 ⩾ 0
CT3 ⩾ 0
CT4 ⩾ 100 ns
CT5 > 0

Key:

CT = channel times.
T = attachment controlled times.

Figure 2-12. Poll sequence with 'burst return' timing diagram



Timings:

T1 $\geq$ 100 ns
T2 $\leqslant$ 100 ns

CT1 $\geq$ 180 ns

Key:

CT = channel times
T = attachment-controlled times

Figure 2-13. 'Poll propagate' timing diagram

Processor-Initiated IPL Sequence Description

Refer to Figure 2-14. The processor-initiated IPL sequence is executed as follows:

1. The 'initiate IPL' line is activated at the processor channel output, along with status bus bit 0 or 1, as a result of the operator pressing the Load key. Status bus bit 0 and 1 reflect the position of the IPL Source switch (Primary or Alternate), at the time the Load key was pressed. The first 'system reset' in this IPL sequence is also activated at this time. 'Initiate IPL' and the 'status bus' are held valid until the activation of the 'IPL' tag at the processor channel input after the first 'system reset' is deactivated. (There may be only one primary and one alternate device on the channel.)

   On the activation of the logical AND of 'initiate IPL' and 'system reset,' the device must dc-reset the 'IPL' tag due to a previous IPL request within 200 nanoseconds, T1, as seen at the device interface. On activation of the first 'system reset,' the device executes all other system reset functions. Because of possible skew, 'system reset' may lag 'initiate IPL' and the 'status bus' at the device interface. Therefore, the 'IPL' tag may temporarily become active at the device interface prior to the first 'system reset.' However, the processor channel ignores the 'IPL' tag during the initial part of the sequence and does not examine the tag line until the first 'system reset' has been activated.

   In no case should the selected IPL device use the leading-edge transition of the first 'system reset.' This is because the first 'system reset' could also lead the 'initiate IPL' and 'status bus' at the device interface.

2. The first 'system reset' is deactivated after a time, CT1, of 4.8 microseconds, minimum, at the device interface. The IPL source device then activates the 'IPL' tag. The attachment must not use the trailing edge transition of the first 'system reset' to activate the 'IPL' tag; rather, the attachment should use a dc-set condition of the 'initiate IPL' tag, the particular status bus bit, and the absence of the first 'system reset' to activate the 'IPL' tag. The time, T2, from the deactivation of the first 'system reset' to the activation of the 'IPL' tag must be greater than 0, as seen at the device interface, but the maximum time is device-dependent. This maximum time should be kept within reasonable limits and, generally, this time should only depend upon electronic, rather than mechanical delays.

3. As a result of 'IPL' going active, 'initiate IPL' is deactivated. The 'status bus' is not valid for the primary/alternate selection portion of the IPL sequence after the time when 'initiate IPL' is deactivated.

4. A second 'system reset' is activated. The time from the deactivation of 'initiate IPL' and activation of the second 'system reset,' CT3, is 200 nanoseconds, minimum, as seen at the device interface. This second 'system reset' is unique. The IPL source device maintains an active 'IPL' tag while using this 'system reset' to enable the cycle-steal transfer for the storage load. The device should use only the trailing edge of the second 'system reset' to accomplish this enabling.

The time from the activation of the 'IPL' tag by the device to the activation of the second 'system reset' by the processor channel, CT4, is less than 500 microseconds. This time may be used by a host processor initiating an IPL sequence as a time-out to detect a defective IPL sequence.

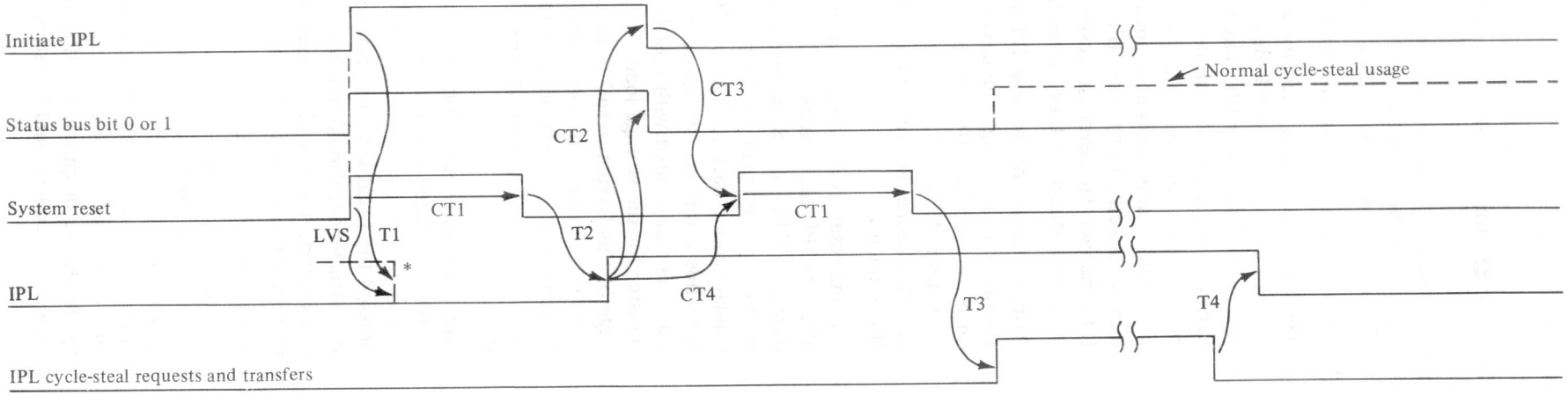
5. The second 'system reset' is deactivated. IPL cycle-steal requests and transfers may then begin. The time, T3, from the deactivation of the second 'system reset' to the activation of the first cycle-steal request, must be greater than 0, as seen at the device interface. The maximum time is device-dependent; however, this time should be kept to a minimum. At this time, the status bus returns to its original function; that is, the reporting of status information to the I/O device being serviced. The IPL record length can be up to a maximum of 64K bytes. Successful completion of IPL is signaled to the processor by the device dropping the 'IPL' tag. Time T4, from the end of cycle-steal requests and transfers (as defined by the deactivation of the last 'service gate return') to the deactivation of the 'IPL' tag, has a minimum time of 0. The maximum time is device-dependent, but should also be kept to a minimum for the same reason as stated for time T3.

   Following the successful completion of IPL and the dropping of the 'IPL' tag, the I/O device must be prepared to level 0 with its I-bit on and presenting an interrupt request to the processor I/O channel. The device must be available in all other respects. When the interrupt is accepted, the device presents the device-end interrupt condition code.

6. If a system reset occurs after the device has enabled cycle-steal requests and transfers, the device must deactivate the 'IPL' tag within 200 nanoseconds at the device interface, terminate the cycle-steal transfers, and execute all other system-reset functions. Note that this system reset could be the result of (1) the operator pressing the Reset key or (2) the operator pressing the Load key to begin another processor-initiated IPL sequence where 'system reset' leads the 'initiate IPL' tag at the device interface. Therefore, this represents an added condition for resetting the 'IPL' tag. Note also that this condition is dependent upon being in an enabled state for IPL transfer as a result of the second 'system reset.'

7. If, during cycle-steal transfers, an error condition is posted to the device on the status bus, the device must terminate further requests and cycle-steal transfers, leave the 'IPL tag' active, and not present an end interrupt. If, during the cycle-steal requests and transfers, a hardware failure causes a channel time-out, the system remains in a "hung" condition; the device should leave the 'IPL' tag active. 'Halt or MCHK' does not occur so that diagnosis of the problem in the state in which the failure or error occurred is allowed.

   Attachment methods for devices with power supplies external to a processor or I/O expansion card file must be capable of executing an IPL if the device is powered up to a ready condition either before or after the processor has activated the 'initiate IPL' tag, 'status bus,' and the first 'system reset' of a processor-initiated IPL sequence.



*IPL tag from previous IPL request

Timings:

T1 $\leq$ 200 ns
T2 $\geq$ 0
T3 $\geq$ 0
T4 $\geq$ 0
CT1 $\geq$ 4.8 μs
CT2 $\geq$ 0
CT3 $\geq$ 200 ns
CT4 $\leq$ 500 μs

Key:

CT = channel times.
T = attachment-controlled times.
LVS = last valid signal, occurring in time, of a group of signals being activated on the channel. The group is shown linked by short, dotted lines on the timing diagram.

Figure 2-14. Processor-initiated IPL sequence timing diagram

Host-Initiated IPL Sequence Description

Refer to Figure 2-15. The figure is divided into two basic sequence timing diagrams: Ⓐ "Initial sequence to normal end" and Ⓑ "Termination and retry sequences," which assumes abnormal termination. The two parts have a common entry point in the activation of the 'IPL' tag by the host IPL device, as shown in the upper part of the figure. The host-initiated IPL sequences (sometimes called remote IPL) are executed as follows:

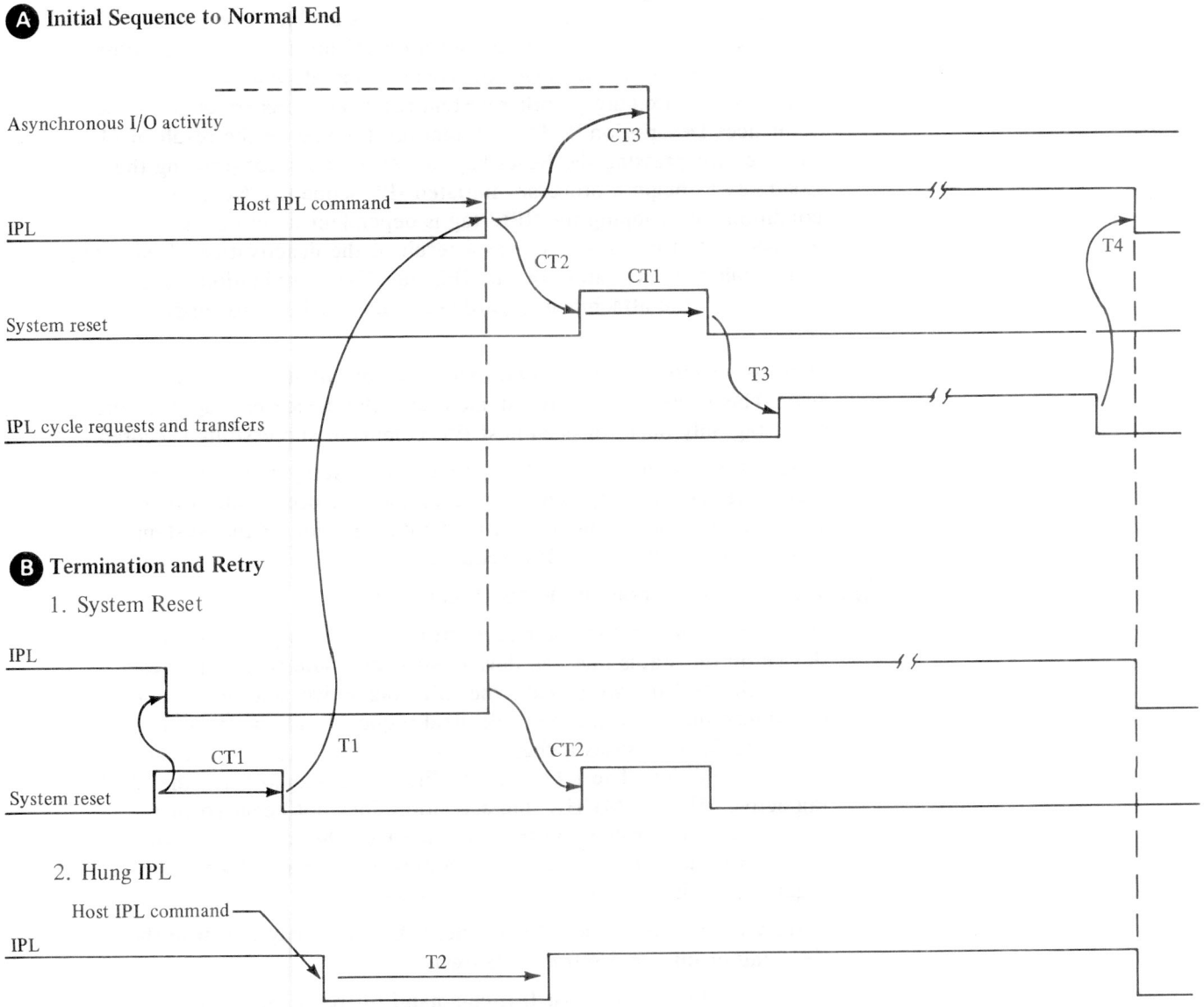
Ⓐ Initial sequence to normal end (Figure 2-15)

1. The host successfully executes a command to the I/O channel device configured as the host IPL device to IPL the system. It is important to remember that a host IPL may be an asynchronous event to the Series/1; therefore, it is to be expected that asyrchronous activity may be in progress on the channel at the time of execution of the host IPL command. These sequences, including normal I/O activity and resets, may be directed to the host IPL attachment or to other devices on the I/O channel. However, successful execution of the host IPL command must be assumed to take precedence over Series/1 sequences.
2. After execution of the host IPL command, the device attachment must activate the 'IPL' tag. The device attachment activates this tag only once for each host IPL command successfully executed. After activation of the 'IPL' tag, the host IPL device attachment must ignore all I/O channel activity not specifically related to execution of the host IPL sequence.
3. 'System reset' is activated at a time, CT2 less than 500 microseconds after the IPL tag is activated. This 'system reset' is activated for a duration, CT1, of 4.8 microseconds, minimum, and is analogous to the second 'system reset' of the processor-initiated IPL sequence; it has a similar unique nature. The host IPL device maintains an active 'IPL' tag while using this 'system reset' to clear its interface signals, to reset status not associated with host IPL, and to enable the cycle-steal transfer for the storage load. The device should use only the trailing edge of this 'system reset' to accomplish this enabling. All other devices on the channel obey this 'system reset' as if it were a normal 'system reset.' Asynchronous I/O activity on the channel is cleared, as seen at the device interface prior to the deactivation of this 'system reset.'

   Note: The only exception to the clearing of this asynchronous I/O activity is related to a processor-initiated IPL sequence. This condition would arise, for example, in a rare situation where the operator pressed the Load key just prior to the host initiating an IPL. The host IPL attachment should not be cognizant of such activity; for purposes of executing the host IPL sequences, the attachment should assume that all asynchronous I/O activity is cleared.
4. After this 'system reset' is deactivated, IPL cycle-steal requests and transfers may begin. The time, T3, from the deactivation of the 'system reset' to the activation of the first cycle-steal request must be greater than 0, as seen at the device interface; the maximum time is device-dependent. The IPL record length can be up to a maximum of 64K bytes. Successful completion of IPL is signaled to the processor by the device dropping the 'IPL' tag. The time, T4, from the end of cycle-steal requests and transfers (as defined by the deactivation of the

last 'service gate return') to the deactivation of the 'IPL tag' has a minimum time of 0; the maximum time is device-dependent.

Following the successful completion of IPL and the dropping of the 'IPL' tag, the host IPL device must be prepared to level 0 with its I-bit on and present an interrupt request to the processor I/O channel. The device must be available in all other respects. When the interrupt is accepted, the device presents the device-end interrupt condition code.



Timings:

T1 ⩾ 3 μs
3 μs ⩽ T2 ⩽ 7 μs
T3 ⩾ 0
T4 ⩾ 0
CT1 ⩾ 4.8 μs
0 ⩽ CT2 ⩽ 500 μs
CT3 ⩽ 1.8 μs

Legend:

CT = channel times.
T = attachment controlled times

Figure 2-15. Host-initiated IPL sequence timing diagram

Ⓑ Termination and retry sequences (Figure 2-15)

Host IPL retry on Series/1 is not only allowed, but is encouraged to be supported by a host IPL device. Retry sequences are dependent upon the type of abnormal termination. The discussion of asynchronous I/O activity in item 1 of Ⓐ applies equally as well in the following sequence descriptions.

1 System reset termination and retry (Figure 2-15).

1. If a 'system reset' occurs after the device has enabled cycle-steal requests and transfers, the device must deactivate the 'IPL' tag within 200 nanoseconds at the device interface, terminate the cycle-steal transfers, and execute all other system reset functions (refer to "Reset Sequences Description"). This 'system reset' could be the result of (1) the operator pressing the Reset key or (2) the operator pressing the Load key to begin a processor-initiated IPL sequence. Note that this condition for dropping the 'IPL' tag is dependent upon being in an enabled state for IPL transfer as a result of the deactivation of 'system reset' following activation of the 'IPL' tag. This termination must be executed by the attachment regardless of its capability to support retry.
2. If retry is supported, the I/O device may not initiate a retry on its own. This is essentially a restatement that the device may activate the 'IPL' tag only once for each host IPL command successfully executed.
3. After execution of the host IPL command for retry, the device must reactivate the 'IPL' tag. The activation may not occur until a time, T1, of 3 microseconds, minimum, after the deactivation of the 'system reset' that terminated the IPL sequence.

2 Hung IPL Termination and Retry (Figure 2-15).

1. If, during cycle-steal transfers, an error condition is posted to the device on the status bus, the device must terminate further requests and cycle-steal transfers, leave the 'IPL' tag active, and not present an end interrupt. If, during the cycle-steal requests and transfers, a hardware failure causes a channel time-out, the system remains in a "hung" condition. The I/O channel IPL device should leave the 'IPL' tag active. 'Halt or MCHK' tag activation does not occur so that diagnosis of the problem in the state in which the failure or error occurred is allowed. This termination must be executed by the device regardless of its capability to support retry.
2. If retry is supported, the I/O channel IPL device may not drop the 'IPL' tag or initiate a retry on its own.
3. After execution of the host IPL command for retry, the device deactivates, and then reactivates the 'IPL' tag. The reactivation must occur within a time, T2, of from 3 microseconds, minimum, to 7 microseconds, maximum, after deactivation of the 'IPL' tag, as seen at the device interface.

Reset Sequences Description

1. The effect that 'halt or MCHK,' 'system reset,' or 'power-on reset' must have has been discussed throughout this chapter.
2. The 'halt or MCHK' and 'system reset' tags, when occurring, are active for 4.8 microseconds, minimum, as seen at the device interface. Power-on reset sequencing is discussed in "Processor I/O Channel Electrical Characteristics" in this chapter.
3. The deactivation of the device interface signals that are active at the time of the reset must be performed within 200 nanoseconds, as seen at the device interface. The prepare field and I-bit must be reset under the envelope of a 'system reset.'
4. The processors may have unpredictable values on the address, data, and status buses during resets. Therefore, resetting of registers must not depend on the values of these buses.
5. For specific information concerning a reset sequence in conjunction with another sequence, refer to the description of the basic sequences in "Operational Sequences On the Channel" in this chapter.

Design Considerations for Operational Sequences

This section highlights some aspects of device-adapter design that require further explanation. In some cases, typical circuits are used as a vehicle to explain the aspect under discussion. The area of logic represented should *not* be taken in the context of a total design, when other considerations would result in added function to a logic area. These logic diagrams are intended *only* to aid in explanation of channel interface function. *Timing relationships may not be inferred from the logic diagrams; all timing must be as shown in the timing diagrams.* For example, the figures assume one device only, although an attachment may service more than one device. The logic figures (Figures 2-16 through 2-19) use the following conventions:

- Connections—those with a circled "I" indicate a unit load or drive to the device interface with the channel; Those with a circled "J" indicate a jumper connection. Circled dots indicate that the signal is connected to another figure in this subsection. Dots alone indicate that the signal is used or originates elsewhere in an attachment, but is not connected to another figure.
- Logic—wedges indicate negative active signals. Logic blocks are labeled with a particular logic function; the blocks perform that particular logic function with the polarity of the inputs as shown for the block. Except for the invert function, logic functions are considered to produce a positive output internal to a block. In some cases, a logic function is combined with a signal inversion to indicate the complete function of the block.
- Labels—signal lines are labeled with the polarity appropriate to the active level of the signal.

"Operational Sequences on the Channel" in this chapter specified that for DPC, interrupt-service, and cycle-steal service sequences, the deactivation of a return tag ('address gate return' or 'service gate return') occurred only after the deactivation of the respective outgoing tag ('address gate' or 'service gate') and 'data strobe.'

Because the channel deactivates the outgoing tag simultaneously with the deactivation of 'data strobe,' the phase relationships between the outgoing tag and 'data strobe' could be skewed at the device interface. At the device interface, 'data strobe' can be deactivated either before or after the deactivation of the outgoing tag. However, 'data strobe' would never be active completely outside the active envelope of the outgoing tag for that operational sequence. This suggests that a method for keeping the return tag active to meet the condition specified in the first paragraph is to logically OR the outbound tag with 'data strobe.' This is true, provided that certain considerations are taken into account. First, as seen by any device, 'data strobe' or 'address gate' can occur randomly outside of a DPC sequence, when 'address bus bit 16' (DPC sequence) is not active. This is because of the presence of main storage physically attached to the channel for the 4952 and 4953 processors. Second, as seen by the poll mechanism of any device, 'data strobe' can occur randomly. This is because of the asynchronous nature of polling and service sequences on the channel. A device may operate its poll mechanism while it or other devices are executing a sequence associated with the service group. These two considerations make it necessary to (1) ensure that the logical OR is gated only for those sequences specifically of interest to the device when it is selected, and (2) keep the poll mechanism operation independent of 'data strobe.'

Figure 2-16 illustrates a method for keeping the return tags active for DPC, interrupt, and cycle-steal sequences. For a DPC sequence, DPC selection is the condition of system ready, 'address bus bit 16' active, and a true device address compare Ⓐ. The logical OR of 'address gate' and 'data strobe,' Ⓓ gated with DPC selection Ⓑ Ⓒ will give the maximum '+address gate' envelope, correcting for any outgoing tag skew. For interrupt and cycle-steal service sequences, device selection is based on the first active 'service gate' following a poll capture.

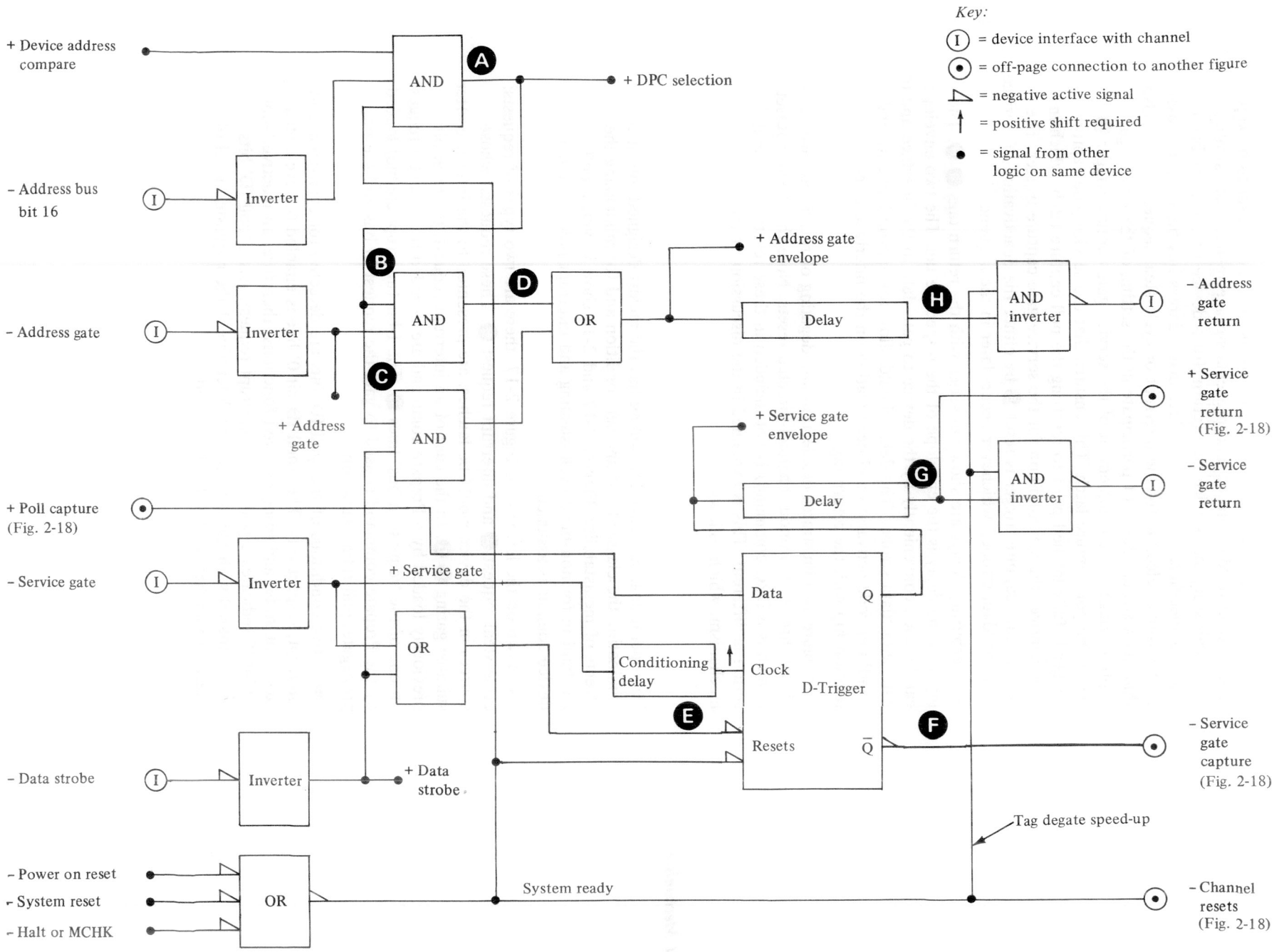


Figure 2-16. Tags and data strobe logic

The circuit shown in Figure 2-16 enables the poll mechanism to be kept independent of 'data strobe' and prevents storage-related 'data strobes' from activating the 'service gate return' for a device unless it has been selected specifically for service. Note that 'address bus bit 16' is not used to determine selection for the interrupt or cycle-steal sequence. Note also that 'data strobe' does not participate in the setting of the service gate capture trigger. The complement of the service gate capture trigger (F) resets the poll capture latch. This ensures that the service gate capture trigger is fully latched prior to resetting the poll capture latch, which in turn removes the set condition for the service gate capture trigger. The service gate capture trigger is reset (E) by either the deactivation of 'service gate' or 'data strobe,' whichever occurs later in the sequence.

Two arbitrary delays are shown in series with the return tags (G) (H). The input to the delay is the envelope of the respective tag. The two envelopes can be used conveniently by the device to gate data to the interface and to gate with 'data strobe.' The delay should allow for appropriate data and condition code activation and deactivation on the interface in correct relationship with the return tag.

The figure also illustrates deselection and degating of return tags with any of the three synchronous channel-directed resets. Note that Device Reset (which is a DPC command) is not included in these resets, because its action is different. This is explained in the discussion of the poll mechanism, which follows.

Poll Mechanism

The operational sequence for polling has the means designed into it for eliminating the classical test and set condition and for minimizing the effects of metastability. Figures 2-17 and 2-18 show a typical poll mechanism for non-burst cycle-stealing and interrupt polling. A single device adapter is assumed.

As shown on the left side of Figure 2-17, there are two types of requests: cycle-steal request (A) and interrupt request (B). These requests, whose sources in the device would be latches, are presented to the interface after suitable gating (C) (D). In the case of an interrupt request, the level bits previously loaded by a Prepare command are decoded to present a request on one of the 'request in bus' lines (C). The I-bit (interrupt enable) loaded by the Prepare command is used to gate the request-in bus and the poll propagate/poll return function.

The active conditions of the 'poll ID' bits are detected for cycle-steal and interrupt, respectively. The '-poll ID bit 0' line is enabled for cycle-steal, quiescent state, and some reserved functions; therefore, an inactive '-poll ID bit 0' indicates a poll for an interrupt request. Also, 'poll ID' bits 1–4 are compared with the level bits to determine if the requested level of interrupt matches the level being polled.

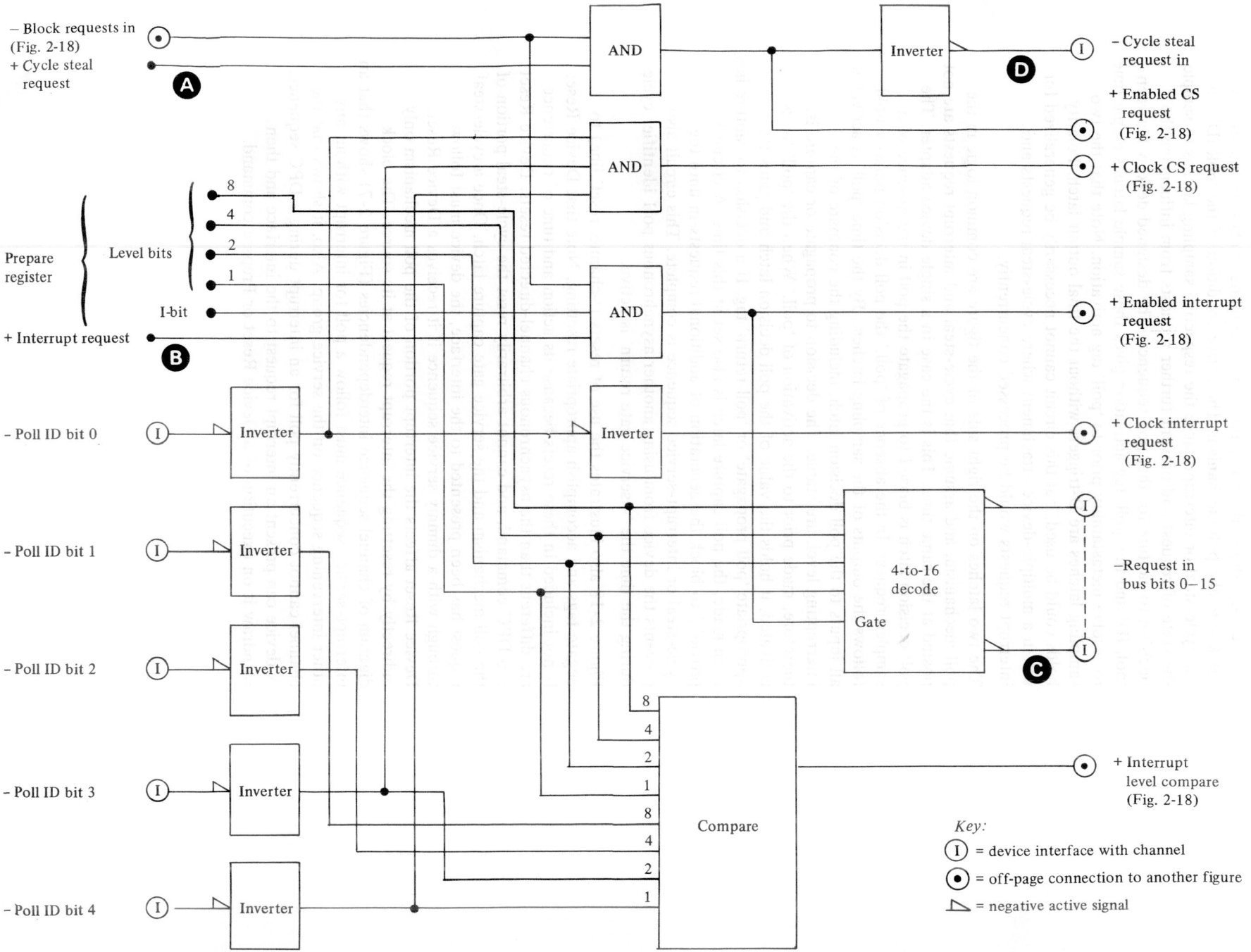
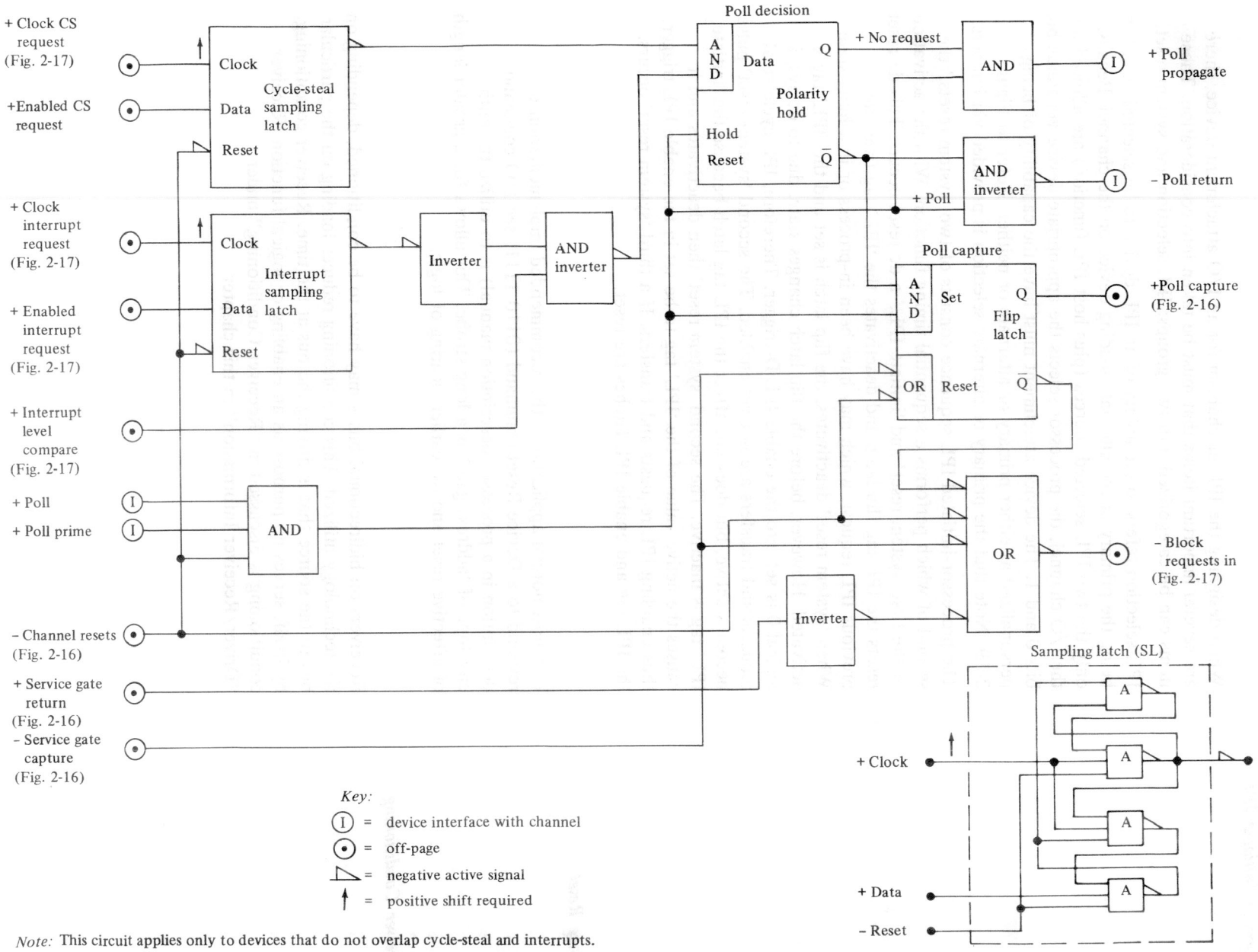


Figure 2-17. Poll mechanism—request and poll ID logic

Figure 2-18 shows the poll latches. The sampling latches on the left are the key to the poll mechanism. The active condition of the 'poll ID' bits for cycle-steal or interrupt cause the respective sampling latches to sample the state of request and prevent further requests from influencing the decision to capture for that poll sequence. The designed deskew between 'poll ID' and the 'poll' tag activation gives these sample latches ample time to resolve metastability prior to 'poll' tag activation. Note that the two sampling latches are D-triggers without the final output latch. Polarity holds could be used, but this circuit cannot necessarily be generalized for use in a multiple-device attachment where cycle-steal requests and interrupt requests would be processed concurrently.

The two latches on the right side of the figure are common logic in the poll mechanism, and assume that cycle-steal and interrupt requests are not posted at the same time. This is the case in a single device adapter. The poll decision latch is biased to propagate the poll in the absence of a sampled request. In the absence of 'poll,' the poll decision polarity hold follows the outputs of the sampling latches.. By the time 'poll' is activated, all inputs to the poll decision latch, including the compare of the interrupting level, are stable. The decision to propagate or capture is, therefore, made prior to the activation of 'poll.' When the 'poll' tag is activated, it holds the value of the poll decision latch and gates the appropriate 'poll propagate' or 'poll return' tag. If a decision to capture has been made, the poll capture latch is also set at this time. A circuit is provided to block the generation of additional requests-in until the cycle-steal or interrupt-service sequence is complete. This circuit also prevents the device from using another asynchronous pol1 identifier cycle during the time the '+service gate return' is active.

Figure 2-18 also illustrates the use of resets ('-channel reset' line) to degate tags and accomplish appropriate resetting. Note that Device Reset is not included in these resets because its action and time of occurrence are different than the asynchronous channel-directed resets. Device Reset is a DPC command, and cannot arbitrarily reset the cycle-steal portion of the poll mechanism and the service gate capture latch. Once a cycle-steal request has been presented to the interface, the device must follow through with a dummy service sequence if it receives a Device Reset. Device Reset affects the interrupt portion of the poll mechanism only indirectly by resetting the interrupt request at its source. The block diagram of channel sequence interdependencies (Figure 2-7) shows that an interrupt-service sequence must follow a poll for interrupt without any other intervening sequence on the service group. Also, it shows that the channel cannot concurrently poll for an interrupt during a DPC sequence. A device can present an interrupt request to the interface and then withdraw it on execution of a Device Reset or Prepare command.



Note: This circuit applies only to devices that do not overlap cycle-steal and interrupts.

Figure 2-18. Poll mechanism—latches

Processor-Initiated IPL

When designing the IPL mechanism for an I/O attachment device, there are several important items that must be taken into consideration. These items can be categorized into two groups: IPL selection and system reset.

IPL selection refers to the ability of an IPL device to be selected as either being the primary or the alternate loading device on the channel. Because only the two IPL selected sources (plus host IPL function) are allowed on the I/O channel, the processor selects the appropriate device via status bus bits 0 and 1. The device attachment must have the capability of being personalized as either primary or alternate or neither. Refer to Figure 2-19. Note that the primary or alternate selection is provided via jumpers.

The processor-initiated IPL sequence consists of two 'system resets,' the second of which performs a sequential timing function. With the activation of the first 'system reset' and 'initiate IPL,' a dc reset occurs. This dc reset resets the IPL tag flip latch and deactivates the 'IPL' tag from any previous IPL request, which may have been in-process or in a hung state. When 'system reset' deactivates, the flip latch is set and the 'IPL' tag is activated. However, before the flip latch changes state, due to delays, a logical 0 is set into the enable IPL D-trigger. Therefore, IPL cycle-steal requests and transfers are not yet enabled. The second 'system reset' pulse becomes active, but does not affect the IPL tag latch because the 'initiate IPL' tag is inactive. The second 'system reset' then deactivates and it causes the active value of the 'IPL' tag to be set in the enable IPL trigger, thus enabling IPL requests and transfers. If a third 'system reset' occurs, the IPL tag and enable IPL latches are reset.

Device Reset

For most normal applications, the recommended implementation to respond to a Device Reset command (0110 1111; see I/O command description in a processor description manual) is to utilize the entire envelope of 'address gate' as a long strobe. This allows for a greater length of effective reset and for earlier clearing of logic.

Receiver Conditioning

Receivers on bidirectional buses may have to be conditioned, depending on the technology utilized. This conditioning reduces loading on the particular bus to the source that is driving the bus at the time. Receiver conditioning, by itself, serves no purpose as an enabling or logical function. Receiver conditioning is discussed in "Receiver Conditioning" under "Driver/Receiver Information" in this chapter.

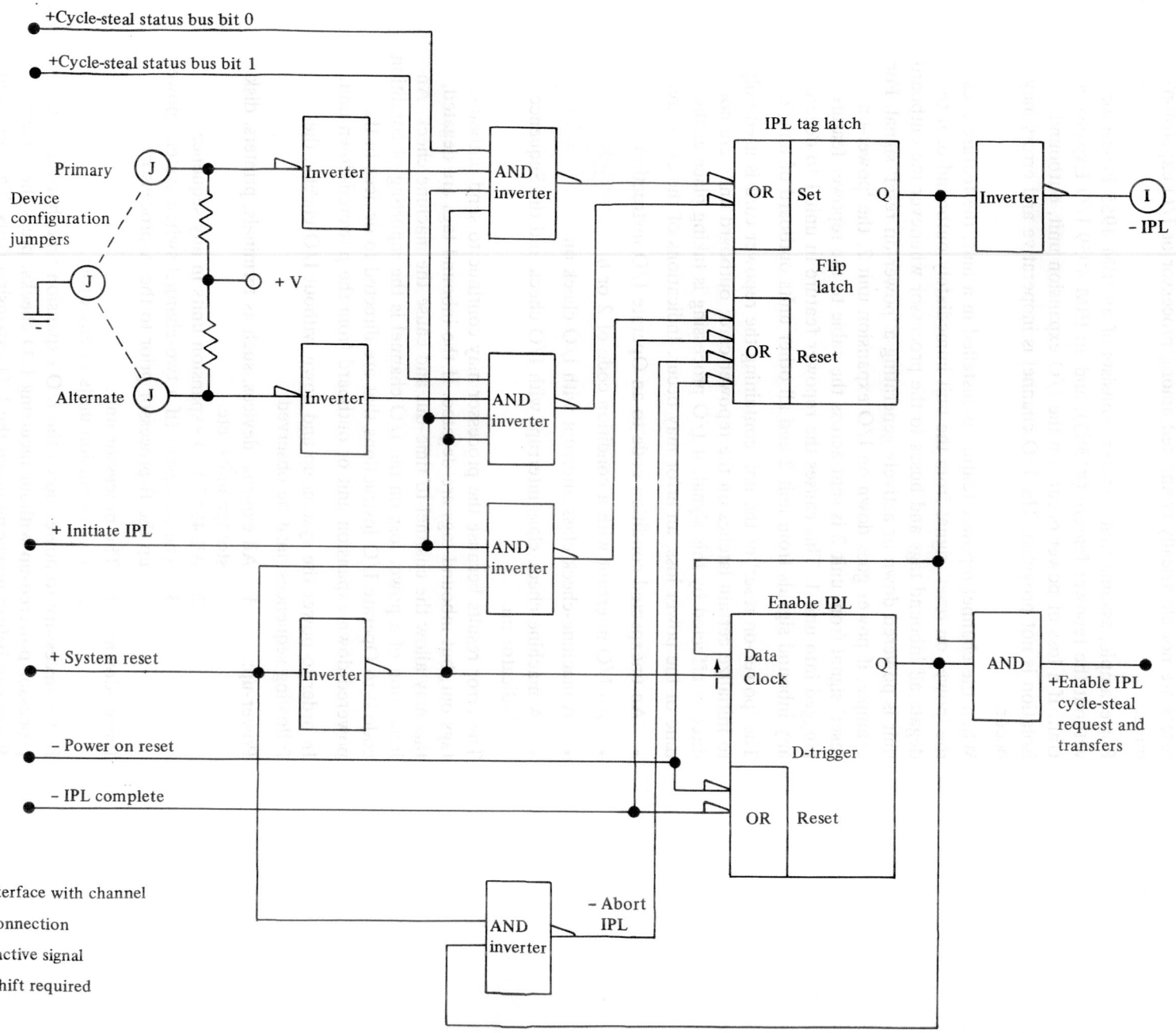


Figure 2-19. Processor-initiated IPL logic

Refer to Figure 2-20. Each processor unit and I/O expansion unit on the I/O channel has a self-contained power-on reset. These unit power-on resets are not electrically connected among processor or I/O expansion units.

For example, assume that a system consists of an IBM 4955 Processor, without the repower feature (#1565), and an IBM 4959 I/O Expansion Unit. If a loss of power occurs on the I/O expansion unit, outbound isolation is not provided. The I/O channel is inoperative and errors may occur.

When the channel repower feature is installed in a unit, the feature uses the 'power on reset' signal from the unit immediately outbound of it to degate all inbound tags and buses to the processor whenever the outboard unit is powered down or actively generating a 'power-on reset' signal. For example, if power goes down on I/O expansion unit 2, the 'power-on reset' signal from unit 2 is sent across the cable to the repower feature plugged into unit 1. This causes the repower feature in unit 1 to degate any inbound signals from unit 2 and all other units outboard of unit 2.

The 'power-on reset' of the unit containing the repower card is used only to initialize certain latches on the repower card; outboard units are not directly affected by this signal. If I/O processing is taking place at the time of the power loss, an error may occur. Indications of the error are:

- An unexpected condition code to an Operate I/O instruction
- An I/O interrupt with a condition code of 2 or 6
- A machine-check class interrupt with I/O check on
- A machine-check class interrupt with I/O check and the Sequence indicator on.

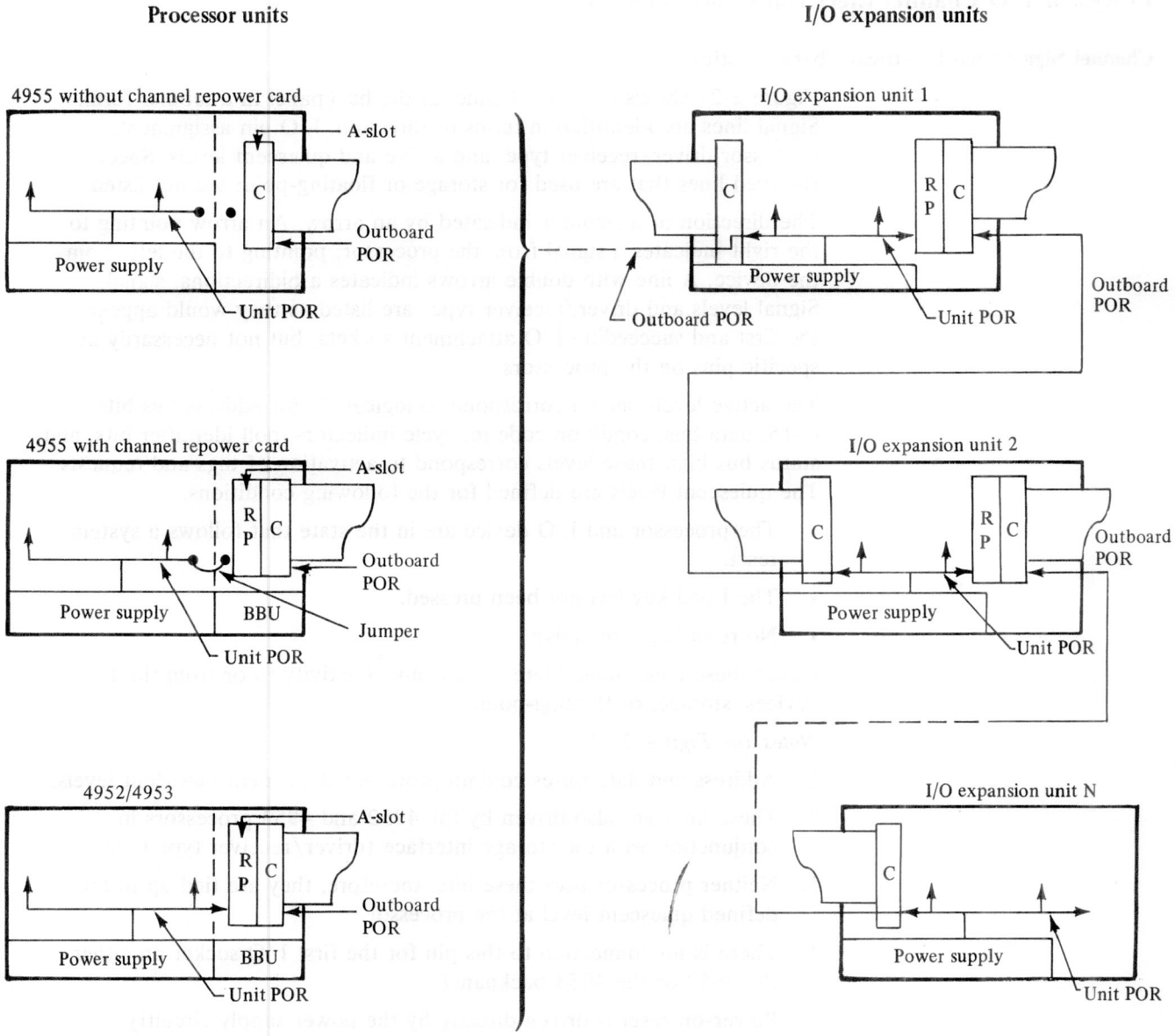
The error results because the processor may continue to send outbound tags out, but inbound tags are degated. If the inbound tags are degated, this may allow the channel to time-out and cause the machine check. An indication of a power loss on the I/O channel is the reporting of condition code 0 to Operate I/O instructions that are directed to devices in the powered-down expansion unit or outboard from the powered-down unit.

In order to power the system up and down without I/O checks, the following sequences must be observed:

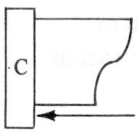
Power-up:
1. All external devices, such as terminals, printers, disk storage units, etc.
2. All 4959 I/O expansion units in any sequence.
3. The processor (if a two-channel switch system, power up the B-processor prior to the A-processor).

Power-down:
1. The processor unit.
2. I/O expansion units in any order.

If it is necessary to power-down the I/O expansion unit, but leave the processor powered-up without incurring I/O checks, press the system Reset key before powering down the I/O expansion units. This procedure is valid only if the channel repower feature is installed in the processor.

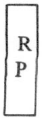


Key.



I/O cable and connector showing power-on reset (POR)

Outboard POR (through cable to channel repower card)



Channel repower card

POR = power-on reset

BBU = IBM 4999 Battery Backup Unit (optional)

Figure 2-20. Power-on resets as they affect the I/O channel

Processor I/O Channel Electrical Characteristics

Channel Signal Line Electrical Characteristics

Figure 2-21 shows the I/O channel at the backpanel in a tabular form. Signal lines are identified in terms of direction, I/O pin assignment, processor driver/receiver type, and active and quiescent levels. Special reserved lines that are used for storage or floating-point are not listed.

The direction of a signal is indicated by an arrow. An arrow pointing to the right indicates a signal from the processor; pointing to the left, from the device. A line with double arrows indicates a bidirectional signal. Signal levels and driver/receiver types are listed as they would appear at the first and succeeding I/O attachment sockets, but not necessarily at specific pins on the processors.

The active levels shown correspond to logical 1's for address bus bits 0–15, data bus, condition code in, cycle indicators, poll identifier bits, and status bus bits; these levels correspond to activation of tags and requests. The quiescent levels are defined for the following conditions:

- The processor and I/O device are in the state that follows a system reset.
- The Load key has not been pressed.
- No reset tags are active.

Under these conditions, there is no channel activity to or from the I/O devices, storage, or floating-point.

Notes for Figure 2-21:

1. Address and data buses contain processor-dependent quiescent levels.
2. These lines are also driven by the 4952 and 4953 processors in conjunction with the storage interface (driver/receiver type C-C).
3. Neither processor uses these bits; therefore, they are tied up to the defined quiescent level at the processor.
4. There is no connection to this pin for the first I/O socket on either the 4952 or the 4953 backpanel.
5. Power-on reset is driven directly by the power supply circuitry.
6. Neither the 4952 nor the 4953 backpanel connects to any of these pins.
7. Neither the 4952 nor the 4953 processor uses status bus bit 2 (for storage protect); therefore, this line is tied up to the defined quiescent level.

Line name	Direction	I/O pin assignment	Processor driver receiver type	Active level	4952/4953 quiescent level	4955 quiescent level
Address bus bit 0	⟷	B02	C-A	Minus	Note 1	Plus
Address bus bit 1	⟷	B03	C-B	Minus	Note 1	Plus
Address bus bit 2	⟷	B04	C-B	Minus	Note 1	Plus
Address bus bit 3	⟷	B05	C-B	Minus	Note 1	Plus
Address bus bit 4	⟷	B07	C-B	Minus	Note 1	Plus
Address bus bit 5	⟷	B08	C-B	Minus	Note 1	Plus
Address bus bit 6	⟷	B09	C-B	Minus	Note 1	Plus
Address bus bit 7	⟷	B10	C-B	Minus	Note 1	Plus
Address bus bit 8	⟷	B12	C-B	Minus	Note 1	Plus
Address bus bit 9	⟷	D02	C-B	Minus	Note 1	Plus
Address bus bit 10	⟷	D04	C-B	Minus	Note 1	Plus
Address bus bit 11	⟷	D05	C-B	Minus	Note 1	Plus
Address bus bit 12	⟷	D06	C-B	Minus	Note 1	Plus
Address bus bit 13	⟷	D07	C-B	Minus	Note 1	Plus
Address bus bit 14	⟷	D09	C-B	Minus	Note 1	Plus
Address bus bit 15	⟷	D10	C-B	Minus	Note 1	Plus
Address bus bit 16	→	D11	C-D	Minus	Plus	Plus
Address gate	→	M08	C-D	Minus	Plus	Plus
Address gate return	←	M09	C-E	Minus	Plus	Plus
Burst return	←	P04	C-E	Minus	Plus	Plus
Condition code in bit 0	←	D12	C-E	Minus	Plus	Plus
Condition code in bit 1	←	D13	C-E	Minus	Plus	Plus
Condition code in bit 2	←	B13	C-E	Minus	Plus	Plus
Cycle byte indicator (Note 2)	←	P10	C-E (Note 2)	Minus	Plus	Plus
Cycle input indicator (Note 2)	←	P09	C-E (Note 2)	Minus	Plus	Plus
Cycle steal request in	←	M02	C-E	Minus	Plus	Plus
Data bus bit 0	⟷	G02	C-C	Minus	Note 1	Plus
Data bus bit 1	⟷	G03	C-C	Minus	Note 1	Plus
Data bus bit 2	⟷	G04	C-C	Minus	Note 1	Plus
Data bus bit 3	⟷	G05	C-C	Minus	Note 1	Plus
Data bus bit 4	⟷	G07	C-C	Minus	Note 1	Plus
Data bus bit 5	⟷	G08	C-C	Minus	Note 1	Plus
Data bus bit 6	⟷	G09	C-C	Minus	Note 1	Plus
Data bus bit 7	⟷	G10	C-C	Minus	Note 1	Plus
Data bus bit P0	⟷	G12	C-C	Minus	Note 1	Minus
Data bus bit 8	⟷	J02	C-C	Minus	Note 1	Plus
Data bus bit 9	⟷	J04	C-C	Minus	Note 1	Plus
Data bus bit 10	⟷	J05	C-C	Minus	Note 1	Plus
Data bus bit 11	⟷	J06	C-C	Minus	Note 1	Plus
Data bus bit 12	⟷	J07	C-C	Minus	Note 1	Plus
Data bus bit 13	⟷	J09	C-C	Minus	Note 1	Plus
Data bus bit 14	⟷	J10	C-C	Minus	Note 1	Plus
Data bus bit 15	⟷	J11	C-C	Minus	Note 1	Plus
Data bus bit P1	⟷	J12	C-C	Minus	Note 1	Minus

Figure 2-21 (Part 1 of 2). Channel drivers/receivers types and levels

Line name	Direction	I/O pin assignment	Processor driver receiver type	Active level	4952/4953 quiescent level	4955 quiescent level
Data strobe	→	M10	C-D	Minus	Plus	Plus
Halt or MCHK	→	M07	C-D	Minus	Plus	Plus
Initiate IPL	→	P07	C-D	Minus	Plus	Plus
IPL	←	S04	C-E	Minus	Plus	Plus
Poll	→	M12	C-D	Plus	Minus	Minus
Poll identifier bit 0	→	P11	C-D	Minus	Minus	Minus
Poll identifier bit 1	→	S02	Unused	Minus	Plus (Note 3)	Plus (Note 3)
Poll identifier bit 2	→	S03	Unused	Minus	Plus (Note 3)	Plus (Note 3)
Poll identifier bit 3	→	P12	C-D	Minus	Plus	Plus
Poll identifier bit 4	→	P13	C-D	Minus	Plus	Plus
Poll prime	→	M13	C-D (Note 4)	Plus	Minus	Minus
Poll propagate	→	M11		Plus	Minus	Minus
Poll return	←	M04	C-E	Minus	Plus	Plus
Power on reset	→	S05	Note 5	Minus	Plus	*Plus*
Request in bus bit 0	←	S07	C-E	Minus	Plus	Plus
Request in bus bit 1	←	S08	C-E	Minus	Plus	Plus
Request in bus bit 2	←	S09	C-E	Minus	Plus	Plus
Request in bus bit 3	←	S10	C-E	Minus	Plus	Plus
Request in bus bit 4	←	S12	Unused	Minus	Note 6	Plus
Request in bus bit 5	←	S13	Unused	Minus	Note 6	Plus
Request in bus bit 6	←	U02	Unused	Minus	Note 6	Plus
Request in bus bit 7	←	U04	Unused	Minus	Note 6	Plus
Request in bus bit 8	←	U05	Unused	Minus	Note 6	Plus
Request in bus bit 9	←	U06	Unused	Minus	Note 6	Plus
Request in bus bit 10	←	U07	Unused	Minus	Note 6	Plus
Request in bus bit 11	←	U09	Unused	Minus	Note 6	Plus
Request in bus bit 12	←	U10	Unused	Minus	Note 6	Plus
Request in bus bit 13	←	U11	Unused	Minus	Note 6	Plus
Request in bus bit 14	←	U12	Unused	Minus	Note 6	Plus
Request in bus bit 15	←	U13	Unused	Minus	Note 6	Plus
Service gate	→	P05	C-D	Minus	Plus	Plus
Service gate return	←	P06	C-E	Minus	Plus	Plus
Status bus bit 0	→	J13	C-D	Minus	Plus	Plus
Status bus bit 1	→	G13	C-D	Minus	Plus	Plus
Status bus bit 2	→	M03	C-D	Minus	Plus (Note 7)	Plus
Status bus bit 3	→	P02	C-D	Minus	Plus	Plus
System reset	→	M05	C-D	Minus	Plus	Plus

Figure 2-21 (Part 2 of 2). Channel drivers/receivers types and levels

Driver/Receiver Information

Figures 2-22 and 2-23 contain further information about the drivers and receivers for the Series/1 processors.

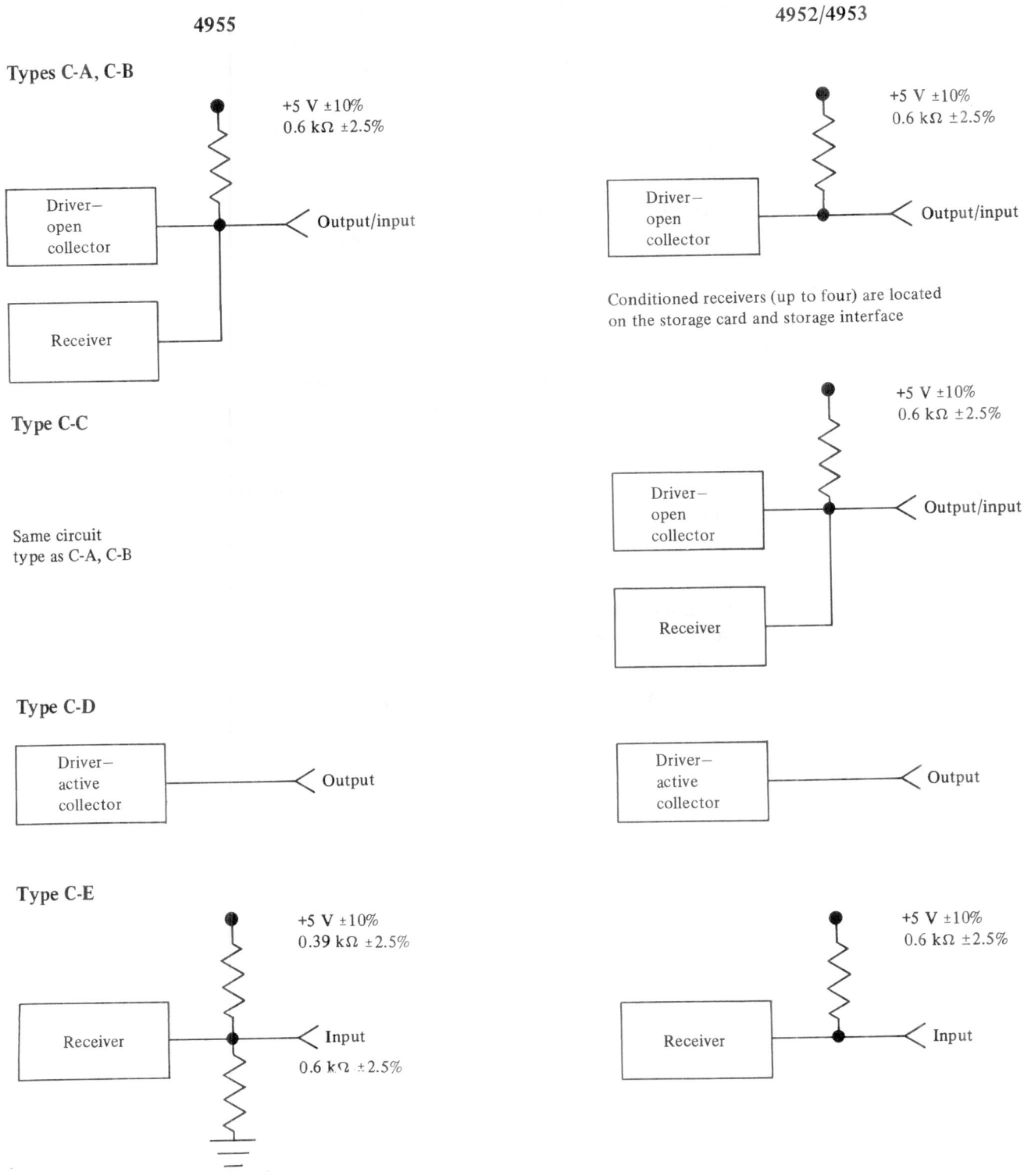


Figure 2-22. I/O channel driver/receiver classification

Types C-A, C-B	4952/4953		4955	
	Driver	Receiver	Driver	Receiver
MPUL	5.5 V	5.5 V	5.5 V	5.5 V
LPUL	2.4 V	2.0 V	2.4 V	2.0 V
MPDL	0.6 V	0.8 V	0.4 V	0.8 V
LPDL	0.0 V	0.0 V	0.0 V	0.0 V

Type C-C	4952/4953		4955	
	Driver	Receiver	Driver	Receiver
MPUL	5.5 V	5.5 V	5.5 V	5.5 V
LPUL	2.4 V	2.0 V	2.4 V	2.0 V
MPDL	0.6 V	0.8 V	0.45 V	0.8 V
LPDL	0.0 V	0.0 V	0.0 V	0.0 V

Type C-D	4952/4953	4955
	Driver	Driver
MPUL	5.5 V	5.5 V
LPUL	2.4 V	2.4 V
MPDL	0.6 V	0.6 V
LPDL	0.0 V	0.0 V

Type C-E	4952/4953	4955
	Receiver	Receiver
MPUL	5.5 V	5.5 V
LPUL	2.0 V	2.0 V
MPDL	0.8 V	0.8 V
LPDL	0.0 V	0.0 V

Key:

MPUL = most-positive up level
LPUL = least-positive up level
MPDL = most-positive down level
LPDL = least-positive down level

Figure 2-23. Channel driver/receiver information

Unit-Load Characteristics

This section describes the specifications for a unit load on the channel.

A device adapter or attachment represents a single drop on the I/O channel. It can represent one or more logical devices, each with a device address. For a device adapter to attach to the I/O channel and not restrict the I/O configuration because of improper loading, it must present a unit load to the I/O channel. A unit load means that every specification on each of the drivers and receivers to each I/O channel line has been met or exceeded. A violation of any of the driver/receiver specifications constitutes a violation of the unit-load requirement. Proper operation of the channel under these circumstances would then be dependent on the particular configuration of attachments on the channel and, consequently, would be generally unpredictable.

Figure 2-24 shows the classifications of driver/receiver types to I/O channel signal lines. Figure 2-25 illustrates each driver/receiver type in general terms and establishes the reference current direction for the elements of each type. Figure 2-26 shows the drivers and receivers for each type. Two types of unit loads are specified: a general unit load and a TTL unit load. IBM attachments present general unit loads to the interface.

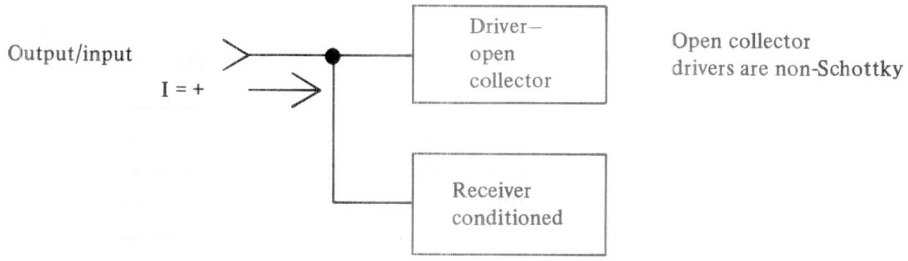
Line name	Direction	I/O Pin assignment	I/O driver/receiver type
Address bus bit 0	⟷	B02	A-A
Address bus bit 1	⟷	B03	A-B
Address bus bit 2	⟷	B04	A-B
Address bus bit 3	⟷	B05	A-B
Address bus bit 4	⟷	B07	A-B
Address bus bit 5	⟷	B08	A-B
Address bus bit 6	⟷	B09	A-B
Address bus bit 7	⟷	B10	A-B
Address bus bit 8	⟷	B12	A-B
Address bus bit 9	⟷	D02	A-B
Address bus bit 10	⟷	D04	A-B
Address bus bit 11	⟷	D05	A-B
Address bus bit 12	⟷	D06	A-B
Address bus bit 13	⟷	D07	A-B
Address bus bit 14	⟷	D09	A-B
Address bus bit 15	⟷	D10	A-B
Address bus bit 16	→	D11	A-D
Address gate	→	M08	A-D
Address gate return	←	M09	A-E
Burst return	←	P04	A-E
Condition code in bit 0	←	D12	A-E
Condition code in bit 1	←	D13	A-E
Condition code in bit 2	←	B13	A-E
Cycle byte indicator	←	P10	A-E
Cycle input indicator	←	P09	A-E
Cycle steal request in	←	M02	A-E
Data bus bit 0	⟷	G02	A-C
Data bus bit 1	⟷	G03	A-C
Data bus bit 2	⟷	G04	A-C
Data bus bit 3	⟷	G05	A-C
Data bus bit 4	⟷	G07	A-C
Data bus bit 5	⟷	G08	A-C
Data bus bit 6	⟷	G09	A-C
Data bus bit 7	⟷	G10	A-C
Data bus bit P0	⟷	G12	A-C
Data bus bit 8	⟷	J02	A-C
Data bus bit 9	⟷	J04	A-C
Data bus bit 10	⟷	J05	A-C
Data bus bit 11	⟷	J06	A-C
Data bus bit 12	⟷	J07	A-C
Data bus bit 13	⟷	J09	A-C
Data bus bit 14	⟷	J10	A-C
Data bus bit 15	⟷	J11	A-C
Data bus bit P1	⟷	J12	A-C

Figure 2-24 (Part 1 of 2). Unit-load driver/receiver types

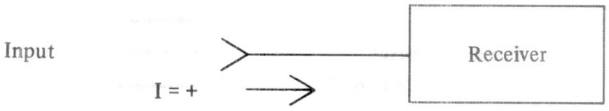
Line name	Direction	I/O Pin assignment	I/O driver/receiver type
Data strobe	→	M10	A-D
Halt or MCHK	→	M07	A-D
Initiate IPL	→	P07	A-D
IPL	←	S04	A-E
Poll	→	M12	A-G
Poll identifier bit 0	→	P11	A-D
Poll identifier bit 1	→	S02	A-D
Poll identifier bit 2	→	S03	A-D
Poll identifier bit 3	→	P12	A-D
Poll identifier bit 4	→	P13	A-D
Poll prime	→	M13	A-G
Poll propagate	→	M11	A-F
Poll return	←	M04	A-E
Power on reset	→	S05	A-D
Request in bus bit 0	←	S07	A-E
Request in bus bit 1	←	S08	A-E
Request in bus bit 2	←	S09	A-E
Request in bus bit 3	←	S10	A-E
Request in bus bit 4	←	S12	A-E
Request in bus bit 5	←	S13	A-E
Request in bus bit 6	←	U02	A-E
Request in bus bit 7	←	U04	A-E
Request in bus bit 8	←	U05	A-E
Request in bus bit 9	←	U06	A-E
Request in bus bit 10	←	U07	A-E
Request in bus bit 11	←	U09	A-E
Request in bus bit 12	←	U10	A-E
Request in bus bit 13	←	U11	A-E
Request in bus bit 14	←	U12	A-E
Request in bus bit 15	←	U13	A-E
Service gate	→	P05	A-D
Service gate return	←	P06	A-E
Status bus bit 0	→	J13	A-D
Status bus bit 1	→	G13	A-D
Status bus bit 2	→	M03	A-D
Status bus bit 3	→	P02	A-D
System reset	→	M05	A-D

Figure 2-24 (Part 2 of 2). Unit-load driver/receiver types

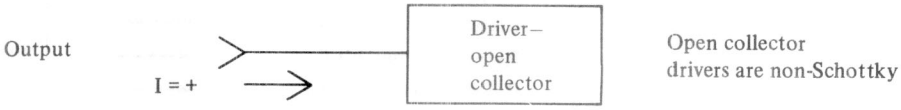
Types A-A, A-B, A-C



Type A-D



Type A-E



Type A-F

Type A-G

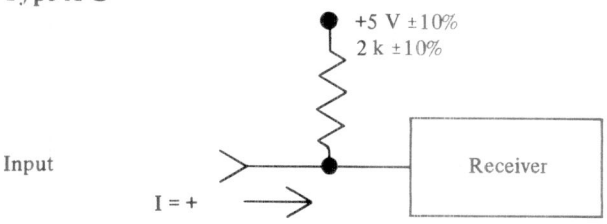


Figure 2-25. Unit-load driver/receiver classification

Type and element	Parameter	Test condition (volts) at node	General unit load-current (mA) min	max	TTL unit load-current (mA) min	max
A-A driver	High-level output	2.4		+0.110		+0.250
	Low-level output	0.45 (Note 1)	+20		+20	
A-A receiver	High-level input	2.4		+0.04		+0.04
(conditioned)	Low-level input-conditioned inactive	0.2 (Note 2)		−0.1		−0.2
	Low-level input-conditioned active	0.4 (Note 3) 0		−0.75 −0.93		−1.6
A-B, A-C driver	High-level output	2.4		+0.110		+0.250
	Low-level output	0.45 (Note 1)	+16		+16	
A-B, A-C receiver (conditioned)	High-level input	2.4		+0.04		+0.04
	Low-level input-conditioned inactive	0.2 (Note 2)		−0.2		−0.4
	Low-level input-conditioned active	0.4 (Note 3) 0		−0.75 −0.93		−1.6

Figure 2-26 (Part 1 of 2). Unit-load driver/receiver specifications

Type and element	Parameter	Test condition (volts) at node	General unit load-current (mA) min	max	TTL unit load-current (mA) min	max
A-D receiver	High-level input	2.4		+0.03		+0.04
	Low-level input	0.4 (Note 3) 0		−0.75 −0.93		−1.6
A-E driver	High-level output	2.4		+0.150		+0.250
	Low-level output	0.45 (Note 1)	+16		+16	
A-F driver	High-level output	2.4		−0.4		−0.4
	Low-level output	0.6 (Note 1)	+16		+16	
A-G receiver	High-level input	2.4		+0.04		+0.04
(without resistor)	Low-level input	0.4		−1.6		−1.6

Notes: The information in this section describes the specifications for a unit load on the channel. The specifications apply to an operating range of 0°C to 70°C. Each unit driver and receiver must be no more than one physical element. For example, two half-unit load receivers should not be used in lieu of a one-unit load receiver. Test conditions assume that the supply voltage (V_{CC}) is at maximum or minimum value to produce worst-case conditions. The operating limits of V_{CC} are ±10 percent.

1. Test conditions of less than the listed voltage, with the specified sink capability, also satisfies the specification.
2. The unit-load current versus test-condition voltage is highly nonlinear. Types A-A, A-B, and A-C receivers need not be conditioned if the receiver always satisfies the conditioned inactive unit-load current for a test condition of from 0.0 to 0.45 volt. See "Receiver Conditioning" in this section for further explanation of conditioning.
3. The general unit-load current may be computed at any other test-condition voltage by linear extrapolation, using the two points given.

Figure 2-26 (Part 2 of 2). Unit-load driver/receiver specifications

Voltage Levels and Switching Characteristics

The driver voltage levels given are the minimum and maximum output levels for the driver circuits, as seen at the logic circuit output pins.

The receiver switching levels given are as seen at the logic circuit pins and include dc-noise tolerance.

Driver voltage levels

Levels	*Non-Schottky*	*Schottky*
MPUL	5.50 V	5.5 V
LPUL	2.40 V	2.4 V
MPDL	0.45 V	0.6 V
LPDL	0.0 V	0.0 V

Receiver switching characteristics

Levels	*Input*
MPUL	5.5 V
LPUL	2.0 V
MPDL	0.8 V
LPDL	0.0 V

Key:

MPUL = most-positive up level
LPUL = least=positive up level
MPDL = most-positive down level
LPDL = least-positive down level

Capacitive Loading

Any single data or tag line that represents one drop on the I/O channel must not be loaded with more than 30 picofarads (pf). Where a TTL load has been substituted for a general-unit load, the line capacitance may not exceed 60 pf. Each circuit line through the socket adapter must be estimated at 10 pf for application purposes.

Receiver Conditioning

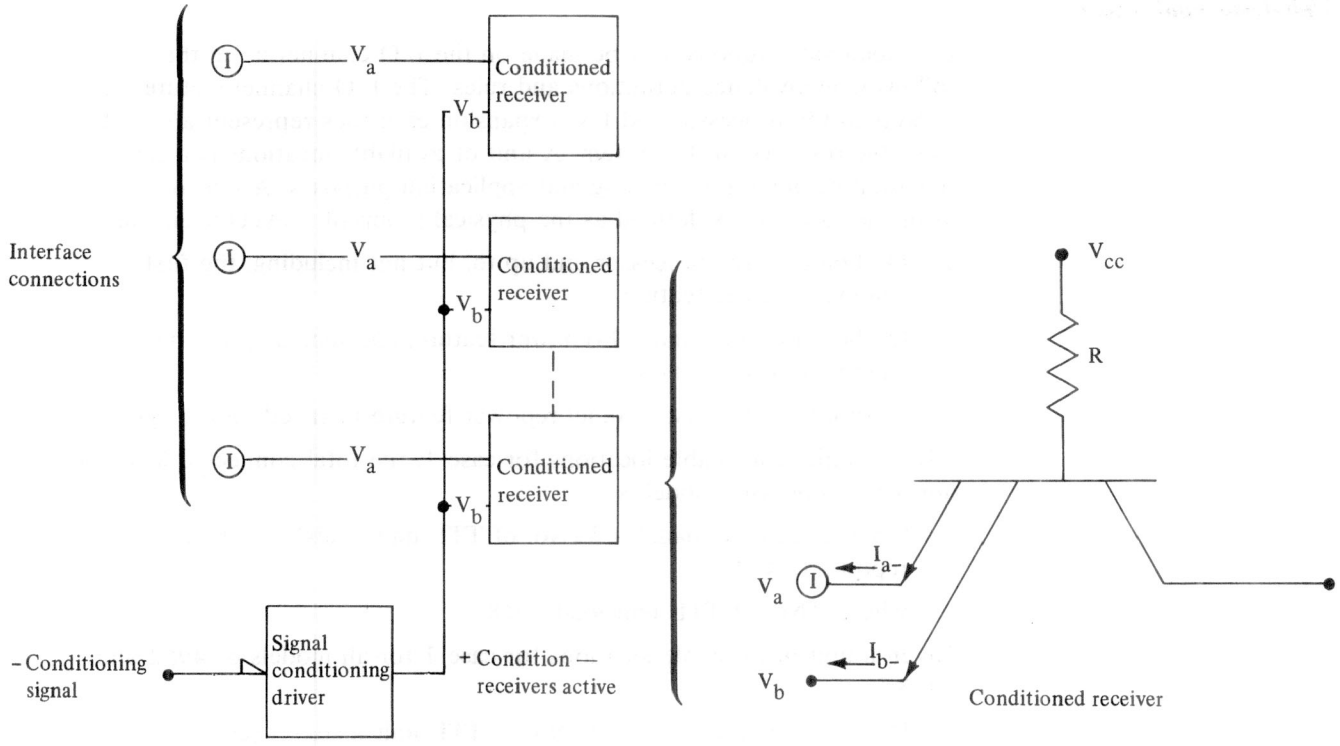
The number of receivers that can be connected to a bidirectional line is limited by the total current that the receivers supply to the line, relative to the amount of current that a driver on the line can sink and still maintain a down state within specification. These limitations impose a major restriction to the number of receivers that can be operated by a single driver. Receiver conditioning relieves these limitations for conventional technology by providing a means of gating off a receiver when it is not the intended recipient of the logic signal on the bus. This allows a larger number of receivers to be connected to the bus. Signals must be provided to condition the receivers independent of the bus. Conditioning, in itself, is not an enabling or logical function; however, conditioning signals are generated from logical conditions in the attachment.

Receiver conditioning is shown in Figure 2-27. When a receiver is not intended to be responsive to the logic signal on the bus (V_a), the control gate (conditioning driver) holds the second input point of the receiver (V_b) to the lower voltage or down state. Because the bus driver contains a larger load than the conditioning driver, the conditioning driver is able to sink more current than the bus driver, thus making $V_a > V_b$. In this state, current I_b is greater than I_a and the receiver does not present a current load as large as it normally would to the bus. Therefore, the receiver is said to be conditioned off or inactive. It is important to choose a signal conditioning driver with a low down-level voltage in the region of 0.15 volt or less. Selecting a high-current capability driver and designing for a low fan-out helps to maintain this low down level.

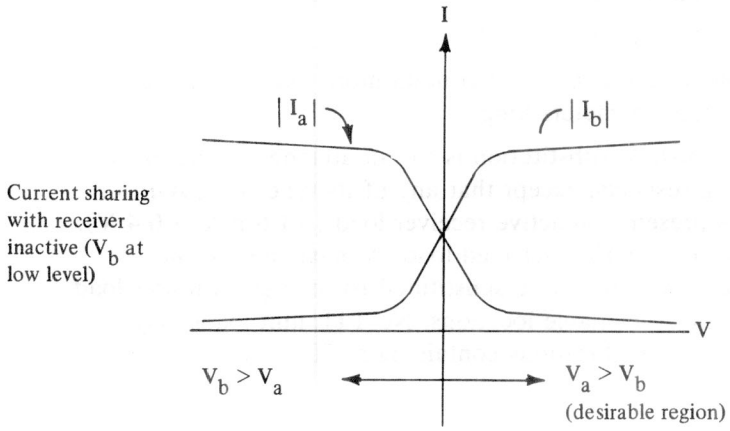
If the receiver is intended to respond to the logic state on the bus, the control signal to the conditioning driver releases the appropriate potential at V_b to allow the receiver to be gated into a state that is responsive to the logical signal at V_a. The receiver is now said to be conditioned on or active.

The address bus bits 8–15 receivers are conditioned active only with 'address bus bit 16' being active. Address bus bits 0–7 are conditioned active only during a DPC selection, which is, in effect, 'address bus bit 16' being active and a device address comparison. The data bus is conditioned during: (1) a DPC selection with address bus bit-1 equal to a logical 1 and only until the deactivation of address gate return, and (2) a service gate capture for a cycle-steal service sequence for an output transfer and only until the deactivation of 'service gate return.'

Note: The receivers must be conditioned active only during the preceding events; they are to be conditioned off or inactive at all other times.



(a)



(b)

Figure 2-27. Receiver conditioning

Unit-Load Equivalences

Unit-load substitutions may be made on the I/O channel using the following equivalence definitions and rules. The I/O channel feature sockets in the processor and I/O expansion card files represent an available resource in the system. A unit of available locations is a subset of this total resource for planning and application purposes. A unit of available locations is defined as the physical group of sockets available:

1. Outboard of the processor and up to, but not including, the first channel repower feature.
2. Outboard of any channel repower feature, and including the next channel repower feature.
3. Outboard of the last channel repower feature installed on the system.

Given a unit of available locations for case 1, the total connected load for any 4955 processor model is:

[(No. of general loads) +2 (No. of TTL unit loads) + (channel repower)] ≤ 21

where: (No. of TTL unit loads) ≤ 8.

Given a unit of available locations for case 1 for all models of 4952 and 4953:

[(No. of general loads) +2 (No. of TTL unit loads) +(channel repower)] ≤ 14

where: (No. of TTL unit loads) ≤ 6

All versions of the 4952 and 4953 processors require a channel repower card to exit the card file.

For cases 2 and 3:

[(No. of general loads) +2 (No. of TTL unit loads)] ≤ 14

where: (No. of TTL unit loads) ≤ 7

Any unit of available locations may not contain more than one cable, which must be less than 1.8 meters long.

A special case of a unit-load substitution is for an attachment that presents a TTL unit load in all respects, except that any of its type A-A, A-B, or A-C receiver always presents an active receiver load (−1.6 mA at 0.4 V). This type of load is called a TTL-selected load. A maximum of one TTL-selected load attachment can be substituted for one general unit-load attachment in any unit of available locations. No TTL unit loads may coexist in a unit of available locations containing a TTL-selected load.

Other Attachment Considerations

Location of Physical and Logical Elements

Each device attachment or other circuitry occupying a card socket in a Series/1 card file must be able to redrive or propagate a poll as part of the serial polling mechanism. This polling mechanism must be contained on that part of the device attachment card(s) that plugs into the I/O socket. This is to ensure that: (1) cabling delays are not encountered (for example, cabling out to the poll mechanism at the device may cause incorrect timing sequences to occur depending on cable length and driving/receiving capability), and (2) powering down a device must not affect the ability to propagate a poll.

All I/O channel drivers, receivers, and logic necessary to condition receivers should be on that part of the device attachment card(s) that plugs into the I/O socket. This includes at least device address comparison logic, some DPC command logic (for detecting a write sequence), and service gate capture logic.

IPL logic, to the extent that the attachment should have the ability to hold the state of the 'enable IPL cycle steal request and transfers' pending device response, should be located on that portion of the attachment that plugs into and derives power from the I/O socket. Otherwise, this may preclude the capability of the device to execute a processor-initiated IPL in auto-IPL mode.

For attachments to devices that are capable of executing processor-initiated IPLs, at least that portion of the IPL logic that will detect and hold the indication that the attached device is to IPL, should reside on that part of the attachment that plugs into and takes power from the I/O socket. (See also "Processor-Initiated IPL Sequence Description" and "Host-Initiated IPL Sequence Description.")

Some attachments will service devices and device logic that take power from a source separate from the power source providing power to the I/O socket into which the attachment is plugged. Such attachments must be capable of preventing an I/O check due to a channel time-out if a power loss occurs on the device or device logic that is separately powered from the attachment.

Printed Circuit Wire Lengths

Printed circuit wire lengths between I/O channel drivers/receivers and the connector tabs on the interfacing card should be held to *75 mm (3 in), maximum*. Tag inputs and outputs, and 'request in' lines should use shorter lengths.

Signal Clamping

All I/O channel circuit modules should have clamping for negative excursions of the signal input.

Circuit Module Voltage Tolerances

Circuit modules used in device attachments that utilize voltages from IBM supplies must be capable of operating with ±10 percent tolerances from nominal, as seen at the module pins.

Circuit Module Overvoltage

All circuit modules must have an overvoltage rating for voltage supplied of 40 percent over nominal.

Power Supply Electrical Characteristics

The power supplies for the processor and I/O expansion units provide five regulated dc output voltages: +5.0, +8.5, +12.0, −5.0, and −12.0 volts. Both supplies contain overvoltage, undervoltage, and overcurrent protection. Should overvoltage or undervoltage occur, the condition initiates a power supply shutdown sequence. (See *IBM Series/1 Configurator*, GA34-0042, for use of the Communications Power feature, #2010.)

Sequencing Requirements

The 'power on reset' signal is provided to ensure the state of the logic during power on and off. The signal is TTL-compatible. A logical 1 (up) level is between +2.6 V and +5.5 V; a logical 0 (down) level is between 0.0 V and +0.4 V. The 'power on reset' signal starts at the TTL down level. When the +5 V, −5 V, and +8.5 V are within operational limits, this signal goes to the TTL up level after a 500-millisecond delay. Should any of the three voltages go approximately 3 percent below their minimum tolerances, this signal goes to the TTL down level.

Logic Voltage Sequencing

If a user incorporates a technology such that voltage sequencing must occur within a given period of time (>350 ms), the following method can be used: Assume that, for substrate biasing purposes, V_n=−5.0 V and V_h=+8.5 V; if V_n is more positive than −3.5 V, V_h must not remain above +5.0 V for more than 500 ms. Although no true sequencing occurs, after approximately 350 ms the power supply circuitry checks to see that the voltages are at an operational level. If they are not, the supply shuts down; otherwise, the sequencing is met and the technology is protected.

Processor I/O Channel Physical Characteristics

This section describes I/O pin and cable assignments for all standard channel signals, voltages, and identifies special reserved lines. It also provides basic data for the basic physical components of the channel.

Signal Pin and Cable Assignments

Figure 2-28 defines the signal lines and shows their corresponding cable and I/O pin assignments. Figure 2-29 defines the voltage/ground/special pin assignments and compares a typical I/O slot position to the A-slot position. The corresponding I/O cable pin assignments are also given in this figure. When connecting to an I/O expansion unit, four standard I/O channel cables must be used to obtain all signal lines. These cables leave the 4955 processor via the A-socket position on the board or via a repower card contained on the board, depending on the configuration. The 4952 and 4953 processors can only be cabled out via a repower feature. In an I/O expansion unit, the A-socket is restricted for use as the entry point for the I/O channel cables.

Each cable carries twenty signal lines, which are arranged so that cable #1 plugs into the top of the A-socket and cable #4 plugs into the bottom of the A-socket.

Line name	Direction	I/O pin assignment	I/O channel cable assignment #1	#2	#3	#4
Address bus bit 0	⟷	B02	B02			
Address bus bit 1	⟷	B03	B03			
Address bus bit 2	⟷	B04	B04			
Address bus bit 3	⟷	B05	B05			
Address bus bit 4	⟷	B07	B07			
Address bus bit 5	⟷	B08	B08			
Address bus bit 6	⟷	B09	B09			
Address bus bit 7	⟷	B10	B10			
Address bus bit 8	⟷	B12	B12			
Address bus bit 9	⟷	D02	D02			
Address bus bit 10	⟷	D04	D04			
Address bus bit 11	⟷	D05	D05			
Address bus bit 12	⟷	D06	D06			
Address bus bit 13	⟷	D07	D07			
Address bus bit 14	⟷	D09	D09			
Address bus bit 15	⟷	D10	D10			
Address bus bit 16	→	D11	D11			
Address gate	→	M08			B08	
Address gate return	←	M09			B09	
Burst return	←	P04			D04	
Condition code in bit 0	←	D12	D12			
Condition code in bit 1	←	D13	D13			
Condition code in bit 2	←	B13	B13			
Cycle byte indicator	←	P10			D10	
Cycle input indicator	←	P09			D09	
Cycle steal request in	←	M02			B02	
Data bus bit 0	⟷	G02		B02		
Data bus bit 1	⟷	G03		B03		
Data bus bit 2	⟷	G04		B04		
Data bus bit 3	⟷	G05		B05		
Data bus bit 4	⟷	G07		B07		
Data bus bit 5	⟷	G08		B08		
Data bus bit 6	⟷	G09		B09		
Data bus bit 7	⟷	G10		B10		
Data bus bit P0	⟷	G12		B12		
Data bus bit 8	⟷	J02		D02		
Data bus bit 9	⟷	J04		D04		
Data bus bit 10	⟷	J05		D05		
Data bus bit 11	⟷	J06		D06		
Data bus bit 12	⟷	J07		D07		
Data bus bit 13	⟷	J09		D09		
Data bus bit 14	⟷	J10		D10		
Data bus bit 15	⟷	J11		D11		
Data bus bit P1	⟷	J12		D12		

Figure 2-28 (Part 1 of 2). I/O channel pin and cable assignments—signal lines

Line name	Direction	I/O pin assignment	I/O channel cable assignment #1	#2	#3	#4
Data strobe	→	M10			B10	
Halt or MCHK	→	M07			B07	
Initiate IPL	→	P07			D07	
IPL	←	S04				B04
Poll	→	M12			B12	
Poll identifier bit 0	→	P11			D11	
Poll identifier bit 1	→	S02				B02
Poll identifier bit 2	→	S03				B03
Poll identifier bit 3	→	P12			D12	
Poll identifier bit 4	→	P13			D13	
Poll prime	→	M13			B13	
Poll propagate	→	M11				
Poll return	←	M04			B04	
Power on reset (see Note)	→	S05				B05
Request in bus bit 0	←	S07				B07
Request in bus bit 1	←	S08				B08
Request in bus bit 2	←	S09				B09
Request in bus bit 3	←	S10				B10
Request in bus bit 4	←	S12				B12
Request in bus bit 5	←	S13				B13
Request in bus bit 6	←	U02				D02
Request in bus bit 7	←	U04				D04
Request in bus bit 8	←	U05				D05
Request in bus bit 9	←	U06				D06
Request in bus bit 10	←	U07				D07
Request in bus bit 11	←	U09				D09
Request in bus bit 12	←	U10				D10
Request in bus bit 13	←	U11				D11
Request in bus bit 14	←	U12				D12
Request in bus bit 15	←	U13				D13
Service gate	→	P05			D05	
Service gate return	←	P06			D06	
Status bus bit 0	→	J13		D13		
Status bus bit 1	→	G13		B13		
Status bus bit 2	→	M03			B03	
Status bus bit 3	→	P02			D02	
System reset	→	M05			B05	

Note: 'Power-on reset' at an I/O socket is the 'power-on reset' from the unit power supply powering the I/O socket. Pin S05 on the 4955 processor A-socket is not connected and is jumpered from S05 of the B-socket when an I/O attachment or repower feature is installed. 'Power-on reset' in the I/O channel cable is the unit 'power-on reset' from the next outboard I/O expansion unit.

Figure 2-28 (Part 2 of 2). I/O channel pin and cable assignments—signal lines

Voltage/ ground/ special pin	I/O socket	4952B/ 4953B,D/ 4955 A-socket	Corresponding I/O cable pin 1	2	3	4
B06	−12 V	Gnd	Gnd(B06)			
B11	+12 V	Gnd	Gnd(B11)			
D03	+5 V	+5 V	NC(D03)			
D08	Gnd	Gnd	Gnd(D08)			
G06	−5 V	Gnd		Gnd(B06)		
G11	+8.5 V	Gnd		Gnd(B11)		
J03	+5 V	+5 V		NC(D03)		
J08	Gnd	Gnd		Gnd(D08)		
M06	Res	Gnd			Gnd(B06)	
M11	Poll propagate	Gnd			Gnd(B11)	
P03	+5 V	+5 V			NC(D03)	
P08	Gnd	Gnd			Gnd(D08)	
S06	Res	Gnd				Gnd(B06)
S11	Res	Gnd				Gnd(B11)
U03	+5 V	+5 V				NC(D03)
U08	Gnd	Gnd				Gnd(D08)

Key:

Gnd = ground
NC = no connections at these pins.
Res = pins reserved for special system functions and features and are not to be connected to an I/O attachment.

Figure 2-29. I/O channel pin and cable assignments—special lines for A-socket and I/O cable

I/O Channel Physical Components Description

Refer to Figures 2-30 and 2-31 for the following description. The card sockets in a board are designated alphabetically from A (excluding I and O) starting at the left side of the board, viewed from the card side. Pin rows on the top socket of a card slot are designated B on the left and D on the right. The pins on the second socket are designated G on the left and J on the right. The pins on the third socket are designated M on the left and P on the right. The pins on the bottom socket are designated S on the left and U on the right. Each row of pins is numbered 2–13, top to bottom. Note that the contact assignments on the card are shown as viewed when facing the end of the card.

The center-to-center distance between card slots is 15.88 mm (0.625 in). The dimensions of a standard IBM card are 178 mm by 229 mm (7 in by 9 in). The clearance on the wiring side (left side as viewed from the front of the card file) is 5.6 mm (0.220 in), measured from the center of the card stock, and clearance on the component side is 10 mm (0.380 in), measured from the center of the card stock.

The maximum current that a device may draw through any single board pin is 3 amperes. Additionally, the maximum wattage per slot is 19 watts, total. Care must be taken to ensure that the power requirements for a new device are compared with the total power requirements for the particular system configuration. This ensures that the total power consumption remains below the maximum ratings for the power supply.

I/O channel cables are available in 0.61-m (2-ft) or 1.83-m (6-ft) lengths. They are 20-signal, unshielded cables with IBM connectors. Each connector contains three ground pins: D08, B06, and B11. There is no connection to pin D03 (see Figure 2-29).

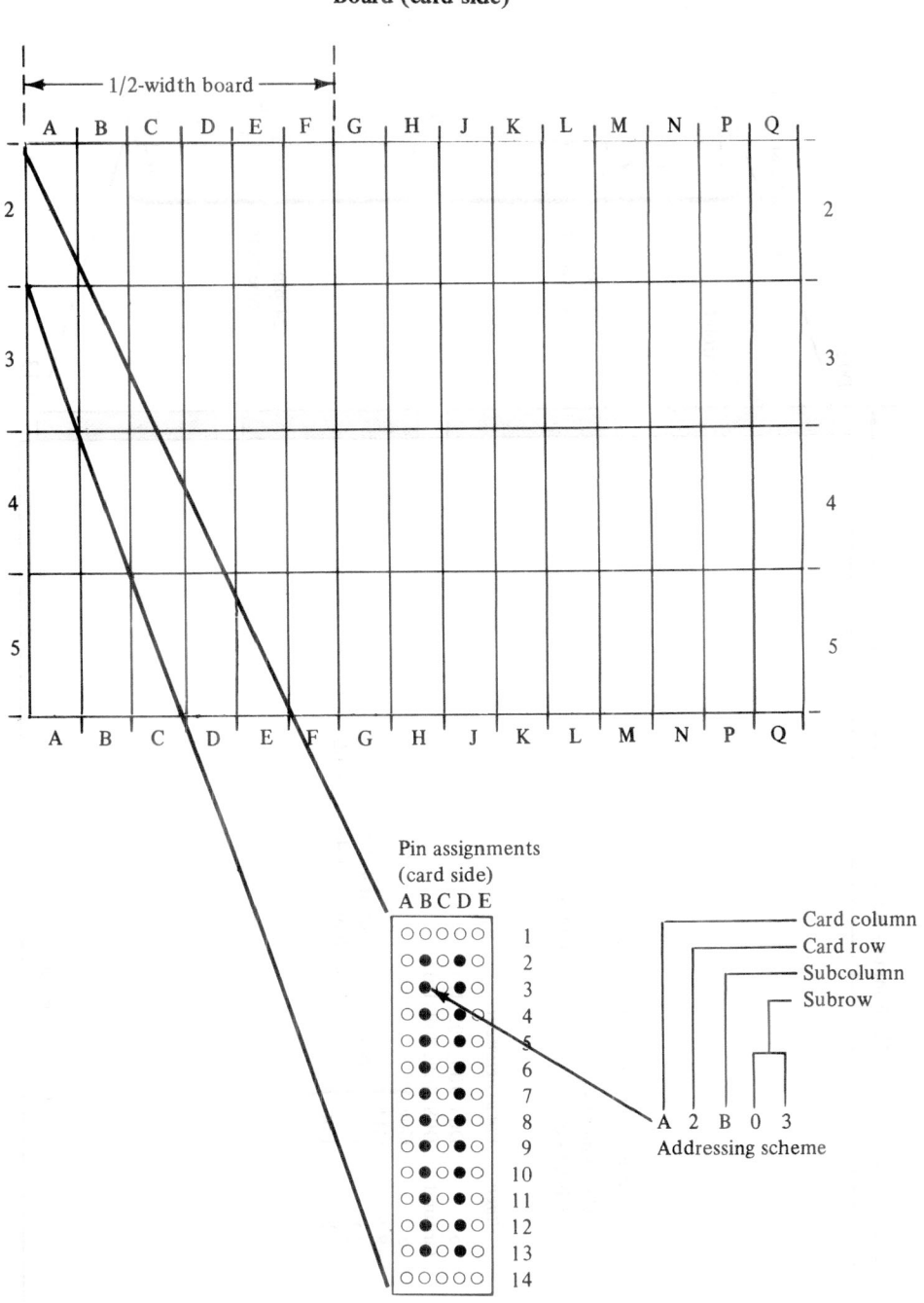
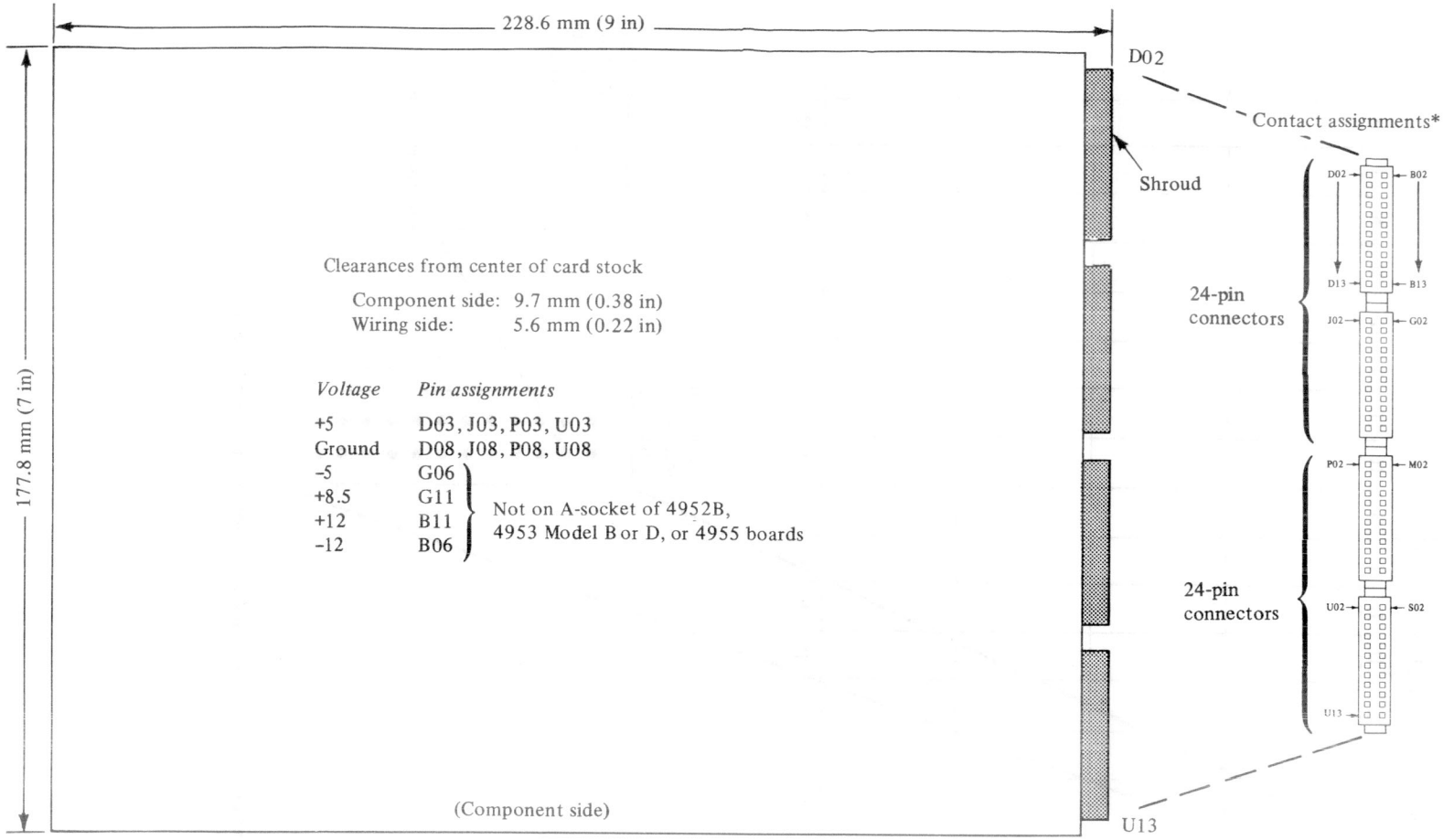


Figure 2-30. Processor and I/O expansion unit board identification



*Contact assignments are shown as viewed when facing the end of the card.

Figure 2-31. Standard IBM printed circuit card

Sequence of Plugging Device Attachments

The recommended procedure for installing device attachments into the I/O card file is to insert the attachment cards in an alphabetically *descending* sequential order, with no empty sockets between cards. To facilitate the removal of a device attachment from the I/O channel without interrupting the poll propagation, a bypass mechanism has been provided. This makes it possible to insert attachment cards in every other socket location without breaking continuity, but it is not advised to do so. Should a user wish to insert cards so that two or more empty sockets lie between two attachment cards, provisions must be made to ensure continuity of poll propagation when every other card *of the ones installed* are unplugged.

Processor I/O Channel Attachment Features

Channel Repower Feature

The channel repower feature, an IBM printed circuit card consisting of IBM and TTL technology, is designed to repower the processor I/O channel signal lines and to provide electrical isolation between I/O card files.

The processor I/O channel is received at the bottom of the channel repower feature card and the redriven signal lines are available at four top-card connectors (Figure 2-32). In normal configurations, the channel repower feature is plugged into the A-socket locations of the 4952, 4953 and 4955, or into the B-socket location of the 4959. The channel repower feature can also be inserted into any I/O socket for cabling out to a customer's attachment or card file. When used for this purpose, the repower feature must be the last series element directly plugged into the I/O channel. (This last element could be in the 4952, 4953, 4955, or the 4959, depending on the system configuration.) This is because the feature does not have any provision for propagating the poll back into the I/O socket. The repower feature can drive 14 general unit loads, or equivalent, through a maximum of 1.83 m (6 ft) of standard I/O channel cable. Only one series cable can be used to attach these loads. The feature does not provide dc logic voltages at its top-card connectors.

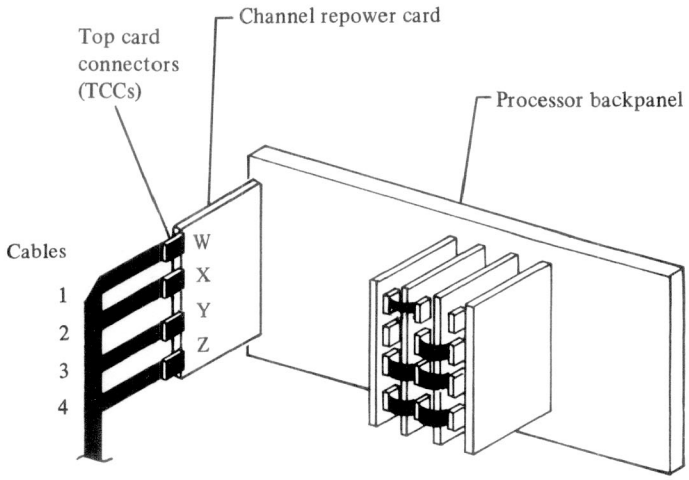


Figure 2-32. Channel repower feature—top card connectors

Direction logic for bidirectional address and data lines is provided on the feature so that its operation is transparent to the outboard I/O attachments. In the absence of any activity on the channel, the bidirectional buses (data bus and address bus) are shut off. The repower feature inhibits the outboard signal lines from affecting the availability of inboard devices when the outboard attachment or card file is powered down. 'Data strobe' is not propagated through the repower card unless either the 'address gate return' tag or the 'service gate return' tag coming from an outboard file is active.

The feature has a TTL-level compatible hysteresis receiver for the outboard 'power-on reset.' The receiver has a maximum current of 100 microamperes, which the outboard attachment or card file is required to sink at 0.45 V (most positive down level) when powered down or actively signalling 'power-on reset.'

The pin assignments for the repower feature are listed in Figure 2-33. The top-card connectors (TCCs) are standard IBM connectors, and receive standard I/O channel cables. For reference purposes, TCC pins W02, X02, Y02, and Z02 correspond to cable pins D02, J02, P02, and U02, respectively. Top card connectors W, X, Y, and Z correspond to cables 1, 2, 3, and 4, respectively. Therefore, when facing a repower feature that is plugged into an I/O socket, the W-connector is at the top and would receive cable 1 (see Figure 2-32).

Top-card connector pins W26, W31, X26, X31, Y26, Y31, Z26, and Z31 are grounds to receive the special grounds in the I/O channel cables. Pins W08, X08, Y08, and Z08 are also grounded pins, corresponding to the normal grounds supplied on an I/O socket. There are no connections to pins W03, X03, Y03, and Z03. These pins correspond to the normal +5-volt dc pins on an I/O socket (D03, J03, P03, and U03).

Line name	Direction	I/O pin assignment	TCC pin no.
Address bus bit 0	⟷	B02	W22
Address bus bit 1	⟷	B03	W23
Address bus bit 2	⟷	B04	W24
Address bus bit 3	⟷	B05	W25
Address bus bit 4	⟷	B07	W27
Address bus bit 5	⟷	B08	W28
Address bus bit 6	⟷	B09	W29
Address bus bit 7	⟷	B10	W30
Address bus bit 8	⟷	B12	W32
Address bus bit 9	⟷	D02	W02
Address bus bit 10	⟷	D04	W04
Address bus bit 11	⟷	D05	W05
Address bus bit 12	⟷	D06	W06
Address bus bit 13	⟷	D07	W07
Address bus bit 14	⟷	D09	W09
Address bus bit 15	⟷	D10	W10
Address bus bit 16	⟶	D11	W11
Address gate	⟶	M08	Y28
Address gate return	⟵	M09	Y29
Burst return	⟵	P04	Y04
Condition code in bit 0	⟵	D12	W12
Condition code in bit 1	⟵	D13	W13
Condition code in bit 2	⟵	B13	W33
Cycle byte indicator	⟵	P10	Y10
Cycle input indicator	⟵	P09	Y09
Cycle steal request in	⟵	M02	Y22
Data bus bit 0	⟷	G02	X22
Data bus bit 1	⟷	G03	X23
Data bus bit 2	⟷	G04	X24
Data bus bit 3	⟷	G05	X25
Data bus bit 4	⟷	G07	X27
Data bus bit 5	⟷	G08	X28
Data bus bit 6	⟷	G09	X29
Data bus bit 7	⟷	G10	X30
Data bus bit P0	⟷	G12	X32
Data bus bit 8	⟷	J02	X02
Data bus bit 9	⟷	J04	X04
Data bus bit 10	⟷	J05	X05
Data bus bit 11	⟷	J06	X06
Data bus bit 12	⟷	J07	X07
Data bus bit 13	⟷	J09	X09
Data bus bit 14	⟷	J10	X10
Data bus bit 15	⟷	J11	X11
Data bus bit P1	⟷	J12	X12

Figure 2-33 (Part 1 of 2). Channel repower feature pin assignments

Line name	Direction	I/O pin assignment	TCC pin no.
Data strobe	→	M10	Y30
Halt or MCHK	→	M07	Y27
Initiate IPL	→	P07	Y07
IPL	←	S04	Z24
Poll	→	M12	Y32
Poll identifier bit 0	→	P11	Y11
Poll identifier bit 1	→	S02	Z22
Poll identifier bit 2	→	S03	Z23
Poll identifier bit 3	→	P12	Y12
Poll identifier bit 4	→	P13	Y13
Poll prime	→	M13	Y33
Poll propagate	→	M11	--
Poll return	←	M04	Y24
Power on reset (see Note)	→	S05	Z25
Request in bus bit 0	←	S07	Z27
Request in bus bit 1	←	S08	Z28
Request in bus bit 2	←	S09	Z29
Request in bus bit 3	←	S10	Z30
Request in bus bit 4	←	S12	Z32
Request in bus bit 5	←	S13	Z33
Request in bus bit 6	←	U02	Z02
Request in bus bit 7	←	U04	Z04
Request in bus bit 8	←	U05	Z05
Request in bus bit 9	←	U06	Z06
Request in bus bit 10	←	U07	Z07
Request in bus bit 11	←	U09	Z09
Request in bus bit 12	←	U10	Z10
Request in bus bit 13	←	U11	Z11
Request in bus bit 14	←	U12	Z12
Request in bus bit 15	←	U13	Z13
Service gate	→	P05	Y05
Service gate return	←	P06	Y06
Status bus bit 0	→	J13	X13
Status bus bit 1	→	G13	X33
Status bus bit 2	→	M03	Y23
Status bus bit 3	→	P02	Y02
System reset	→	M05	Y25

Note: 'Power on reset' at the top-card connector pin Z25 is the 'power-on reset' from the next outboard I/O expansion unit. Neither this 'power-on reset' nor the 'power-on reset' at the bottom of the card are repowered (both of these resets are used in the card for control logic).

Figure 2-33 (Part 2 of 2). Channel repower feature pin assignments

Socket Adapter Feature

The socket adapter feature allows customer access to the Series/1 I/O channel. The channel socket adapter is a two-component system to adapt the 1-mm (0.040-in) IBM backpanel configuration to a 1.5-mm (0.060-in) industry connector (see Figure 2-34). The first component is a 64-mm (2.53-in) high IBM socket card (paddle card) with gold-plated, printed-circuit tabs on the opposite end. The second component is a modified 72-pin Continental* double billows feed-through connector to allow customer access to 72 pins of the I/O channel. No logic electronics are provided on the channel socket adapter; it is only a mechanical adapter.

This assembly is plugged into any of the Series/1 I/O sockets. The customer then plugs his 1.5-mm (0.060-in) printed circuit logic card into the 72-pin connector. Dimensions for a customer printed circuit card, which is designed to use the socket adapter feature, are shown in Figure 2-35.

The maximum amount of current a customer logic card may draw when using the socket adapter feature is 3 amperes at +5 volts. Each customer signal line directly connected to the Series/1 I/O channel must conform to the electrical specifications described in "Processor I/O Channel Electrical Characteristics" in this chapter. The 'poll' and 'poll prime' signals must be propagated as described in "Poll Sequence Description" in this chapter. As viewed from the Continental-connector side of the socket adapter feature, each customer signal line must have a characteristic impedance of between 60 and 120 ohms, and must present a nominal capacitive load, as described in this section. The customer-supplied I/O channel drivers and receivers must be located on the logic card (Figure 2-35) that connects directly to the socket adapter.

The I/O channel is designed to support a nominal 30 pf per line per drop. As discussed in "Unit-Load Characteristics" in this chapter, TTL loads may be substituted for general unit loads, resulting in an allowable maximum of 60 pf for a single drop with TTL loads. The socket adapter is assumed to be nominally 10 pf, yielding a customer-load maximum of 20 pf for a general load or 50 pf for a TTL load.

The signal lines available from the socket adapter are the same as for a standard I/O channel, but with only four 'request in bus' lines, corresponding to levels 0–3. The +5 volts dc is available on pin D02. Figure 2-36 contains the IBM backpanel-to-Continental-connector pin assignment translation.

---

* Manufactured by Continental Connector Corporation

Because the socket adapter is designed primarily for use by a technical expert, the customer is responsible for the operation of the design. To achieve adequate results, good design practices—both electrical and mechanical—must be adhered to. Components are to be no higher than 11 mm (0.440 in) from the surface of the card. No more than 15 watts are to be dissipated on the card. Only logic voltages should be used (less than 24 volts dc) to avoid safety problems. The customer is responsible to evaluate the exposure to the vibrational forces or translational forces caused by any customer cables that may be attached to the card. The card size used must be specified.

IBM BEARS NO RESPONSIBILITY for customer logic or hardware.

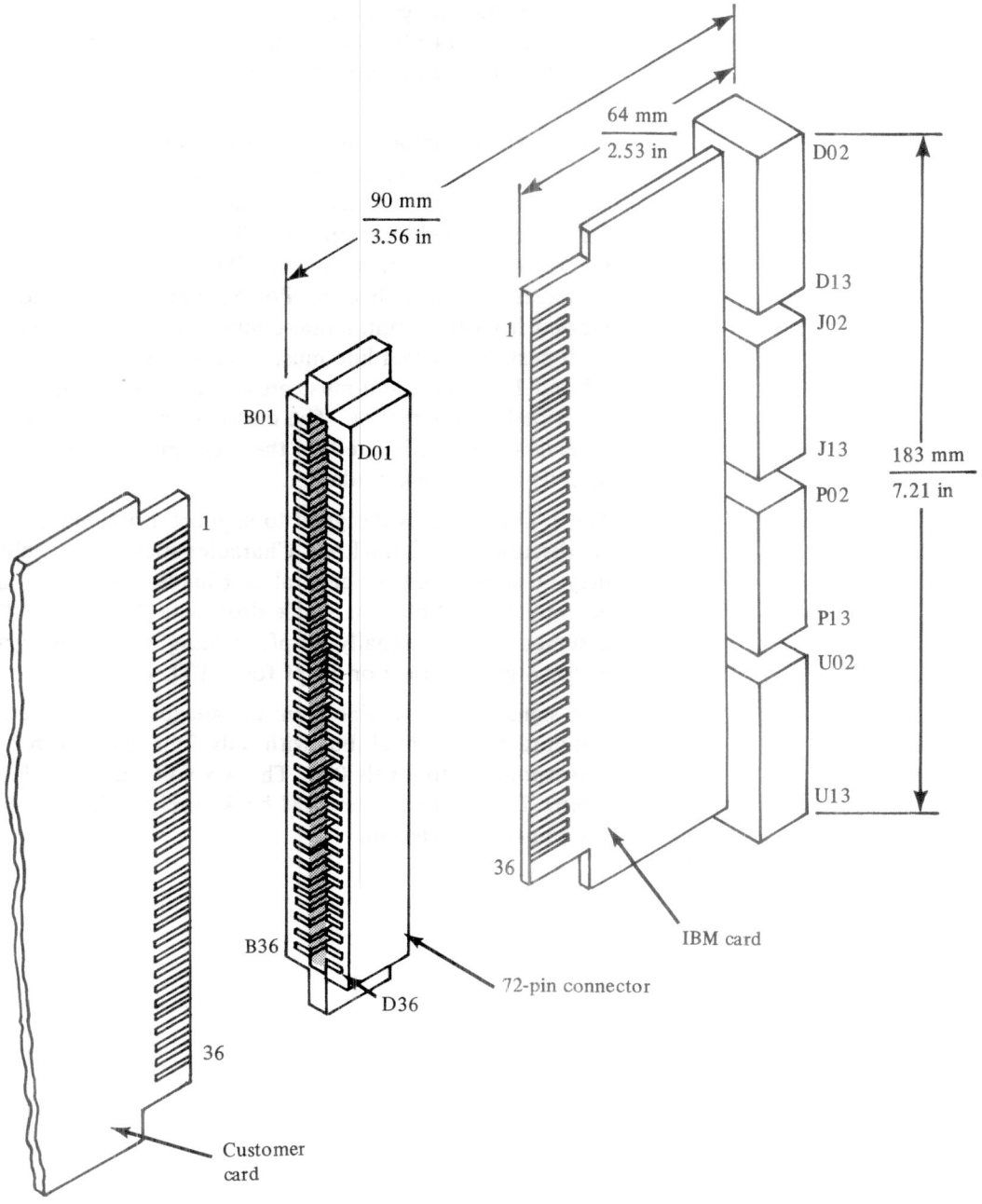


Figure 2-34. Socket adapter and customer card

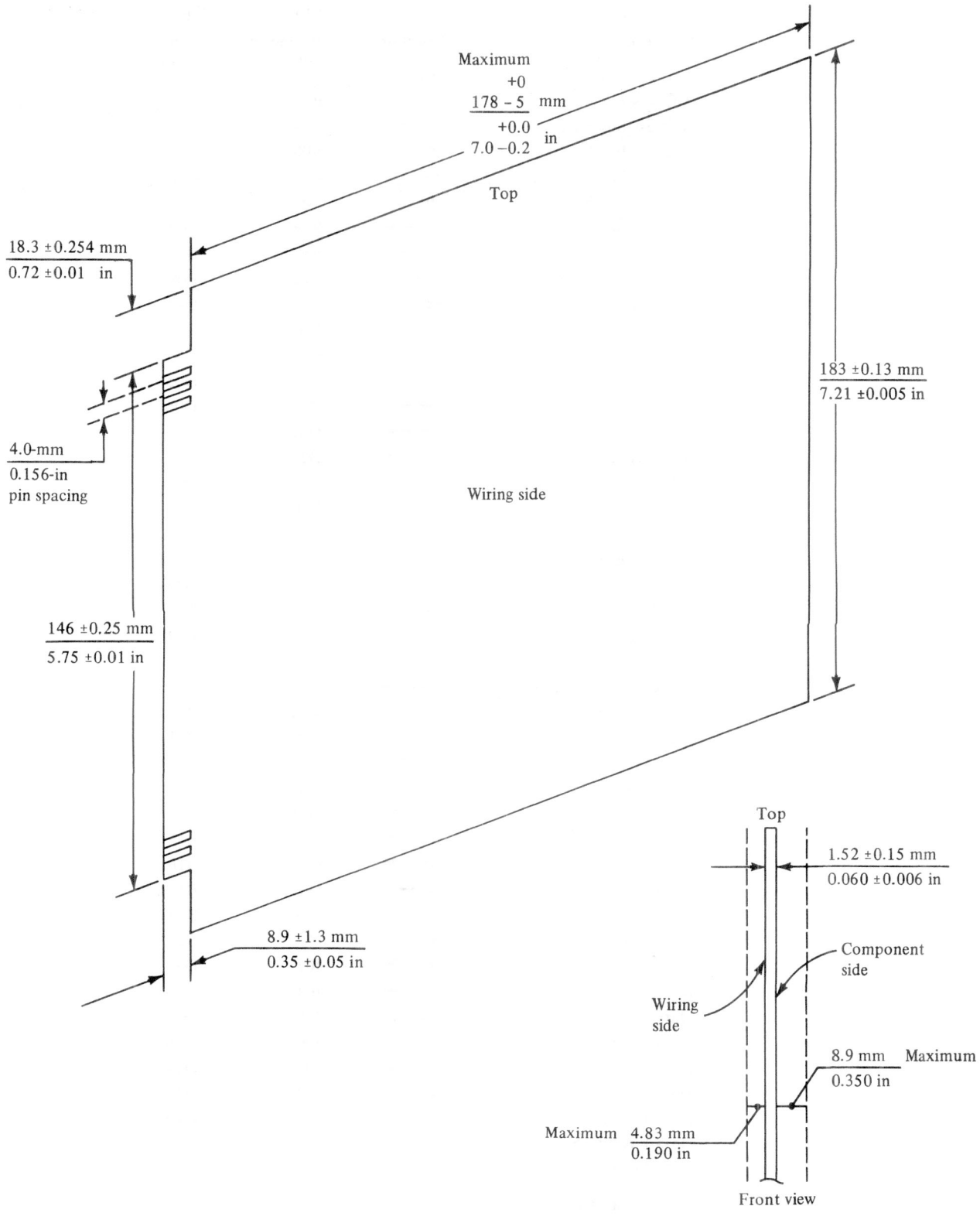


Figure 2-35. Customer card for the socket adapter feature

Line name	Direction	I/O pin assignment	Customer card socket
Address bus bit 0	⟷	B02	B01
Address bus bit 1	⟷	B03	B02
Address bus bit 2	⟷	B04	B03
Address bus bit 3	⟷	B05	B04
Address bus bit 4	⟷	B07	B05
Address bus bit 5	⟷	B08	B06
Address but bit 6	⟷	B09	B07
Address bus bit 7	⟷	B10	B08
Address bus bit 8	⟷	B12	B09
Address bus bit 9	⟷	D02	D01
Address bus bit 10	⟷	D04	D03
Address bus bit 11	⟷	D05	D04
Address bus bit 12	⟷	D06	D05
Address bus bit 13	⟷	D07	D06
Address bus bit 14	⟷	D09	D08
Address bus bit 15	⟷	D10	D09
Address bus bit 16	→	D11	D10
Address gate	→	M08	B26
Address gate return	←	M09	B27
Burst return	←	P04	D24
Condition code in bit 0	←	D12	D11
Condition code in bit 1	←	D13	D12
Condition code in bit 2	←	B13	B10
Cycle byte indicator	←	P10	D29
Cycle input indicator	←	P09	D28
Cycle steal request in	←	M02	B21
Data bus bit 0	⟷	G02	B11
Data bus bit 1	⟷	G03	B12
Data bus bit 2	⟷	G04	B13
Data bus bit 3	⟷	G05	B14
Data bus bit 4	⟷	G07	B15
Data bus bit 5	⟷	G08	B16
Data bus bit 6	⟷	G09	B17
Data bus bit 7	⟷	G10	B18
Data bus bit P0	⟷	G12	B19
Data bus bit 8	⟷	J02	D13
Data bus bit 9	⟷	J04	D14
Data bus bit 10	⟷	J05	D15
Data bus bit 11	⟷	J06	D16
Data bus bit 12	⟷	J07	D17
Data bus bit 13	⟷	J09	D18
Data bus bit 14	⟷	J10	D19
Data bus bit 15	⟷	J11	D20
Data bus bit P1	⟷	J12	D21

Figure 2-36 (Part 1 of 2). Channel socket adapter pin assignment translation

Line name	Direction	I/O pin assignment	Customer card socket
Data strobe	→	M10	B28
Halt or MCHK	→	M07	B25
Initiate IPL	→	P07	D27
IPL	←	S04	B34
Poll	→	M12	B30
Poll identifier bit 0	→	P11	D30
Poll identifier bit 1	→	S02	B32
Poll identifier bit 2	→	S03	B33
Poll identifier bit 3	→	P12	D31
Poll identifier bit 4	→	P13	D32
Poll prime	→	M13	B31
Poll propagate	→	M11	B29
Poll return	←	M04	B23
Power on reset	→	S05	B35
Request in bus bit 0	←	S07	B36
Request in bus bit 1	←	S08	D33
Request in bus bit 2	←	S09	D35
Request in bus bit 3	←	S10	D36
Request in bus bit 4	←	S12	N-C
Request in bus bit 5	←	S13	N-C
Request in bus bit 6	←	U02	N-C
Request in bus bit 7	←	U04	N-C
Request in bus bit 8	←	U05	N-C
Request in bus bit 9	←	U06	N-C
Request in bus bit 10	←	U07	N-C
Request in bus bit 11	←	U09	N-C
Request in bus bit 12	←	U10	N-C
Request in bus bit 13	←	U11	N-C
Request in bus bit 14	←	U12	N-C
Request in bus bit 15	←	U13	N-C
Service gate	→	P05	D25
Service gate return	←	P06	D26
Status bus bit 0	→	J13	D22
Status bus bit 1	→	G13	B20
Status bus bit 2	→	M03	B22
Status bus bit 3	→	P02	D23
System reset	→	M05	B24

Note:
Customer card socket pin D02 provides +5 volts dc; pins D07 and D34 provide ground.

Figure 2-36 (Part 2 of 2). Channel socket adapter pin assignment translation

Chapter 3. Timer Feature

Introduction

The timer feature provides two 16-bit timers: timer 0 and timer 1 (Figure 3-1). Each timer can be used as an interval timer, a pulse counter, or a pulse duration counter with end interrupt. The timers are packaged on one printed circuit card, which plugs into a backpanel that distributes the processor I/O channel signal lines. Electrical power for the timer circuitry is obtained from the backpanel through card-connector pins.

The timer feature also has a 16-pin connector that allows the timers to be used with external signals. Each timer has two output lines, 'run state' and 'external gate enable,' and two input lines, 'customer clock' and 'external gate.' Drivers and receivers for these lines are TTL-compatible.

The two timers are separately addressable and are independently started, stopped, read, or set to any value under program control. The timers can be read without disturbing their operation; however, to set the timer's value or mode, it must be stopped.

Each timer also has a mode register that is used to select one of four internal time bases or an external time base. The internal time bases are 1, 5, 25, and 50 microseconds. The external time base is provided by the user and must be equal to or greater than 20 microseconds when the input is filtered, or 1 microsecond when not filtered. The timer value is decremented with the selected time base. For additional information, see "Receivers" in this chapter. An external gate enable bit is also contained in the mode register. Both the time base and the external gate enable bit are program-selectable.

The program-selectable running modes available for each timer are:

- Periodic interrupts—internal. A 16-bit auto-load register is set to any value by program control. This register automatically reloads the timer when the timer underflows, and causes an interrupt to be generated. This allows periodic interrupts to be generated on 65,536 possible base values of the timer without program intervention.
- Aperiodic interrupts—internal. The timer is loaded with a value, under program control, and an interrupt occurs when the timer underflows. After the first interrupt, the timer is *not* reloaded from the auto-load register and, therefore, counts the full 65,536 counts before the next interrupt occurs, unless a new value is loaded, under program control.
- Periodic or aperiodic interrupts—external. The timer generates periodic or aperiodic interrupts, but timer start and stop is controlled by the external gate when the timer is in the run state.

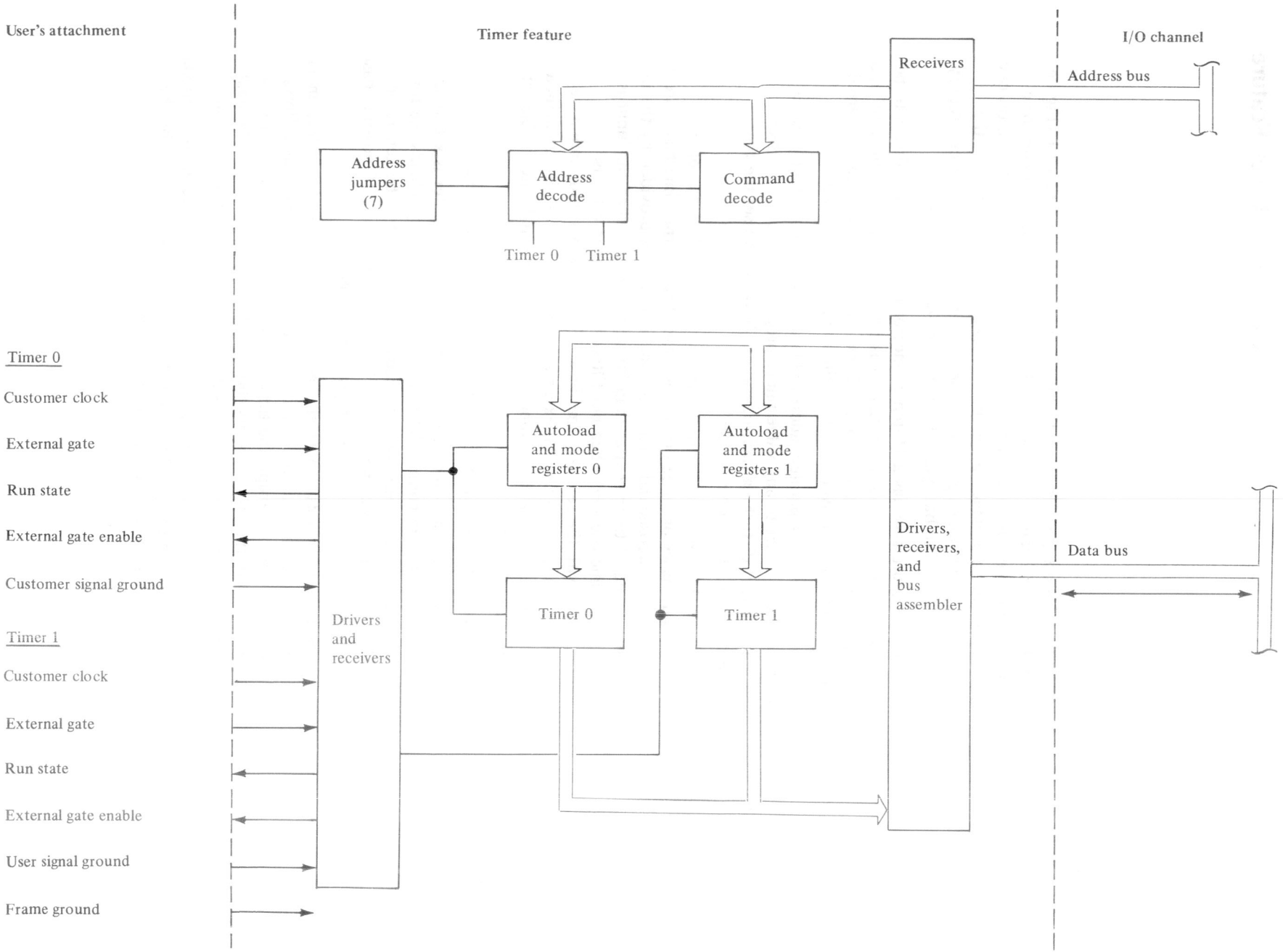


Figure 3-1. Block diagram of timer feature

The timer feature is addressed with the seven most-significant bits of the device address field in the IDCB. The least-significant bit selects one of the two timers within the attachment for all commands (except Prepare, where it is ignored). By convention, when the least-significant bit is 0, timer 0 is selected; when the least-significant bit is 1, timer 1 is selected. The seven most-significant bits of the address are changeable by jumper on the card; the least-significant bit is not changeable.

The timer feature is a DPC device and has no cycle-steal or IPL capabilities.

The timer feature is connected to the processor I/O channel through the following buses, as described in detail in Chapter 2:

- Data bus—16 bits wide, bidirectional, with parity checking and generating (odd parity per byte).
- Address bus—17 bits wide (0–16), receiving only; bit 16 is used to denote a DPC device command and to gate receivers active.
- Request in bus—16 bits wide, driving only.

Relationship to Other Features

The timer card is plugged into any I/O position of an IBM 4955 or 4953 Processor or any position of an I/O expansion unit. There is no limit to the number of timer cards that can be used in a system.

There is an optional filtering capability of the customer digital input lines brought into the timer card. This option is selected with jumper wires on the component side of the timer card either for TTL input or filtered TTL input. The location of the jumper wires is illustrated in Figures 3-2 and 3-3.

Application Summary

The following paragraphs describe the use of the timer feature. The X appearing after the word "timer" denotes either timer 0 or timer 1.

High Accuracy or Nonstandard Frequency Counting

To utilize a clock of any arbitrary accuracy or frequency up to 1MHz, the 'timer X customer clock' input should be used, and the timer mode controls should be set to select the customer time base.

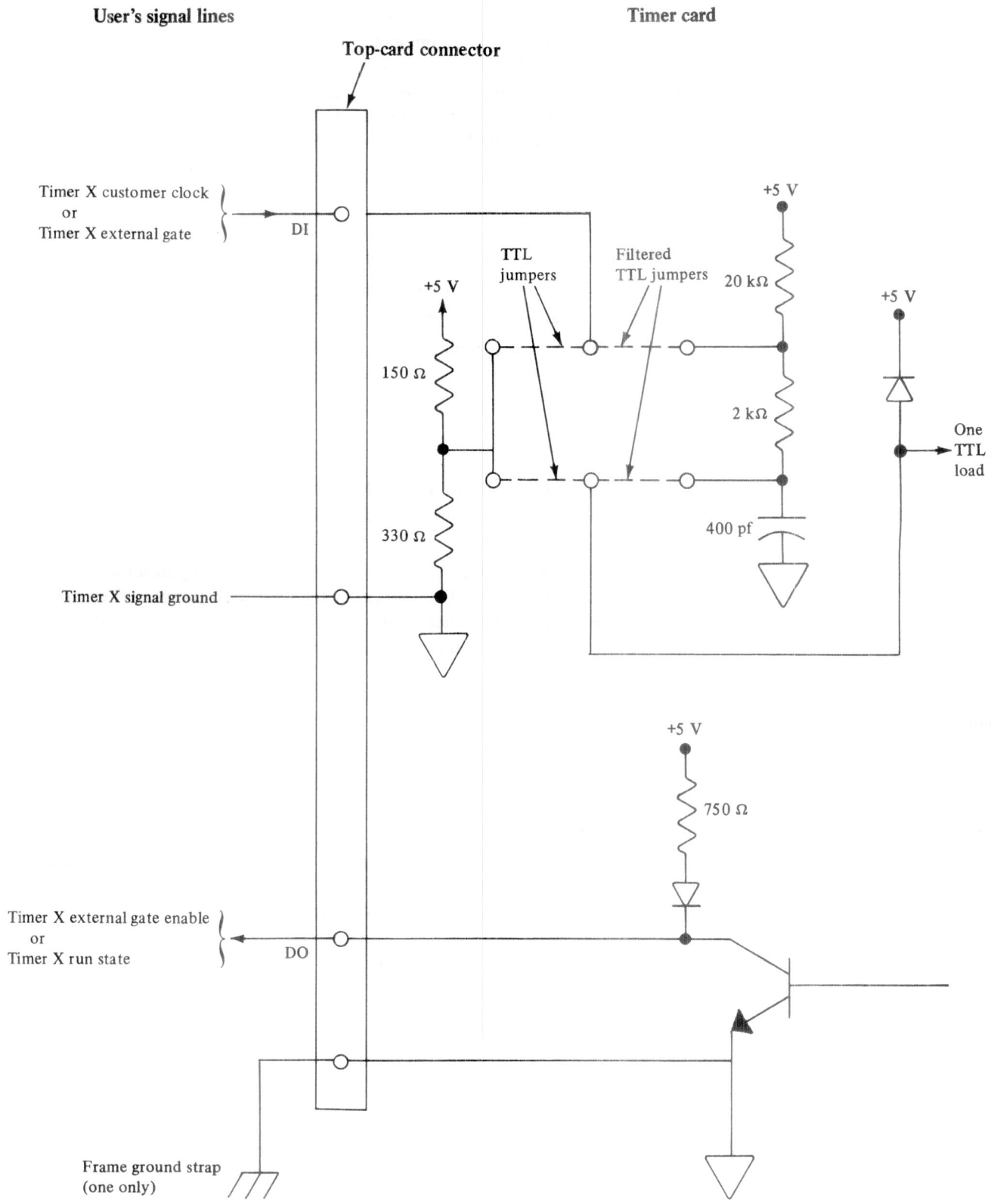
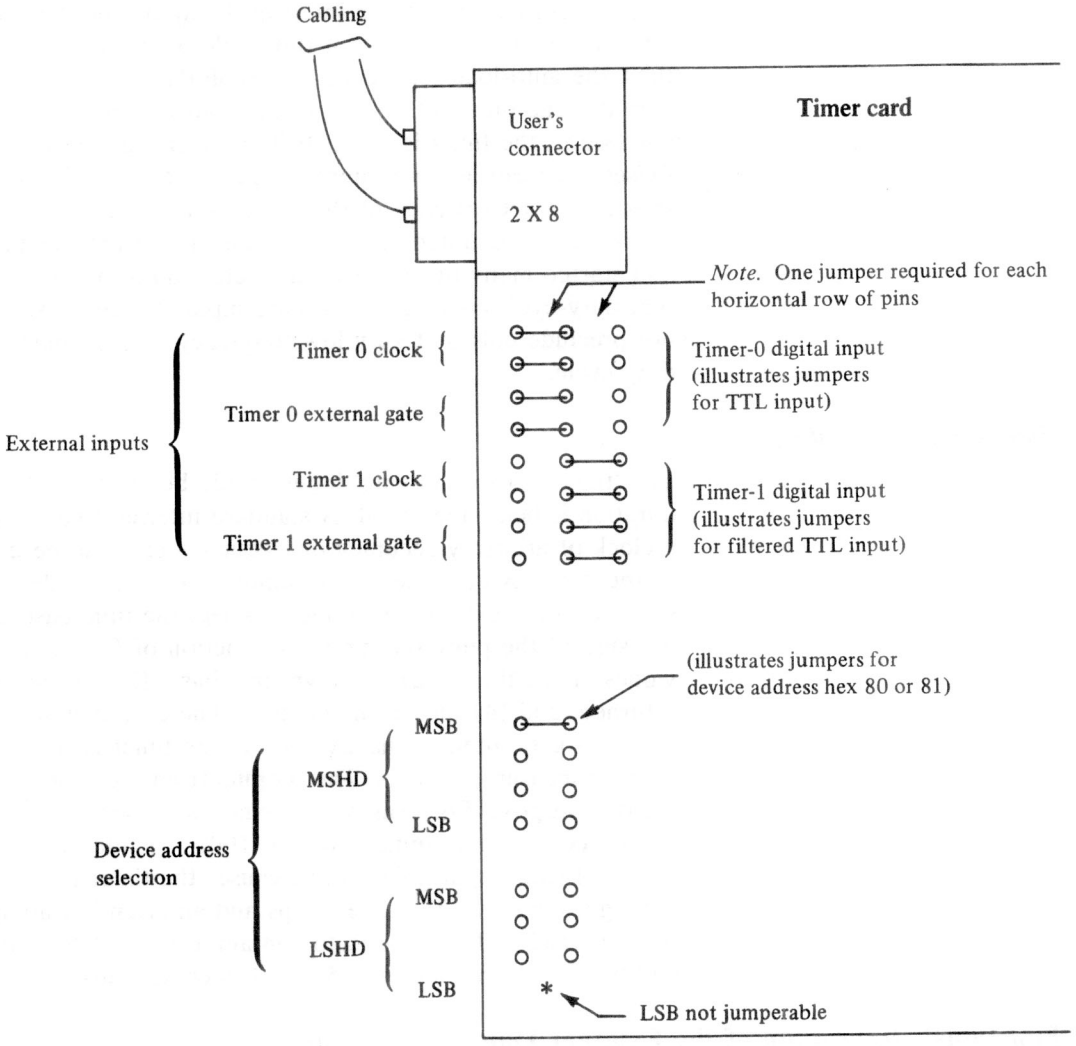


Figure 3-2. Driver/receiver circuits on the timer card



Key:

MSB = most-significant bit
LSB = least-significant bit
MSHD = most-significant hexadecimal digit
LSHD = least-significant hexadecimal digit

Figure 3-3. Jumper selections on the timer card

Pulse or Event Counting

The 'timer X customer clock' input should be used, and the timer mode controls should be set to select the customer time base. The number of pulses recorded prior to an interrupt being posted depends on the value set into the timer and the chosen run mode. For example, if the timer (and, thus, the auto-load register) is set to all 0's, and the chosen run mode is periodic, the timer interrupts on each pulse counted. If, under these same conditions, the timer is set to 100, it interrupts on every 101st pulse. Pulses are recorded and interrupts generated at the leading (passive-to-active) edge of the pulse. Also, except for power-on reset, every pulse is counted only once even though the timers could be stopped and started many times during the active duration of a given pulse. Note that duty-cycle constraints on pulse inputs for the customer clock input do not preclude pulses of very low frequency or even pulses with a random duty cycle.

Pulse Duration Counting

The 'timer X external gate' input should be used for the pulse whose duration is being measured. A standard internal time base can be used, or a clock of arbitrary accuracy or frequency can also be used and connected to the 'timer X customer clock' input. The timer mode controls should be set to arm the external gate and to select the time base desired. The measure of the pulse duration is a function of (1) the initial and end values of the timer, (2) a known time base, (3) the type of interrupt returned, and (4) the run mode used. The customer should ensure that the 'external gate' input is inactive before the timer is set to run state, or an error in measuring occurs. The outputs from the timer card are available for this purpose. For example, assume that clock inputs occur every 1 microsecond and an initial value of 1000 is loaded into the timer. Then, 'external gate' input going active causes the timer to start. When 'external gate' goes inactive, the timer stops and an attention interrupt occurs. The timer is read and it is found to contain a value of 500; therefore, the pulse width of 'external gate' was 500 ± 1 microseconds.

Functional Description of the External Timer Signal Lines

There are four external signal lines per timer. These signal lines permit control of the timer with a user-provided time base and gate. The following table lists the external signal lines:

Signal	Direction	Active level*
Timer X customer clock	To timer	Down
Timer X external gate	To timer	Down
Timer X run state	From timer	Down
Timer X external gate enable	From timer	Down

*All signals are down-level (minus) active.

Signal Line Considerations

The timer attachment digital outputs are solid state switches that can be used with or without a customer source voltage. See "Drivers" in this chapter.

The timer attachment digital inputs are TTL-compatible, and a jumper-wire option is available on the card to provide a filter for these inputs, if required in a noisy environment. A loss of frequency response is the result of using the optional filter. Without filtering, the input rate can go up to 1 MHz. With filtering, the input rate drops to 50 kHz, worst case. For additional information, see "Jumper Selections" in this chapter.

Timer X Customer Clock

'Timer X customer clock' is the input for the user-supplied clock or for a random pulse train. This input uses the down level, and not the down transition, as active.

Timer X External Gate

'Timer X external gate' is the input for the user-supplied gate signal. It is only effective when the external gate control is enabled. This input uses the down level, and not the down transition, as active.

Timer X Run State

'Timer X run state' is an output signal that indicates that the timer is in the run state. Its primary purpose is for state synchronization of the timer X external gate cycle. This signal becomes active with a Start Timer command and remains active until a Stop Timer command is accepted, the 'timer X external gate' signal becomes inactive, or a halt/reset occurs.

Timer X External Gate Enable

'Timer X external gate enable' is an output signal that indicates that the external gate has been enabled through bit 15 of the Set Timer Mode command.

Application Sequences

Interval Timer

Perform the following steps to use the timer as an interval timer with an external time base (customer clock input):

1. Prepare timer.
2. Set timer period and initial value.
3. Set timer mode (external time base—bit 14 of the IDCB data word set to 1).
4. Start timer periodic.

The timer starts counting clock pulses and interrupts when the counter underflows.

Pulse Counter

Perform the following steps to use the timer as a pulse counter with the external customer clock input:

1. Prepare timer 0 to interrupt in internal mode with the time base at some prescribed interval (for example, 1 second).
2. Load timer 1 with a value that is larger than the number of expected external pulses.
3. Set up timer 1 to receive customer clock (external time base) in aperiodic mode.
4. Have timer 0 interrupt initiate a read timer 1 value in the processor. Subtract the present timer 1 value from the original value of timer 1.
5. Reload the starting value into timer 1 to repeat the cycle.

The customer clock counts per second can be read into the processor.

Pulse Duration Counter

Perform the following steps to use the timer as a pulse-duration counter:

1. Prepare timer.
2. Set timer period and initial value for a value greater than the width of the expected pulse.
3. Set timer mode for external gate control (bit 15 of the IDCB data word set to 1).
4. Start timer.
5. 'Run state' to customer interface becomes active.
6. 'External gate' active starts the timer, and it starts counting.
7. At the fall of 'external gate,' the timer stops running and an attention interrupt is presented to the channel. Read the timer and subtract present value from original value. The result is the pulse duration of the 'external gate' line in terms of the time base selected.
8. Reload the starting value into the timer to repeat the cycle.

Timer Feature Operational Characteristics

Interrupts

Reported at Interrupt Time

The interrupt condition codes (CCs) are described in this section to aid in the understanding of interrupt presentation.

CC value	Meaning
2	Exception
3	Device end
4	Attention
6	Attention and exception
7	Attention and device end

CC2 *Exception*—An overrun condition has occurred in the timer. Overrun means that a device-end interrupt condition occurs while a previous device-end interrupt is still pending in the timer.

CC3 *Device End*—Reported when the timer has decremented one more than the specified number of time intervals (underflow). Also reported when 'external gate' has been enabled and the timer detects an underflow prior to the end of one complete external gate cycle.

CC4 *Attention*—Reported only when an external gate cycle has been completed prior to a timer underflow; 'run state' is reset.

CC6 *Attention and Exception*—Reported if the external gate cycle has been completed and an overrun condition is present in the timer; 'run state' is reset (see CC2).

CC7 *Attention and Device End*—Reported when a timer has underflowed prior to, or at the same time as, the completion of an external gate cycle; 'run state' is reset.

Interrupt Presentation

The timers are prepared together and function as one preparable source. Neither timer should be started unless the I-bit is on.

After the timers start, they post the first device-end interrupt in a time interval corresponding to the specified count up to a maximum of one more count. For example, if a count of hex 0003 is loaded (3 counts), the actual time to the first device-end interrupt ranges from 3 to 4 times the selected time base. This is because of the asynchronous nature of the internal free-running oscillator or external-pulse train, with respect to the program setting of 'run state' or the activation of 'external gate.' This uncertainty must be taken into account only once each time a timer is started.

There is also an uncertainty associated with the value of the timers when measuring the duration of 'external gate' in pulse-duration applications. This is because of the asynchronous nature of the 'external gate' deactivation, with respect to the internal clock or external pulse train. This uncertainty is the time corresponding to ± 1 count in the timer value after it is stopped.

Pulse-averaging applications that use a known fixed-time of 'external gate' activation and random pulses on the 'customer clock' input must also take into account a ± 1 count uncertainty in the timer value after it is stopped by the deactivation of 'external gate.'

Status After Power Transitions and Resets

When a machine check occurs, or when a Halt I/O or Device Reset command is executed, the timers are stopped, 'run state' is reset, the mode register is reset, and any pending interrupt requests are reset. The prepare field, including the I-bit, and the value in the timers are not reset.

When a system reset occurs, both timers are stopped, 'run state' is reset, and the mode registers are reset. The values held in the timers and auto-load registers are not reset. The prepare field, including the I-bit, is reset.

When a power-on reset occurs, all resets caused by system reset occur; in addition, the timers are reset to their maximum value (that is, all 1's), and the auto-load registers are set to their maximum value.

Timer Feature Electrical Characteristics

Refer to Figure 3-2 for the driver/receiver circuits.

Receivers. The timer inputs jumpered for TTL input meet the following specifications:

Input voltage:	
Up level:	+5.5 volts, maximum; +2.4 volts, minimum
Down level:	+0.6 volt at 40 mA, maximum; 0.0 volt, minimum
Input impedance:	≥100 ohms

The input rate must be 1 MHz or less. The input should be on for at least 300 nanoseconds and off for at least 300 nanoseconds at any input rate.

The timer inputs jumpered for filtered TTL input meet the following specifications:

Input impedance:	≥9.2 kilohms at less than 4.5 V; ≥2 kilohms at +24 V
Input limits:	+24 Vdc, maximum; −24 Vdc, minimum
Logical 1:	≤1.0 Vdc
Logical 0:	≥2.5 Vdc
Maximum repetition rate:	50 kHz worst case, with 50% duty cycle

Worst-case condition is an open collector driver. If an active collector driver is used to drive the input points, the maximum repetition rate increases substantially to approach 500 kHz. This is determined by the charging time of the filter (shown in the receiver circuit in Figure 3-2).

Each input point has an internal pull-up resistor, regardless of whether the input is jumpered for filtered or nonfiltered input. Unconnected inputs are held at the inactive state (up level).

Drivers. The timer outputs meet the following specifications:

Output voltage:

1. With user source:

Off state:	+52.8 Vdc, maximum
On state:	+0.8 Vdc, maximum

2. Without user source:

Off state:	+5.5 Vdc at 0.0 mA source, maximum; +2.4 Vdc at 1.0 mA source, minimum
On state:	+0.8 Vdc, maximum
Current input:	
On state:	100 mA per point with user source, maximum
Off state:	500 μA per point at +52.8 Vdc user source, maximum

Because the performance of this interface may be affected by noise, appropriate arc suppression, noise filtering, etc., may be necessary on the user's inputs.

Timer Feature Physical Characteristics

Signal Pin Assignments

The external interface is available at the top of the timer card on a 2 x 8 polarized top-card connector (TCC). See Figure 3-4. The pin assignments are:

Pin	Signal
A01	Timer 0 clock
A02	Timer 0 external gate
A03	Timer 0 run state
A04	Timer 0 external gate enable
A05	Timer 0 customer signal ground
A06	Not used
A07	Not used
A08	Frame ground strap
B01	Not used
B02	Not used (polarizing pin)
B03	Not used
B04	Timer 1 customer signal ground
B05	Timer 1 external gate enable
B06	Timer 1 run state
B07	Timer 1 external gate
B08	Timer 1 clock

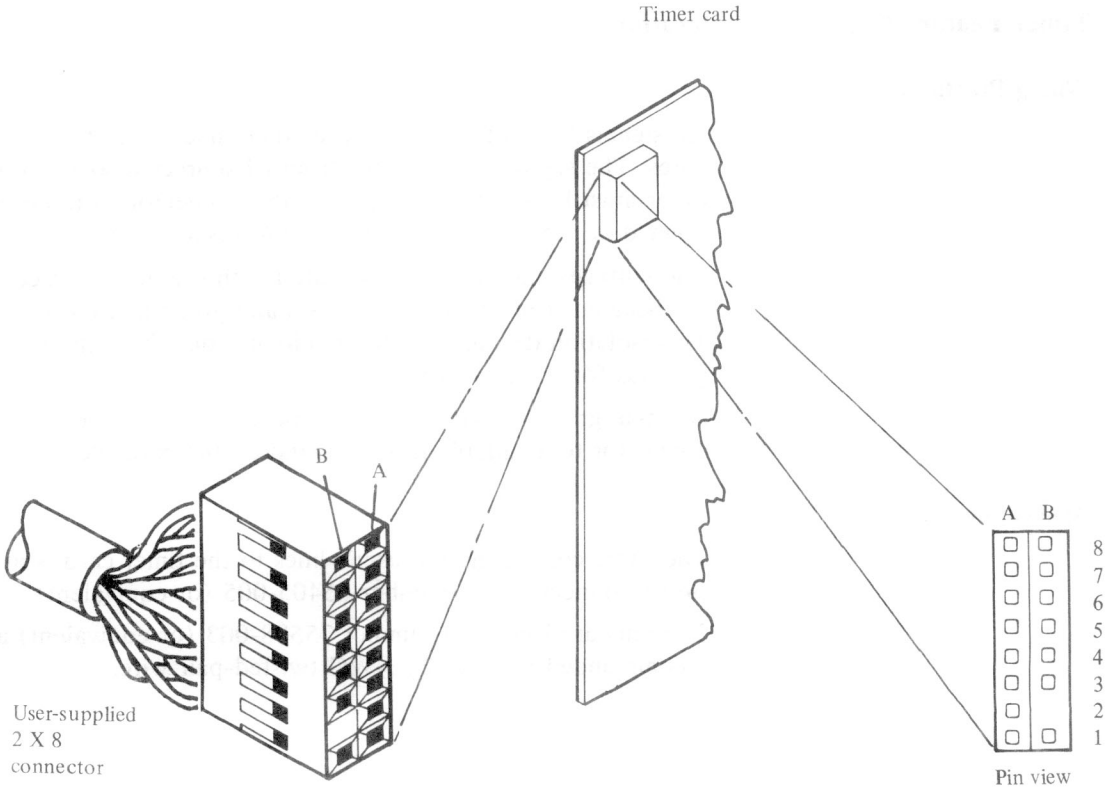


Figure 3-4. Timer card and cable connector

Pin Assignments Showing Customer Access Panel (CAP) Connections

If the customer access panel (CAP) feature (#1590) is ordered, the cable from the top-card connector (TCC) is built-in and connected as follows:

		Timer 0		Timer 1	
Name		*TCC pin*	*CAP pin*	*TCC pin*	*CAP pin*
Customer clock	+	A01	A	B08	U
	–	A05	E	B04	Y
	Shield	Frame	K	Frame	C
External gate	+	A02	C	B07	S
	–	A05	H	B04	W
	Shield	Frame	M	Frame	A
Run state	+	A03	B	B06	V
	–	A05	F	B04	Z
	Shield	Frame	L	Frame	D
External gate enable	+	A04	D	B05	T
	–	A05	J	B04	X
	Shield	Frame	N	Frame	b

Jumper Selections

Refer to Figure 3-3 for the jumpers required on the timer card for the external signal lines and device addressing.

Timer Feature Design Considerations

Wiring Practices

All signals brought into the top-card connector must be via twisted-pair wires. The signal ground wires from all sources associated with a particular timer must be soldered together at the connector card and brought into timer 0 or timer 1 on pin A05 or B04, respectively.

The voltages and grounds associated with the drivers, receivers, and filter are isolated from the timer voltages and grounds used for the timer card. This isolation decouples external circuit noise from the digital voltages and grounds for the timer card.

A single ground strap must be connected from A08 on the top-card connector to a suitable frame ground on the card file.

Application Notes

The cable connecting the user's lines to the timer card is made with a Berg* connector part number 65405-005 (or equivalent).

The pins are Berg part number 75598-003 (or equivalent) and the recommended wire is #24 AWG twisted-pair wire.

* Berg Electronics, Division of E.I. duPont de Nemours & Co., Inc.

Chapter 4. Teletypewriter Adapter Feature

Introduction

The teletypewriter adapter feature (Figure 4-1) is designed primarily to attach teletypewriter I/O devices to the processor I/O channel. The adapter may also be used to attach other devices that satisfy the requirements of the interface. The feature offers signal and bit-rate selectability by using the appropriate pins of a 16-pin top-card connector and by jumpering the pins on the feature card.

The teletypewriter adapter feature has a four-wire interface for data exchange—two for receive and two for transmit. Operation is full-duplex; that is, data may be transmitted and received concurrently.

The input options offered are:

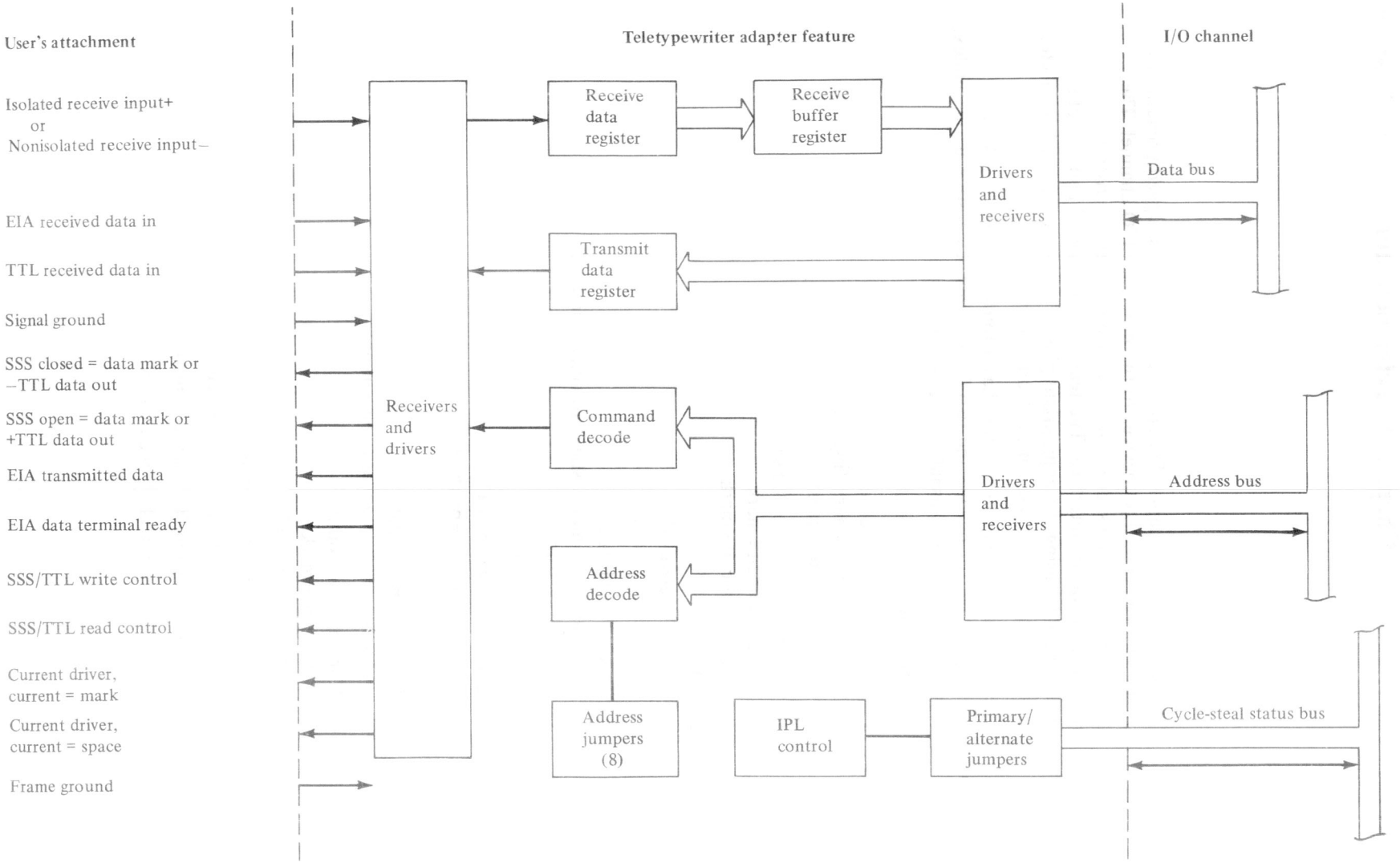
- Isolated contact sense
  - Open circuit=mark (logical 1);
  - closed circuit=mark
- Nonisolated contact sense
  - Open circuit=mark;
  - closed circuit=mark
- TTL
  - Plus level=mark;
  - minus level=mark
- EIA received data
  - Minus level=mark (standard convention) or
  - plus level=mark

The output options are:

- Solid state switch/TTL
  - Closed/minus=mark or
  - open/plus=mark
- EIA transmitted data
  - Minus=mark (standard convention)
- Current driver output
  - Current=mark;
  - no current=mark

Other output lines available are:

- EIA data terminal ready (on when ±12 volts installed)
- Solid-state switch/TTL write control
- Solid-state switch/TTL read control



Key:

TTL = transistor-transistor logic
EIA = Electronic Industries Association
SSS = solid state switch
IPL = initial program load

Figure 4-1. Block diagram of teletypewriter adapter feature

Data bytes are transmitted across the adapter/device interface serially by bit, with the least-significant bit being transmitted first. A 10- or 11-bit start/stop frame is used for synchronization of each byte. The bit rate is selectable on the card by jumper pins. If the device is programmed for one stop bit, a 10-bit start/stop frame is used; if the device is programmed for two stop bits, an 11-bit start/stop frame is used. The following bit rates are available:

Bits per second	
50	
75	
100	
110	
150	The interrupt mask time of the program support system used may preclude operation at these bit rates. See "Receive Operations" in this chapter for more details.
200	
300	
600	
1200	
2400	
4800	
9600	

The teletypewriter adapter feature is code transparent, and all 256 binary combinations can be transmitted and received. The teletypewriter adapter feature does not *transmit* break characters. *Received* break characters appear to the program support system as a series of all 0-characters followed by one unpredictable character. The data exchange over the interface is not checked for parity or device-dependent control characters. The adapter can be configured to perform initial program load (IPL).

Data transfer between the adapter and the processor is by byte, using direct program control (DPC) commands; however, during IPL, the transfer is by byte, using cycle-steal.

The teletypewriter adapter feature is packaged on a single circuit card that plugs into the backpanel of the processor or the I/O expansion unit. The backpanels on these units distribute the I/O channel signal lines to the I/O feature card sockets. Power is obtained from the backpanel through card connector pins except when ±12 volts is required, as explained in "Relationship to Other Features" in this chapter.

Relationship to Other Features

The communications power feature (#2010) furnishes ±12 volts and *is* a prerequisite for the teletypewriter adapter feature *if* the attached device is connected to either the nonisolated current loop interface or the EIA-voltage-level interface. The only exception is when the teletypewriter adapter is plugged into a 4953-A processor, where ±12 volts is standard on the backpanel.

The communications power feature is *not* a prerequisite for the teletypewriter adapter *if* the attached device is connected to either the isolated current loop interface or the TTL-voltage-level interface. When the attached device is connected to the isolated current loop interface, the user must supply power to drive the transmit and receive loops. When the attached device is connected to the TTL interface, normal logic levels presented on the teletypewriter adapter card are used to drive the transmit and receive loops.

The teletypewriter adapter card can be plugged into any I/O position that has +5 volts available at the card slot on the 4955 or 4953 card files or the I/O expansion unit card file. Refer to the prerequisite publications listed in the Preface of this manual.

The A-slot provides only +5 volts (no ±12 volts); therefore, the TTY card can be plugged into the A-slot only if the attached device is connected to either the TTL or isolated current loop interfaces.

Application Summary

The teletypewriter adapter is a device adapter designed to attach OEM devices that operate as start-stop devices in full-duplex mode over a four-wire interface (one pair of wires to transmit data, one pair of wires to receive data). Data can be transferred in current loop mode, or as either EIA or TTL signal levels.

The following is a list of different types of devices commercially available that can be attached to this interface:

- Printer-keyboards
- Keyboard-display
- Keyboard-display-printer
- Printers
- Tape cassettes
- Tape
- Card readers
- Badge readers
- Plotters

The preceding devices can be attached if the interrupt mask time of the program support system used does not preclude operation at the bit rate required by the attached device.

Operation at bit rates greater than 110 bps may not be achieved because of the interrupt mask time of the program support system used. Unbuffered devices whose inputs are from the keyboard, are generally less affected by the interrupt mask time of the program support system. See "Receive Operations" in this chapter for more details.

This interface offers signal and bit-rate selectability to accommodate a wide range of devices.

The input options are as follows:

Type/name	Data mark convention
Nonisolated contact sense	Closed circuit=mark;open circuit=mark
Isolated contact sense	Closed circuit=mark; open circuit=mark
TTL	Minus=mark; plus=mark
EIA received data	Minus (standard convention)=mark; plus=mark

These input options are selected by utilizing appropriate top-card connector pins and by jumper pins on the card. The output signals to the device are nonisolated solid-state switches, current drivers, and EIA drivers.

The output options are as follows:

Type/name	Data mark convention
Current driver	Current out=mark; no current out=mark
Solid-state switch/TTL	Closed/minus=mark; open/plus=mark
EIA transmitted data	Minus (standard convention)=mark
EIA data terminal ready	None (on when ±12 V installed)
	Usage
Solid-state switch/TTL write control	With Write command
Solid-state switch/TTL read control	With Read command

The write and read control outputs are available for device control of the user's hardware and are switched by modifier bit 7 of the Write and Read commands, respectively. These outputs are not used for any standard attachment of a teletypewriter I/O device.

Output options are selected by utilizing the appropriate top-card connector pins.

The teletypewriter adapter operates full-duplex. Data may be transmitted and received concurrently between the adapter and the device.

Selection of the Optimum Interface

This section discusses the advantages and disadvantages of using the following interfaces for attachment of an OEM device:

- Nonisolated current loop interface
- Isolated current loop interface
- EIA-voltage-level interface
- TTL-voltage-level interface

Most OEM devices that can be attached to the teletypewriter adapter card are manufactured with both a current loop interface and an EIA-voltage-level interface as switch-selectable options that are included in the basic price of the device.

Some devices are manufactured with (1) only the EIA interface, (2) only the current loop interface, or (3) one interface as standard and the other as an added cost feature.

Current loop mode also has more noise immunity than EIA or TTL voltage levels.

When most OEM devices are ordered with an EIA interface, they contain the full start-stop feature subset of the EIA interface:

- Transmit
- Receive
- Request to send
- Clear to send
- Data set ready
- Data terminal ready
- Carrier detect
- Signal ground

The only EIA-level signals that the teletypewriter adapter card generates are 'transmit,' 'receive,' 'signal ground,' and 'data terminal ready.' If the teletypewriter adapter is connected to an OEM device with the preceding signals:

- The 'transmit,' 'receive,' and 'signal ground' signals may be connected to the teletypewriter adapter card.
- The 'data terminal ready' signal from the teletypewriter adapter card must be connected to the 'data set ready' and the 'carrier detect' signals.
- The 'request to send' signal must be wired to the 'clear to send' signal at the device end of the cable between the teletypewriter adapter and the OEM device.

There are two different current loop interface "ports" available on the teletypewriter adapter card: one for isolated loops and one for nonisolated loops. The isolated current loop interface requires the user to supply power to drive the two isolated current loops. A separate power supply and current limiting resistor must be placed in the transmit loop and the receive loop. Refer to "Teletypewriter Device Information" *in this* chapter for connection of these power supplies and resistors.

The teletypewriter adapter supplies the power to drive the transmit and receive current loops when the nonisolated current loop interface is used. There are two other significant differences between the isolated and nonisolated current loop:

1. On the isolated current loop, the receive inputs are totally isolated. On the nonisolated current loop, the receive inputs are coupled through resistors to +12 volts and −12 volts generated by the card file power supply. For both isolated and nonisolated current loops, transmit minus is logical ground.
2. On the isolated current loop, the transmit output is a *current sink*. On the nonisolated current loop, the transmit output is a *current source*.

Figures 4-2 and 4-3 show details of the different interfaces available on the teletypewriter adapter card.

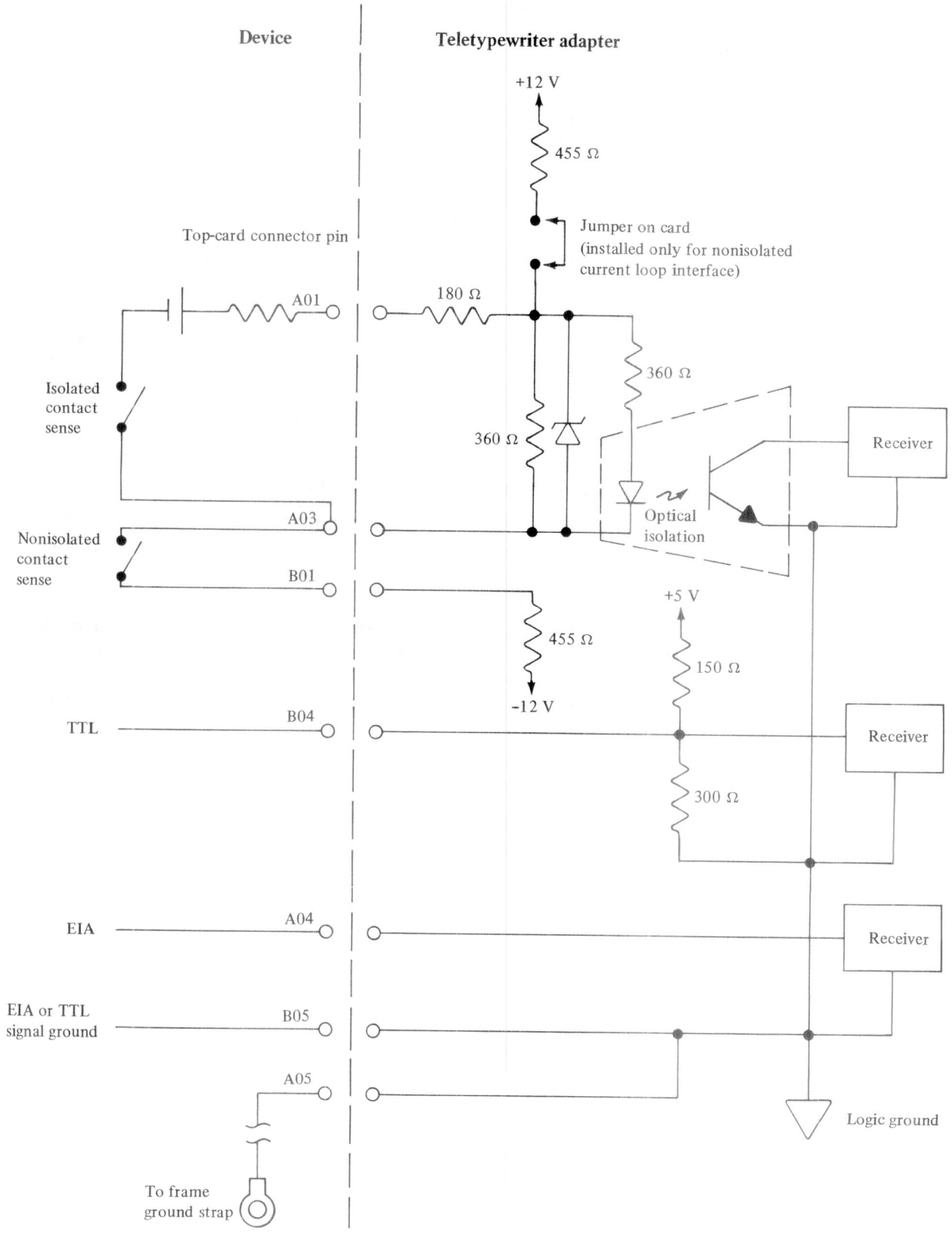


Figure 4-2. Input circuits

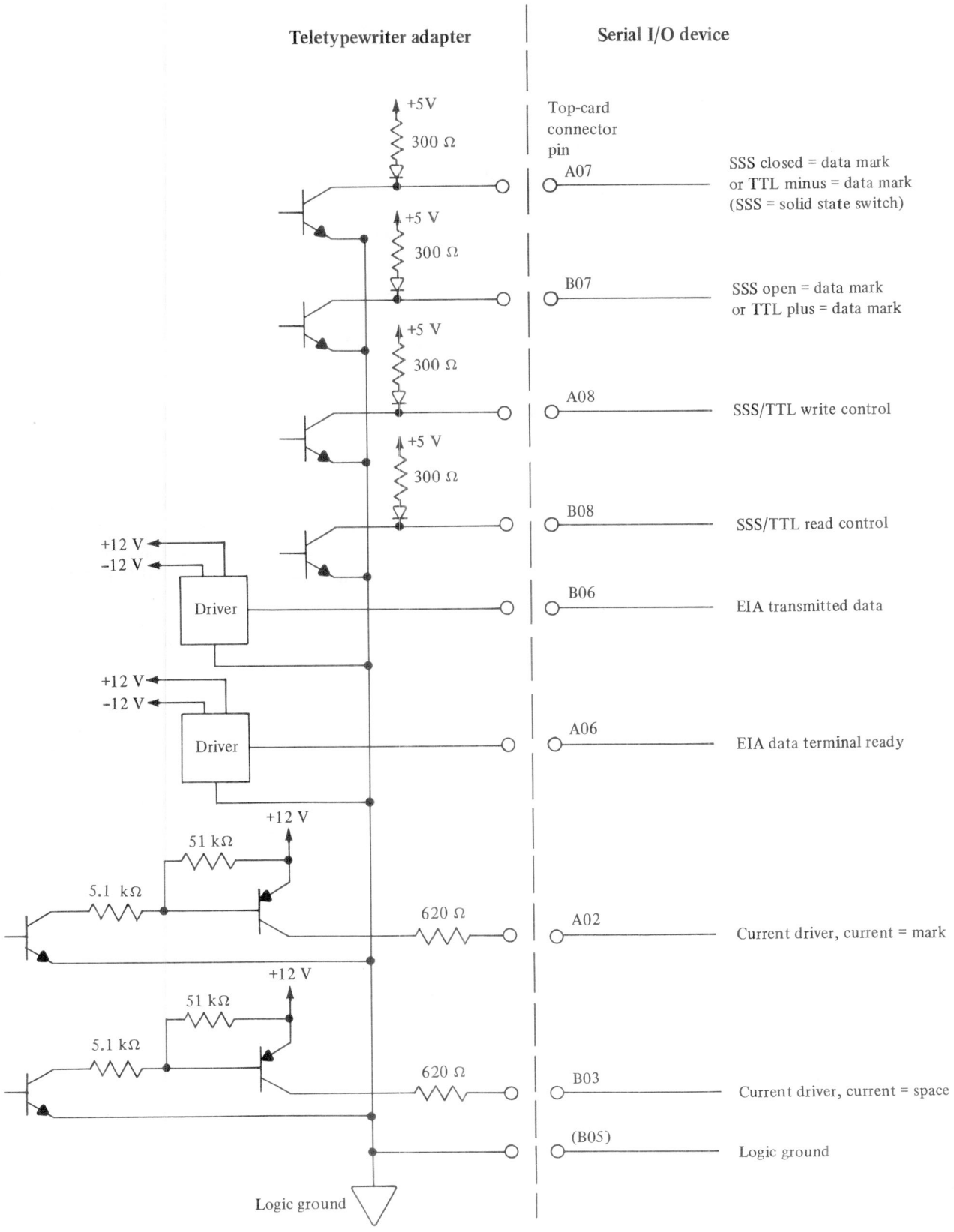


Figure 4-3. Output circuits

Generally, most users will elect to use either the EIA-voltage-level interface or the nonisolated current loop interface.

If a user is in doubt as to which interface to select, the EIA-voltage-level interface should be used.

If the user's environment is electrically noisy, the nonisolated current *loop* interface should be used.

The following table outlines the advantages and disadvantages of each of the four interfaces incorporated into the teletypewriter adapter card:

Interface	Advantages	Disadvantages
EIA voltage level	Customer does not have to purchase OEM power supplies to drive current loops	±12-volt power feature is a prerequisite for this interface
	Simple cabling from card to device	
	Most OEM devices support EIA interface	
Nonisolated current loop	Simple cabling from card to device	±12-volt power feature is a prerequisite for this interface
	High noise immunity	
	Customer does not have to purchase OEM power supply to drive current loops	OEM devices may not have a current loop position
Isolated current loop	High noise immunity	Customer must purchase two OEM power supplies to drive current loops
	±12-volt power feature not required	Customer must furnish cabling from the teletypewriter adapter to power supplies to attached device
		OEM devices may not have a current loop position
TTL voltage level	±12-volt power feature not required	Few OEM devices offer this interface
	Simple cabling from card to device	

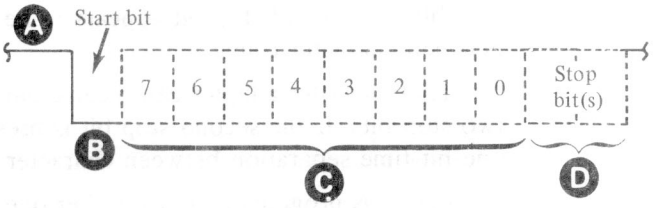
Data Transmission

Data is transmitted and received by the teletypewriter adapter serially by bit. Data is transferred one 8-bit character at a time. Each data character is preceded by one *start* bit and is followed by one or two *stop* bits. Characters being transmitted from the teletypewriter adapter to an OEM device are always followed by two stop bits. Characters being received by the teletypewriter adapter may have one or two stop bits. A start bit is always a *space* or logical 0, and a stop bit is always a *mark* or logical 1. The transmit and receive lines are always held in the mark state when no data is being transferred. Figure 4-4 shows the format of an 11-bit transmitted or received character frame.

Because the teletypewriter adapter is a full-duplex attachment, where data can be transmitted and received concurrently, OEM devices attached to the teletypewriter adapter should be configured for full-duplex operation.

No error checking is done on transmitted or received data. The teletypewriter adapter is code transparent. All 256 combinations of 8-bit characters can be transmitted or received.

It is not possible to overrun on data being transmitted by the teletypewriter adapter, but it is possible to overrun on data being received by the teletypewriter adapter. If a second character is received before the first character is serviced by the software, the first character *is not* lost, but the second character *is* lost.



A The line is always held in a mark condition when no data is being transmitted.

B The start bit is always a space (logical 0).

C Eight data bits are transmitted for each character. Each bit is either a mark or a space, depending on the character code. The least-significant bit is transmitted first.

D The stop bit is always a mark (logical 1). On transmit, two stop bits are always used; on receive, one or two stop bits can be used.

Figure 4-4. Format of an 11-bit transmitted or received character frame

Initial Program Load

The teletypewriter adapter provides initial program load (IPL) capability. A field-installable jumper on the card designates the teletypewriter adapter as the primary or alternate IPL source. If no jumper is installed, the teletypewriter adapter cannot perform IPL.

The IPL record length is 256 bytes, commencing at main storage location 0. The IPL data transfer starts when the adapter recognizes the first non-0 character from the attached OEM device.

The OEM device attached to the teletypewriter adapter must have some means of manually initiating a transmit operation to the teletypewriter adapter, if the OEM device is to be used for IPL.

This implies that the OEM device must be capable of *manually* initiating a read operation from some media (such as cards, tape, or disk) and transmitting the data to the teletypewriter adapter.

Teletypewriter Adapter Operational Characteristics

Data is always transmitted by the teletypewriter adapter in an 11-bit frame: one start bit, eight data bits, and two stop bits. At the beginning of the first stop bit, the teletypewriter adapter sends an interrupt request to the processor to signal the completion of the current character transmission. This interrupt must be serviced and another transmit operation initiated by the end of the second stop-bit time if maximum transmission rate is to be maintained.

Devices that are designed to receive either one or two stop bits may be attached to the teletypewriter card. If the device is designed for only one stop bit, the second stop bit appears to be a one-bit-time separation between character frames.

The teletypewriter adapter can receive data formatted with either one or two stop bits. If the second stop bit is present, it appears to be a one-bit-time separation between character frames.

If a device is programmable for either one or two stop bits, it should be programmed for one stop bit. This increases the receive data rate of the teletypewriter adapter by approximately 9 percent.

If a device is programmable for several different data rates that are supported by the teletypewriter adapter, the device should be programmed for the highest data transfer rate that results in reliable operation in the environment in which the system is placed.

Although the following information describes the internal operation of the teletypewriter adapter, it is presented here as necessary information to understand the subsequent transmit and receive timing charts.

Types of Receive Operations

Prior to presenting the following sections, it is important to distinguish between the two types of receive operations that the teletypewriter adapter performs:

- *A Normal Receive Operation*. This is a receive operation that results in the posting of an attention interrupt. No data characters are lost.
- *An Overrun Receive Operation*. This is a receive operation that results in the posting of an exception (overrun) interrupt. A second character was received and the leading edge of the first stop-bit time for this second character was detected before the first character was read by the program. The second character is lost. The first character is in the receive buffer register and can be read by executing an Operate I/O instruction with a Read command in the IDCB.

Interrupt Presentation

The teletypewriter adapter requests an interrupt (if it has been properly prepared) under the following conditions:

- When a normal receive operation is completed
- When an overrun receive operation is completed
- When a transmit operation is completed

Condition codes (CCs) reported at interrupt-acceptance time are as follows:

CC value	Meaning
2	Exception
3	Device end
4	Attention
6	Attention and exception
7	Attention and device end

The interrupt condition codes are subject to the following rules and considerations:

- The attention and exception codes are associated only with receive operations. The device-end code is associated with a transmit operation.
- The attention and exception codes are associated with operations initiated by the device. The device-end code is associated with operations initiated by the program.
- Attention and exception interrupts may be posted asynchronously to the device-end interrupt. Since interrupt-code presentation does not accommodate both exception and device-end codes during interrupt presentation, the exception code takes precedence over the device-end code at interrupt-presentation time if both interrupts have been posted. The presentation and acceptance of the exception code does not reset a pending device-end interrupt.

The meanings of the interrupt condition codes are as follows:

CC2 Indicates that the adapter has detected at least one overrun receive operation. A device-end interrupt may be pending, but the exception code has taken precedence in presentation.

CC3 Indicates completion of a transmit operation as a result of a Write command or indicates completion of an IPL operation. No exception interrupt has been posted at accept time.

CC4 Indicates completion of a normal receive operation.

CC6 Indicates that the adapter has completed a normal receive operation and has completed at least one overrun receive operation. A device-end interrupt may be pending, but the exception code has taken precedence in presentation.

CC7 Indicates that the conditions that cause CC3 and CC4 have occurred.

A detailed description of the differences among condition codes 2, 4, and 6 can be found in the IBM Series/1 processor description manuals. Refer to the Preface of this manual for titles and order numbers.

Commands That Initiate Receive and Transmit Operations

The teletypewriter adapter has two commands that must be described before presenting timing diagrams of transmit and receive operations: Read and Write.

Read

A character of data is received and deserialized in the receive serializer/deserializer (SERDES) register. After the last bit of the character has been clocked into the receive SERDES register, the character is moved to the receive buffer register.

A Read command transfers the contents of the receive buffer register to main storage.

In normal operation, an attention interrupt indicates to the processor that a data character has been received and is in the receive buffer register. A Read command is then executed as a part of the interrupt service program. The receive buffer register is then free to be used to hold another character.

If the receive control logic attempts to transfer a second received character into the receive buffer register before the first received character has been read from the receive buffer register by the program, an overrun occurs. The first character is still in the receive buffer register, and the second character is lost.

The program has one full *character* time to read the receive buffer register.

Write

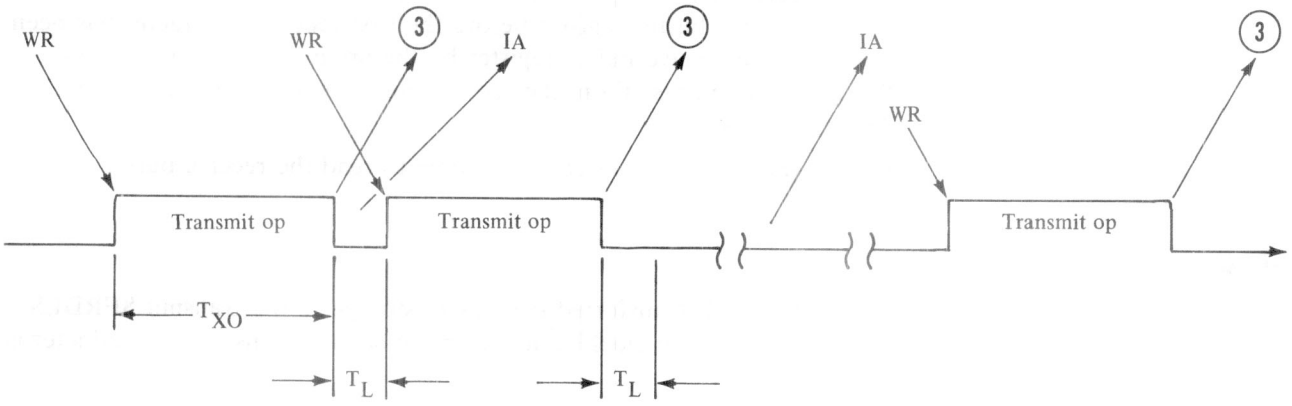
A byte of data is transferred from main storage to the transmit SERDES register; the internal clocking necessary to serially transmit the character is initiated.

At stop-bit time of the transmission of this character, a device-end interrupt signals the processor that character transmission is complete and that the adapter is available to accept another Write command.

Transmit Operations

Figure 4-5 is a timing diagram for transmit operations. T_{XO} is the transmit time from initiation of a transmit operation to posting of the device-end interrupt. T_{XO} is nine bit times at the selected bit rate. At 9600 bps (bits per second), $T_{XO)}$ is 0.936 ms; at 110 bps, T_{XO} is 81.9 ms. T_L is the transmit load time, measured from the posting of the device-end interrupt to the time at which the interrupt is accepted and another Write command can be issued to the adapter without loss of rated performance. T_L is two bit times at the selected bit rate. For 9600 bps, T_L is 0.208 ms; at 110 bps, it is 18.2 ms. If a new Write command is executed within time T_L, the character rate is determined by the adapter clocking; that is, a new transmit operation is not initiated in less than time T_L from the posting of the device-end interrupt. The adapter however, is "write-busy" upon successful execution of the Write command. If a new Write command is delayed beyond time T_L, the transmit operation is initiated immediately upon successful receipt of the Write command.

Note that the teletypewriter attachment always transmits two stop bits.



Baud rate	T_{XO} *(milliseconds)*	T_L *(milliseconds)*
9600	0.936	0.208
4800	1.87	0.416
2400	3.74	0.832
1200	7.49	1.66
600	14.98	3.33
300	29.96	6.66
200	44.94	10.0
150	59.9	13.3
110	81.9	18.2
100	89.88	20.0
75	119.08	26.6
50	179.76	40.0

T_{XO} and T_L are ±0.1%

Key:

(3) = post device-end interrupt (condition code 3)
IA = interrupt accept by processor
WR = Write command accepted

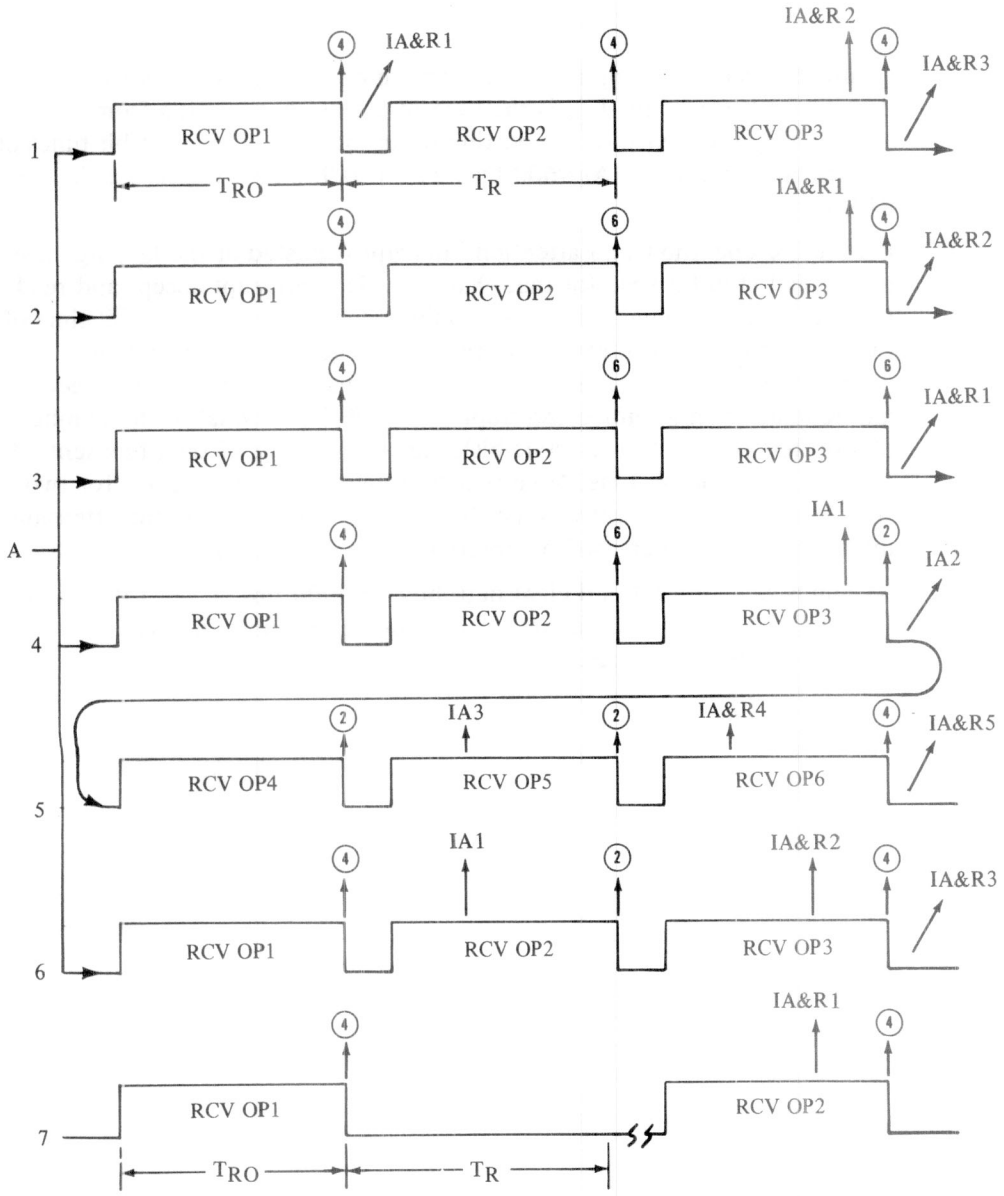
Figure 4-5. Transmit operation timing diagram

Receive Operations

Figure 4-6 depicts timing for receive operations. Timings are depicted at device-rated operation. T_{RO} is the time of a receive operation from initiation by the device to the posting of an interrupt. It is nine bit times at the selected frequency. At 9600 bps, T_{RO} = 0.936 ms; at 110 bps, T_{RO} = 81.9 ms.

On receive operations, an attention interrupt is posted at the leading edge of the first stop-bit time for that character. The interrupt accept and read (IA & R) must be done before the leading edge of the first stop bit time of the *next* character to prevent overrun. T_R is equal to the maximum permissible time the processor can delay in performing an interrupt accept and read after an attention interrupt is posted. T_R is equal to the number of stop bits sent, plus one (start bit), plus the number of data bits sent, all multiplied by one bit time. Note that by programming the device for two stop bits, T_R (the amount of time the program has to handle the attention interrupt) may be increased by approximately 10 percent.

Assuming one stop bit and eight data bits, at 9600 bps, T_R = 1.01 ms; at 110 bps, T_R = 90.8 ms. Figure 4-6 is a state and timing diagram of possible receive sequences.



Baud rate	T_{RO} *(milliseconds)**	T_R *(milliseconds) for one stop bit**	T_R *(milliseconds) for two stop bits**
9600	0.936	1.01	1.12
4800	1.87	2.05	2.26
2400	3.74	4.14	4.55
1200	7.49	8.30	9.14
600	14.98	16.6	18.3
300	29.96	33.3	36.6
200	44.94	49.9	54.9
150	59.9	66.6	73.3
110	81.9	90.8	99.9
100	89.9	99.9	109.9
75	119.1	133.3	146.6
50	179.8	199.9	219.9

**T_{RO} and T_R are ± 0.1%*

Key:

A = entry point
(2)(4)(6) = interrupt with circled condition code
IA = interrupt accept
IA&R = interrupt accept and execute read command
RCV OP = receive operation envelope

Figure 4-6. State and timing diagram for possible receive operations

The basic sequences on Figure 4-6 start from point A with a normal receive operation, and end with an attention interrupt being posted. Line 1 depicts interrupt acceptance and reading of the receive buffer register within time T_R. IA & R1 reads the character received in RCV OP 1, IA & R2 reads the character received in RCV OP 2, and IA & R3 reads the character received in RCV OP 3.

Line 2 depicts delay in interrupt accept and read beyond T_R. In this case, the character received in RCV OP 2 was lost and the data read by IA & R1 was the character received in RCV OP 1.

Line 3 depicts a delay of greater than two T_R times in taking an IA & R for RCV OP 3. In this case, the characters received in RCV OPS 2 and 3 were lost, and the data from RCV OP 1 was read by IA & R1.

Lines 4, 5, and 6 depict what occurs if the read is omitted from the interrupt accept. Lines 4 and 5 depict what occurs if an interrupt accept without read is taken after a condition code 6 (attention and exception) is posted. Note that the characters resulting from RCV OPS 2, 3, 4, and 5 were lost, and that the character read by IA & R4 was the character received in RCV OP 1.

Line 6 depicts what occurs if an interrupt accept without read is taken after a condition code 4 (attention) is taken. Note that the character resulting from RCV OP 2 was lost. IA & R2 read the character resulting from RCV OP 1.

If T_R has been exceeded, no overrun occurs *unless* the first stop-bit time of another character is detected by the attachment before the IA & R occurs to clear the interrupt and read the first character; line 7 is an example of this. Even though IA & R1 did not occur until after T_R, no overrun occurred because the first character was read by IA & R1 before the leading edge of the stop-bit time of the next character.

Unbuffered devices whose input is from the keyboard can generally tolerate a much longer interrupt mask time than the value of T_R listed in Figure 4-6 because it is the device *character* rate that determines how long an interrupt mask time can be tolerated. An unbuffered device may be operating at 9600 bps, but the *character* rate is determined by how rapidly an operator can press keys.

If an operator is entering data on an unbuffered terminal that is configured for 9600 bps, the *bit rate* of any given character is 9600 bps, but the *character rate* is probably 15 characters per second or less. The instantaneous maximum character rate that can be caused by a person keying in data is 30 characters per second.

For a device to be considered unbuffered, it must be determined that there is no possible sequence in which the device could transmit two or more consecutive characters at an instantaneous character rate that exceeds 30 characters per second.

Any device that sends a multiple character burst of data for the pressing of any single key (for example, "here is" key) must be considered a buffered device. Any device that has a multiple byte status that can be read by the program must be considered buffered.

Read Control and Write Control

'Read control' and 'write control' are two general purpose outputs of the teletypewriter adapter. These outputs are not used for any standard attachment of a teletypewriter I/O device. The 'read control' and 'write control' outputs are provided for whatever use the customer can find for them. These two outputs are solid-state-switch outputs and have two states: open and closed.

Read Control

A Read command has the following format:

Bits 0–3	Bits 4–7
0001	000X

Bit 7 of a Read command controls the 'read control' output. If a Read command is issued with bit 7=1, the 'read control' output closes and remains closed until either (1) a Read command is issued with bit 7=0 or (2) the attachment is reset.

If a Read command is issued with bit 7=0, the 'read control' output opens and remains open until a Read command is issued with bit 7=1.

Any system reset or device reset causes the 'read control' output to open and remain open until a Read command is issued with bit 7=1.

A Read command can change the state of the 'read control' output only if the Operate I/O (IO) condition code response to the command is condition code 7 (command accepted).

A Read command *cannot* change the state of the 'read control' output if the IO condition code response to the command is condition code 0 (device not attached), 1 (read busy), or 3 (command reject). The teletypewriter attachment does not use condition code 2, 4, or 6; IO condition code 5 is not used on a Read command.

Read Control Timing. A system reset or device reset can cause the 'read control' output to open asynchronously to the receiving of characters.

Under normal operation, receive interrupts are taken after the leading edge of the stop bit for any given character, and before the leading edge of the start bit of the next character. The Read command is part of the receive interrupt sequence; therefore, the 'read control' output normally switches state only in the time window that starts with the leading edge of the stop bit of one character and ends with the leading edge of the start bit of the next character.

If an overrun occurs, this time window can extend through one or more overrun receive operations until a Read command is executed.

Write Control

A Write command has the following format:

Bits 0–3	Bits 4–7
0101	000X

Bit 7 of a Write command controls the 'write control' output. If a Write command is issued with bit 7=1, the 'write control' output closes and remains closed until either (1) a Write command is issued with bit 7=0, or (2) the attachment is reset.

If a Write command is issued with bit 7=0, the 'write control' output opens and remains open until a Write command is issued with bit 7=1.

Any system reset or device reset causes the 'write control' output to open and remain open until a Write command is issued with bit 7=1.

A Write command can change the state of the 'write control' output only if the IO condition code response to the command is condition code 7 (command accepted).

A Write command *cannot* change the state of the 'write control' output if the IO condition code response to the command is condition code 0 (device not attached), 1 (write busy), 3 (command reject), or 5 (interface data check). The teletypewriter attachment does not use IO condition code 2, 4, or 6.

Write Control Timing. The 'write control' output can change state only during the first 0.2 microsecond of the start bit of a transmit operation. It is opened by a system reset or device reset.

System-Related Characteristics

Power Failure

Any character that is in the process of being either transmitted or received during a power failure is either lost or garbled.

'Power-on reset' is generated when the system is powered back up. This signal resets all controls and registers in the teletypewriter adapter except for the receive serializer/deserializer register. This register is set to all 1's. (This is equivalent to the ASCII "rub out" character.)

Error Recovery

There is no checking of any kind between the teletypewriter adapter and the user's device.

Teletypewriter Adapter Electrical Characteristics

CAUTION: Refer to the engineering machine logic diagrams (MLDs) for positive cable connector-pin designations.

Teletypewriter Adapter Communications Lines

The teletypewriter adapter offers two current-loop interfaces (or "ports") and two voltage-level interfaces for connecting to user's devices:

- Isolated current loop
- Nonisolated current loop
- EIA voltage level
- TTL voltage level

The teletypewriter adapter provides a 16-pin (2 x 8) top-card connector for connecting the user's device.

A separate pin or pair of pins on the top-card connector provides the inputs and outputs for the four different interfaces.

Input Circuits General Description

Figure 4-2 shows the four basic types of receive inputs: isolated contact sense, nonisolated contact sense, TTL, and EIA RS232-C voltage level.

Input options are selected:

- By connecting to the appropriate pins, and
- By a 3-bit, coded jumper-pin selection on the card. See "Jumper Selections" in this section for a detailed explanation of jumpering.

Isolated Contact Sense. Two connector pins are available for the signal input. The isolated common may be strapped to signal ground on the user's connector, if desired in certain applications. When the isolated contact sense input is used, some external non-IBM supplied power source must be used to generate current for the receive current loop.

The equivalent circuit for the TTY-attachment card isolated contact sense inputs is a series resistance between the input pins.

Nonisolated Contact Sense. Two connector pins are available for the signal input. These inputs are used when it is desired that the teletypewriter adapter card generate current for the receive current loop.

The equivalent circuit for the TTY-attachment card nonisolated contact sense inputs is a resistor in series with a voltage source.

TTL. One connector pin is available for TTL-level input. The TTL input is nonisolated.

EIA. One pin is available for EIA RS232-C level input. This input is nonisolated.

Grounding. The cable shielded-ground wire must be connected to *frame ground* at the point of entry into the IBM enclosure and at the user's device end of the cable.

Because the performance of this interface may be affected by noise, appropriate arc suppression, noise filtering, etc., may be necessary on customer inputs.

Contact sense inputs are isolated from card ground. TTL and EIA signal grounds are tied to logic ground in the teletypewriter adapter card.

Output Circuits General Description

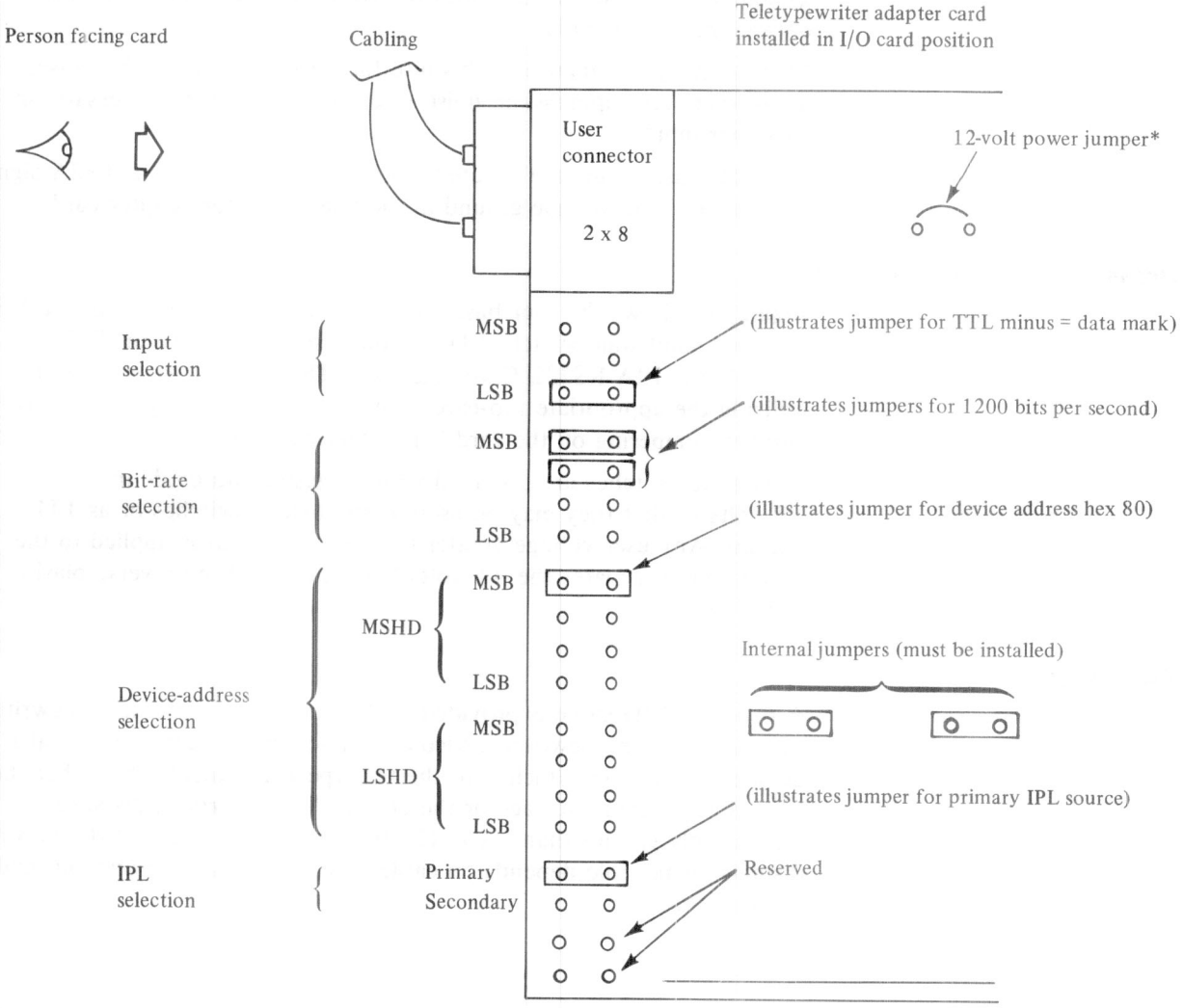
Figure 4-3 shows the four basic types of outputs available: current driver for data, solid-state switch/TTL for data, solid-state switch/TTL for control, and EIA RS232-C voltage level. The outputs are selected by utilizing the appropriate top-card connector pins. All outputs are driven in parallel; jumpering on the card is not necessary for selecting an output.

Solid-state switches are provided with a resistor and diode in series tied to +5 volts so that they may be used as solid-state switches or as TTL outputs. Any user voltage greater than +5 volts that is applied to the switch output isolates the +5 volts from the switch by reverse biasing the series diode.

Cable Length

A 6.1-m (20-ft) cable is provided by IBM to connect the teletypewriter adapter to a teletypewriter device or a functionally equivalent serial I/O device. For devices attached to the teletypewriter adapter by either the EIA-voltage-level interface or the current loop interface, distances significantly greater than 6.1 m (20 ft) can be achieved, but the maximum distance achievable depends on cable type, electrical environment, and device data rate.

Figure 4-7 shows the card jumper selections for the teletypewriter adapter. All card jumper pins are located in-line near the output edge of the installed card so that they can be read while the card is installed in an I/O card slot.



Key:

MSB	=	most-significant bit
LSB	=	least-significant bit
MSHD	=	most-significant hexadecimal digit
LSHD	=	least-significant hexadecimal digit

Figure 4-7. Jumper selections

Generally, the most-significant bit of the selection is the highest of a group. Four groups are provided. From top to bottom, facing the installed card, they are:

- Input selection, binary coded, most-significant bit to least-significant bit (3).
- Bit-rate selection, binary coded, most-significant bit to least-significant bit (4).
- Device address, most-significant hex digit (4) and least-significant hex digit (4).
- IPL selections, primary and secondary (2).
- Reserved (2).

Jumper significance is as follows:

- Input selection—jumper installed means that the appropriate bit of the decode = logical 1. The decode is as follows:

MSB		LSB	Input selected	Input interpretation
0	0	0	Contact sense	Closed=data mark*
0	0	1	TTL	Minus=data mark
0	1	0	EIA	Minus=data mark
0	1	1	Internal	True data out
1	0	0	Contact sense	Open=data mark
1	0	1	TTL	Plus=data mark
1	1	0	EIA	Plus=data mark
1	1	1	Internal	True data out

*The contact sense input, closed=data mark, is the no-jumper default selection.

- Bit-rate selection—jumper installed means that the appropriate bit of the decode = logical 1. The decode is as follows:

MSB			LSB	Input interpretation
0	0	0	0	110 bps*
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	50 bps
0	1	0	1	100 bps
0	1	1	0	200 bps
0	1	1	1	Reserved
1	0	0	0	75 bps
1	0	0	1	150 bps
1	0	1	0	300 bps
1	0	1	1	600 bps
1	1	0	0	1200 bps
1	1	0	1	2400 bps
1	1	1	0	4800 bps
1	1	1	1	9600 bps

*110 bps is the no-jumper default bit-rate selection.

- Device address—jumper installed means that corresponding device address bit = logical 1.
- IPL—jumper installed means "selected." If no jumpers are installed, the teletypewriter adapter cannot perform IPL.

Inputs

Isolated Contact Sense. The user's equipment must supply a current of 20 mA to the isolated contact sense inputs. This results in a voltage of between +9.0 and +16.7 volts placed across the receive input terminals. For a mask condition, the attached device must generate a current of 14 mA or greater. For a space, the device current must be less than 250 μA.

Nonisolated Contact Sense. The teletypewriter adapter can supply a current of 20 mA to drive the receive current loop. The OEM driving source for the receive inputs should be a passive device that can be approximated by a resistor and a switch in series.

When the driving source switch is "open," no current flows, and the potential across the receive inputs is +24 volts $\pm$10%.

When the driving source switch is "closed," a current flows out of the receive plus input and back into the receive minus input. The current flow is I = 18.5 V/(910+R) where I=amperes, V=volts and R=ohms, and where R is the impedance of the OEM driving source. R must be 400 ohms or less for reliable operation. For a mask condition, the attached device must generate a current of 14 mA or greater. For a space, the device current must be less than 250 μA.

EIA. The EIA 'receive data' signal input must conform to EIA RS232-C/CCITT V.24 specifications. The input impedance of the 'receive data' signal is 3 kilohms to 7 kilohms. This signal drives an SN75154 (or equivalent) TTL receiver.

TTL. The TTL 'receive data' signal must be a TTL-compatible signal. The input impedance of the TTL 'receive data' signal is 100 ohms. This signal drives an SN75154 (or equivalent) TTL receiver, and draws 40 mA of current.

Outputs

Current Driver (No Customer Supply Required). The teletypewriter adapter card provides a current driver for transmit output. The current driver provides the current to drive the transmit loop. No external power supply is required if this current driver output is used to drive the OEM device receive input.

When the current driver is "on," a maximum current of 20 mA out of the teletypewriter adapter card is generated. The voltage across the transmit output pins when the current driver is on is:

V_{to} = I to R, where the exact current flowing is

$$I_{to} = \frac{12\ V}{620+R}$$

R is the impedance looking into the OEM device receive input pins. For reliable operation, R should be less than 200 ohms.

When the circuit driver is off, the maximum current out of the transmit output is 500 μA and the voltage across the transmit output pins is V_{to} = 0.0005 R.

Solid-State Switch (With Series Customer Supply). The teletypewriter adapter transmit output is a solid-state switch. In the open or off-state, the maximum voltage the switch can withstand is 52.8 volts. With this voltage, the maximum current through the switch is 500 μA or less.

In the closed or on-state, the maximum permissible current through the switch is 100 mA. The voltage drop across the switch in the closed or on-state must be less than 0.08 volt.

Solid-State Switch/TTL (Without Series Customer Supply). In the open or off-state, the maximum output voltage is 5.5 volts at 50 μA; the minimum output voltage is 2.4 volts at 1 mA.

In the closed or on-state, the maximum output voltage is 0.8 volt; the minimum output voltage is 0.0 volt.

EIA. The EIA outputs must conform to EIA RS232-C/CCITT V.24 specifications. The output driver is an SN74150 TTL driver.

If the $\pm$12-volt supply is not installed, the 'EIA transmitted data' signal and the 'EIA data terminal ready' signal are in the power-off condition. For attached devices using the EIA input for receive-only operations, the $\pm$12-volt supply option is not required. In this case, the 'EIA data terminal ready' signal generated by the attached device should be wrapped back to the input that would normally be connected to the 'data terminal ready' output of the teletypewriter adapter.

Baud-Rate Tolerance

The worst-case baud-rate (bit-time) tolerances for all attached devices must be less than ±2.0%.

Since bit-time tolerances are normally cumulative, this means that the tenth bit (the stop bit) may occur anywhere from 20% early to 20% late.

Data Rise and Fall Times

Current loop—the rise time of a bit (defined as the time to switch from 1 mA to 12 mA) must be less than 3% of one bit time. The fall time (the time to switch from 12 mA to 1 mA) must also be less than 3% of one bit time.

TTL—the rise time of a bit (defined as the time to switch from 0.45 to 2.40 volts) must be less than 3% of one bit time. The fall time (time to switch from 2.40 to 0.45 volt) must also be less than 3% of one bit time.

EIA—the data rise and fall times must conform to EIA RS232-C/CCITT V.24 specifications.

Power Supplies

The teletypewriter adapter does not require any external power supplies. All power required by the teletypewriter adapter is obtained from the I/O card file in which the card is inserted.

The only exception to this is when the user elects to attach the device to the isolated current loop interface. In this case, the user must supply a 25-volt (100-mA) power supply and a current-limiting resistor for both the transmit and the receive loops.

The value of the series resistor must limit the current in each loop to 20 mA. Figure 4-8 shows the current loop connections.

Connections for current loop when the user supplies current

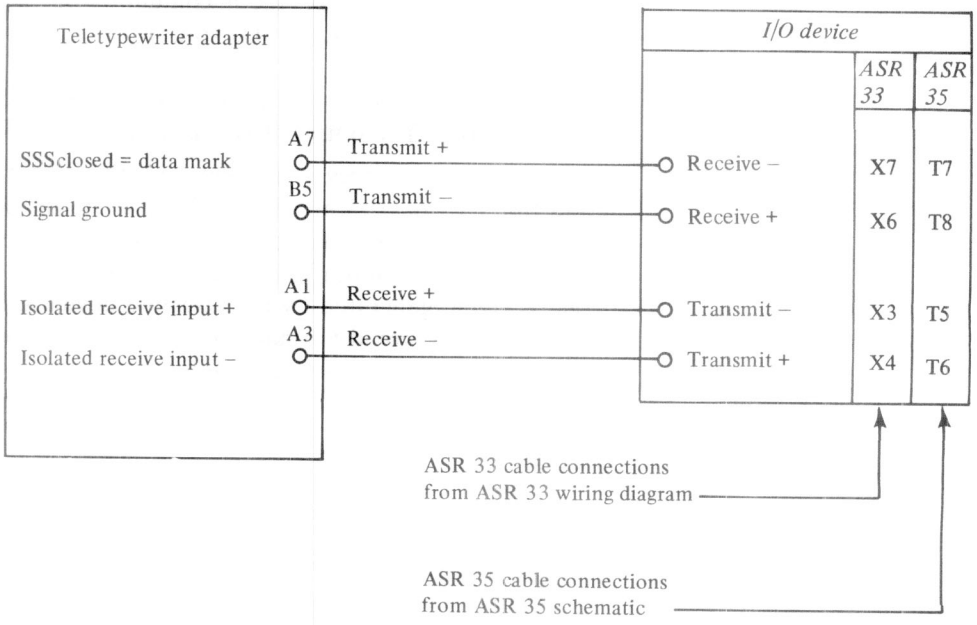


Figure 4-8. Connections for current loop when the user supplies current for the loop

Teletypewriter Adapter Physical Characteristics

Physical Description

The teletypewriter adapter is a standard IBM printed circuit card with two signal planes. (For an illustration of the card, see "I/O Channel Physical Components Description" in Chapter 2.) Four connectors on the card plug into a backpanel board that distributes the processor I/O channel signal lines. There is a 16-pin (2 x 8) connector at the top of the card for device inputs and outputs.

The cable that plugs into this connector should be made with #24 AWG wire, and must use Berg part number 75598-003 pins (or equivalent) and a Berg part number 65405-005 housing (or equivalent).

Signal Pin Assignments

Figure 4-9 shows the cable connections for the teletypewriter adapter card. The following table is a list of the signals and their pin assignments:

Pin	Signal	Pin	Signal
A1	Isolated receive input+	B1	Nonisolated receive input-
A2	Current driver, current =mark	B2	(Polarizing pin)
A3	Isolated receive input- or nonisolated receive input+	B3	Current driver, current= space
A4	EIA received data in	B4	TTL received data in
A5	Frame ground	B5	Signal ground
A6	EIA data terminal ready	B6	EIA transmitted data
A7	SSS closed=data mark or -TTL data out	B7	SSS open=data mark or +TTL data out
A8	SSS/TTL write control	B8	SSS/TTL read control

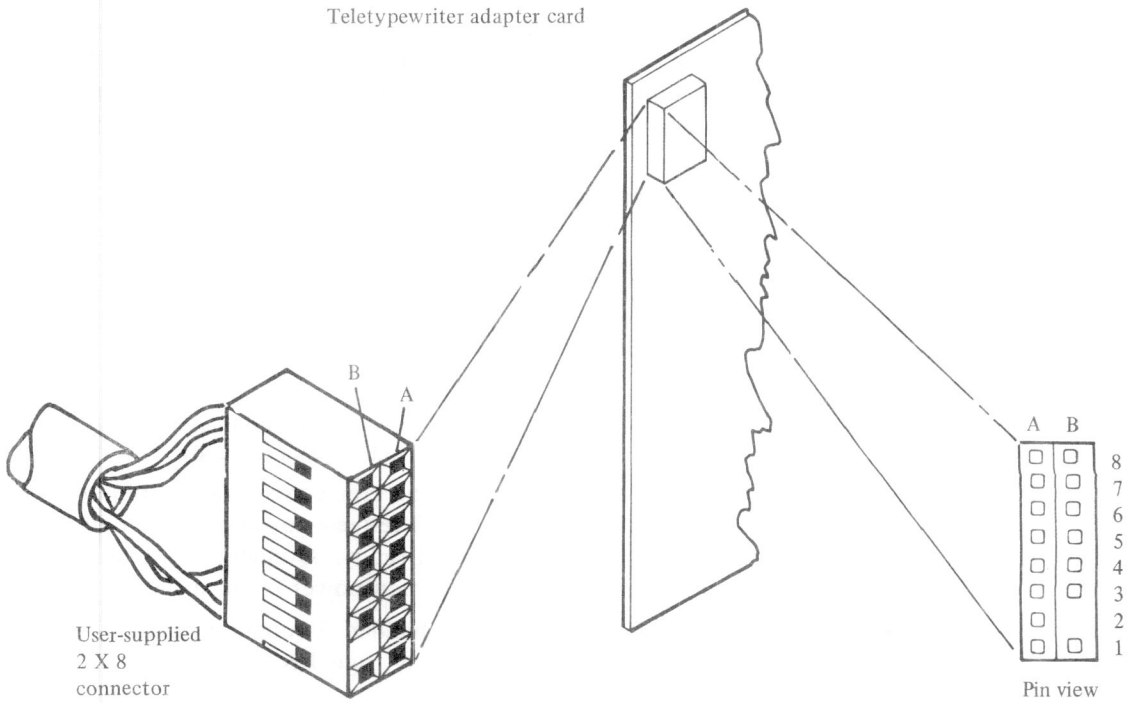


Figure 4-9. Cable connections for the teletypewriter adapter card

Teletypewriter Adapter Design Considerations

Teletypewriter Device Information

The teletypewriter should be configured for full-duplex operation and a 20-mA current loop prior to installation. Teletype* Models ASR 33, ASR 35, or KSR 33 are normally shipped from the factory wired for half-duplex, 60 mA, and even parity.

Either the isolated contact sense input or the nonisolated contact sense input, with input selection code equal to all 0's, must be used for connection of the ASR 33/35.

Either the current driver (current=mark output) or the solid-state switch (closed=data mark output) must be used for the ASR 33/35.

If the system is powered down, the output driver goes to a data space condition, causing the device to "chatter" if it is in "line mode." Consequently, the ASR 33/35 should be turned off or put in "local mode" if the system is powered down. However, no damage to the device results if it is left in line mode, just unnecessary wear.

Also, if the cable is disconnected while the ASR 33/35 is in line mode, the device can chatter.

During an IPL operation, the ASR 33/35 should be placed in line mode prior to pressing the Load key on the processor console.

Cable Connection to the Teletypewriter Adapter

The tables in the following sections indicate how pins on the top-card connector should be connected to pins on the attached device.

EIA

The communications power supply feature furnishes ±12 volts. This feature is a prerequisite for any card file (except the 4953-A processor) in which the teletypewriter (TTY) adapter is installed if the adapter sends EIA output levels to the device. However, the 12-volt supply is not required to only receive EIA levels. The connections for EIA are as follows:

Series/1 TTY card connector	Device connector
A4 EIA received data in	EIA transmitted data
A6 Data terminal ready	Received line signal detector
B5 Signal ground	Signal ground
B6 EIA transmitted data	EIA received data—connect request-to-send to clear-to-send; connect data terminal ready to data set ready

Note that two different wrap connectors may be required at the customer device cable connector: (1) request-to-send to clear-to-send, and (2) 'data terminal ready' to 'data set ready.' Connector pin A6 is 'EIA data terminal ready,' and is a logical 1 when power is on in the teletypewriter adapter.

This interface requires a shielded 3-conductor cable; 4-conductor cable if the 'EIA data terminal ready' signal is used.

---

*Trademark of the Teletype Corporation

TTL

The connections for TTL are as follows:

Series/1 TTY card connector	Device connector
B4 TTL received data	TTL transmitted data
B5 Signal Ground	Signal ground
Either	
A7 SSS closed=data mark or -TTL data out	
	TTL received data
B7 SSS open=data mark or +TTL data out	

Wire the cable to either pin A7 or pin B7, depending on which polarity is required by the attached device for received data.

The interface requires a shielded, 3-conductor cable.

Current Loop With User's Power Supplies

Connections for this current loop are as follows:

Series/1 TTY card connector	Device connector
A1 Isolated receive input+	Transmit –
A3 Isolated receive input–	Transmit +
B5 Signal ground (transmit–)	Receive +
A7 SSS closed=data mark	Receive –

Two external power supplies are required for the current loop interface: one for the transmit loop and one for the receive loop. Both power supplies must generate 25-volt power and must supply a current of up to 100 mA.

The two external power supplies must be placed in series with the transmit and receive loops with the polarities as shown here. The power supplies should be placed at the device end of the cable.

Figure 4-8 is a diagram for the cable connections described (that is, when the customer elects to use external power supplies, solid-state switch teletypewriter adapter outputs, and isolated receive inputs).

Note: For this configuration, the jumper wire that ties +12 volts into the receiver logic should *not* be used (refer to Figures 4-2 and 4-7).

Current Loop Without User's Power Supplies

The teletypewriter adapter card generates the current for the transmit and receive loops. The following table shows connections at the card, the customer access panel (CAP), and the device:

Series/1 TTY card connector	**CAP pin**	**Device connector**
B1 Nonisolated contact in –	3	Transmit –
A3 Nonisolated contact in +	4	Transmit +
B5 Signal ground (transmit –)	1	Receive –
A2 Current driver, current=mark	2	Receive +

No external power supplies are required in this configuration. Current for the transmit and receive current loops is supplied by the teletypewriter adapter card. The teletypewriter adapter card to OEM device cable for this configuration is a straight cable without any series power supplies (Figure 4-10).

In this configuration, the transmit and receive loops are not isolated, because both loops are driven with voltages referenced to logic ground. This configuration puts 12 volts across the receive input and 24 volts across the transmit output of the attached device. Teletype Models ASR 33, ASR 35, and KSR 33 require 24 volts across their transmit outputs for reliable operation.

For devices that require only 12 volts across their transmit outputs, pin B05 should be used instead of B01 at the connector on the teletypewriter adapter card.

Note: The 12-volt power jumper on the teletypewriter adapter card must be installed for this configuration (refer to Figures 4-2 and 4-7).

Connections for current loop when teletypewriter adapter supplies current

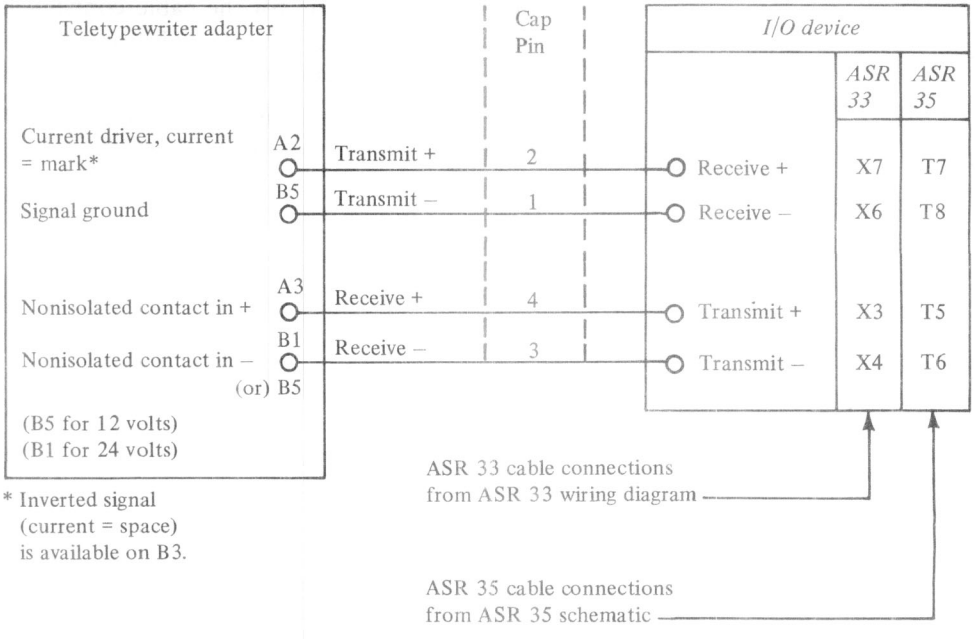


Figure 4-10. Connections for current loop when the teletypewriter adapter supplies current for the loop

Customer Access Panel (CAP) Connections

If the customer access panel (CAP) feature (#1590) is ordered, the cable from the card connector to the CAP is built-in, and the teletypewriter customer access cable feature (#2059) provides the cable from the CAP to the device. If the CAP feature is not ordered, the teletypewriter cable feature (#2055) provides direct cabling from the card connector to the device.

Chapter 5. Integrated Digital Input/Output Feature

Introduction

The integrated digital I/O nonisolated feature allows the user to add digital sensor I/O or non-IBM devices. This feature has the following general characteristics:

- Two 16-point groups of nonisolated digital input/process interrupt (DI/PI).
- Two 16-point groups of nonisolated digital output (DO).
- Four device addresses, one for each DI/PI or DO group. All four devices prepared for interrupts with one Prepare command.
- External synchronization for each group of DI and DO. This user-attachment feature permits asynchronous data transfers.
- Interrupts can be initiated by an external sync input (one input for each DI or DO group) or by a 0-to-1 transition on a PI point.
- The feature is contained on one logic card and can be plugged into either the processor unit or the IBM 4959 I/O Expansion Unit.

Figure 5-1 is a simplified data flow of the integrated digital I/O feature.

Digital Input (DI)

The integrated digital I/O feature has two groups of digital input/process interrupt. Each group of digital input has:

- User-input points (16) that sense the value of nonisolated voltage input.
- One 16-position DI data register for reading unlatched data.
- One 16-position PI data register for reading latched data.
- An 'external sync' input line and a 'ready' output line.
- Interrupt capability from either external sync or process interrupt.

Each digital input group has a unique device address and responds to specific commands. A description of addressing and commands can be found in the IBM Series/1 processor description manual. Refer to the Preface of this manual for the titles and order numbers. The data registers and the functions performed by DI/PI are described in this section.

Each position of the DI data register follows the state of the corresponding user-input point until the register is read. The data in the register is held, either during a Read command or when the 'external sync' input becomes active while in external sync mode. In the second case, the data remains held until the resulting interrupt is serviced and the 'ready' line is activated. For additional information, see "DI External Sync" in this section.

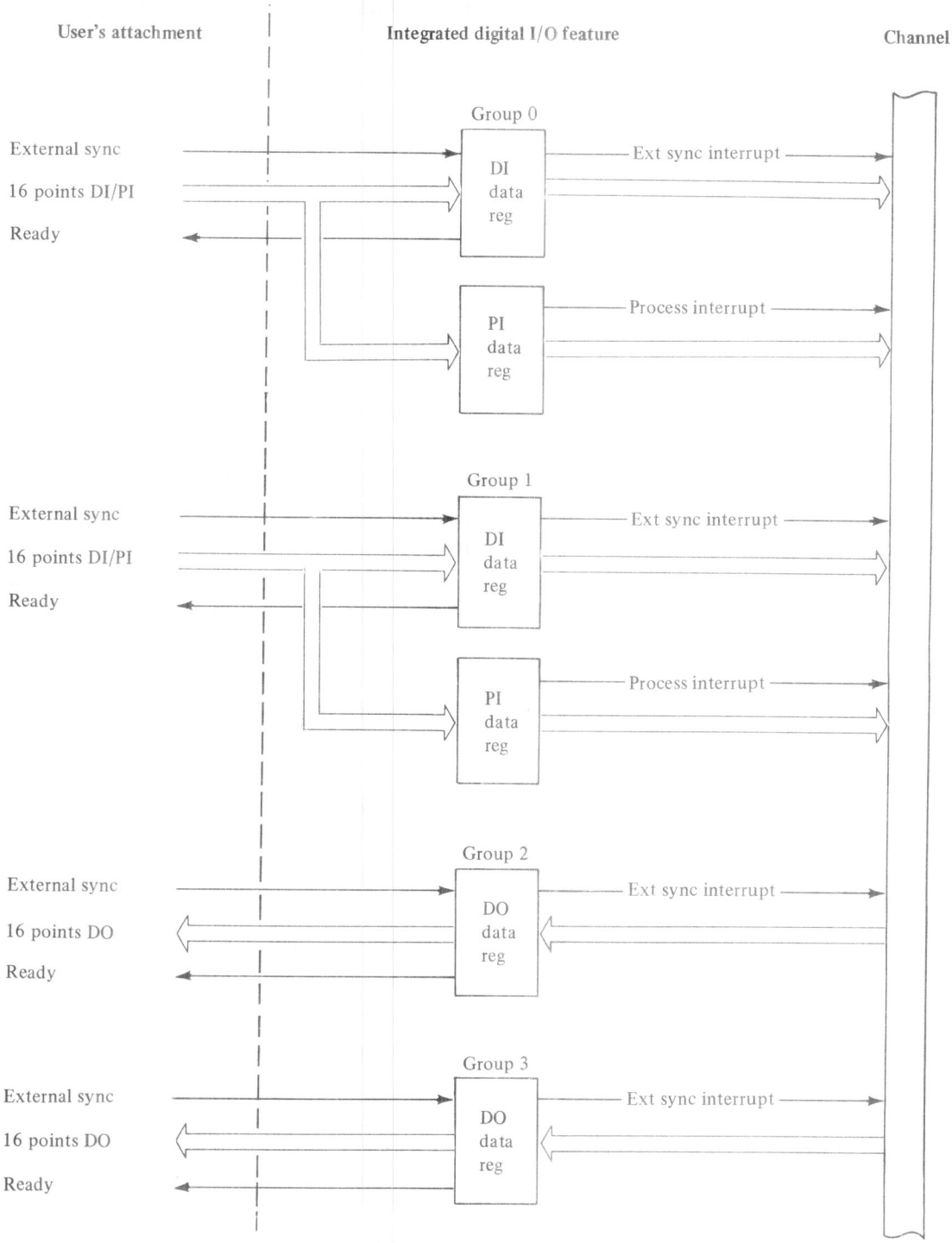


Figure 5-1. Digital I/O feature—simplified data flow

Each position of the PI data register records, with a 1-bit, the first 0-bit to 1-bit transition on the corresponding user-input point. The data in the register remains until it is reset by one of the following:

- Read PI With Reset command
- Arm PI command
- Device Reset command
- System reset
- Power-on reset

When a bit in the PI data register becomes active, a process interrupt is generated if PI mode was previously set with an Arm PI command. For additional information, see "Process Interrupt Mode" under "Digital Input Operation" in this chapter.

A DI/PI group can be tested using two special commands: Set Test Ones and Set Test Zeros. When the appropriate command is executed, the user inputs and outputs are disabled, either 1's or 0's are placed on the input receivers, and the external sync receiver is pulsed. Then, when subsequent Read commands are issued, the group responds exactly as if the actual user inputs, including the PI and external sync functions, had been set.

DI External Sync

DI external sync consists of two signal lines: an 'external sync' input line and a 'ready' output line. A DI group is set to external sync mode by execution of the Arm DI External Sync command. When external sync mode is armed and the system is ready for more DI data, the 'ready' line from the DI group is set active. The user places data on the input points, and then activates the 'external sync' line. When 'external sync' becomes active, the data in the DI data register is assumed to be good and the contents of the register are held. An interrupt is then posted; the 'ready' line becomes inactive and stays inactive until the appropriate command, normally Read DI, is executed. The 'external sync' line must then perform another transition from the 0 to the 1 state to cause another interrupt.

External sync mode is reset by an Arm PI command, a Device Reset command, a Halt I/O command, or any reset condition.

Process Interrupt (PI)

A digital input group is set to PI mode by the Arm PI command. The process interrupt function is performed by logically ORing the bits in the PI data register of the DI group. Any PI register bit that becomes active generates an interrupt.

PI mode is reset by an Arm External Sync command, a Device Reset command, a Halt I/O command, or any reset condition.

Digital Output (DO)

The integrated digital I/O feature has two groups of digital output. Each DO group has:

- User-output points (16). Each point provides a nonisolated, solid-state current switch or TTL (transistor-transistor logic) compatible output voltage.
- One 16-position DO data register.
- An 'external sync' input line and a 'ready' output line.
- Interrupt capability from the 'external sync' input line.

Each digital output group has a unique device address and responds to specific commands. Data is stored into the DO data register by the Write DO command. The DO data register is reset only by a power-on reset.

A DO group can be tested using three special commands: Disable DO, Read DO, and Set Diagnostic External Sync. The Disable DO command disables the user outputs. The Read DO command reads the contents of the DO data register. The Set Diagnostic External Sync command disables the user outputs and simulates the user's 'external sync' line.

DO External Sync

DO external sync consists of two signal lines: an 'external sync' input line and a 'ready' output line. A DO group is set to external sync mode by execution of the Arm DO External Sync command. When a Write DO command is executed in external sync mode and the data on the DO output is good, an active level on the 'external sync' input line causes the 'ready' line to become active. The user signifies receipt of the data by deactivating the 'external sync' line. An interrupt is then posted and the 'ready' line becomes inactive. The 'ready' line stays inactive until another Write DO command is executed and 'external sync' becomes active again. The 'external sync' line must perform another transition from the 1-state to the 0-state to cause another interrupt.

External sync mode is reset by a Device Reset command, a Halt I/O command, or any reset condition.

Integrated Digital I/O Operational Characteristics

The timing charts in this section show a logical 1 as a down level (typically 0 Vdc), and a logical 0 as an up level (typically +5 Vdc).

Digital Output Operation

Each DO group can operate in one of three modes: non-interrupting, external sync, and diagnostic.

Non-Interrupting Mode

When operating in the non-interrupting mode, each 16-point DO group is controlled with a Write DO command. A logical 1 written to a point turns the output transistor on. The output remains in that condition until the next Write DO command is executed. The contents of the DO register may be read using the Read DO command without changing the state of the output drivers.

External Sync Mode

The 'external sync' line permits the user to control the change of the DO group. 'External sync' meets all of the specifications of a DI point. Figure 5-2 shows the timing for DO external sync.

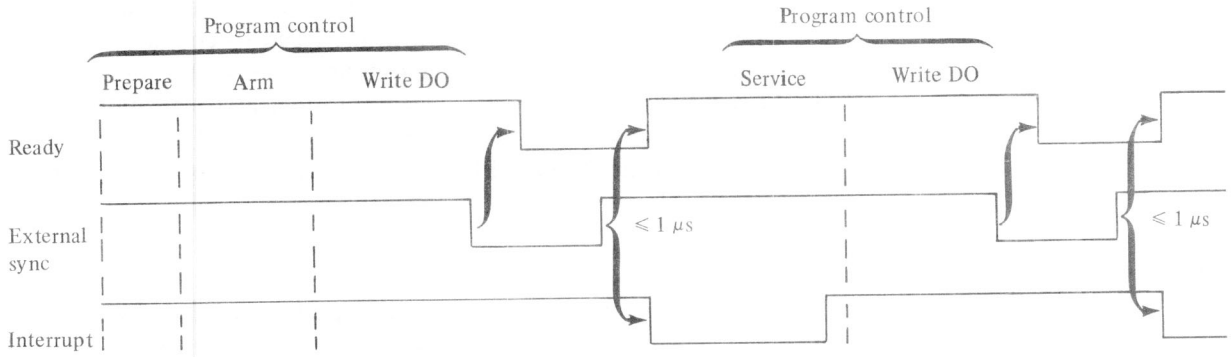


Figure 5-2. DO external sync timing diagram

This sequence is executed as follows:

1. The external sync mode of operation is initiated by an Arm External Sync command.
2. The user's external equipment signifies that it is ready to receive new input from the DO group by activating 'external sync' (down level).
3. The system signifies that the Write DO command is complete and that new data is available by activating the 'ready' output (down level).
4. When the external equipment has received the new data, it deactivates the 'external sync' input line (up level).
5. The system then deactivates the 'ready' line and posts an interrupt to the channel, indicating that the external equipment has received the data.
6. After the interrupt has been serviced, another Write DO command is performed to set up the group for the next data transfer sequence. The system is then waiting for the next transition of 'external sync' to an active state.

Diagnostic Mode

The diagnostic mode is entered by performing the Disable DO and the Set Diagnostic External Sync commands. These instructions disable all outputs and inputs for the group. If the Set Diagnostic External Sync command is performed after the Disable DO command, and if the DO group is set up to perform an external-sync transfer, the Set Diagnostic External Sync command causes an interrupt to be posted to the channel. If an interrupt is pending, busy is returned and the commands are not performed. In the diagnostic mode, all commands and modes operate as usual, except that the user's inputs are disabled and the user's outputs are turned off. When leaving diagnostic mode, the data in the DO register is placed on the user's outputs; the user's inputs are enabled.

Digital Input Operation

Each DI group can operate in one of four modes: (1) non-interrupting, (2) process interrupt, (3) external sync, and (4) diagnostic.

Non-Interrupting Mode

When operated in the non-interrupting mode, the state of the DI group non-latching input register is read with the Read PI command. This command reads the history of the DI inputs from the latching PI register. The PI register records the first logical 0 to logical 1 transition of each DI input following any system or feature reset. The Read PI With Reset command reads the latching PI register and then resets it at the end of the instruction cycle.

Process Interrupt Mode

The process interrupt mode is entered by performing the Arm PI command. The first logical 0 to logical 1 transition on any input of the armed group sets the appropriate bit in the latching register and causes an interrupt to be posted to the channel. After the interrupt is serviced, a Read PI With Reset command reads the latching register and resets it, allowing a new interrupt to be generated on the next transition of any input point of that group. If the interrupt is serviced and a Read PI command is issued, the PI register is not reset and a new interrupt is not generated.

External Sync Mode

Figure 5-3 is a timing diagram for DI external sync. This sequence is executed as follows:

1. The external sync mode is entered by performing the Arm External Sync command. This causes the 'ready' output line to become active, indicating that the system is ready for new input data.
2. A subsequent logical 0 to logical 1 transition on 'external sync' by the user's equipment latches the group register, deactivates the 'ready' line, and posts an interrupt to the channel.
3. After the interrupt is serviced, a Read DI command reads the DI register, resets the register, and activates the 'ready' line.

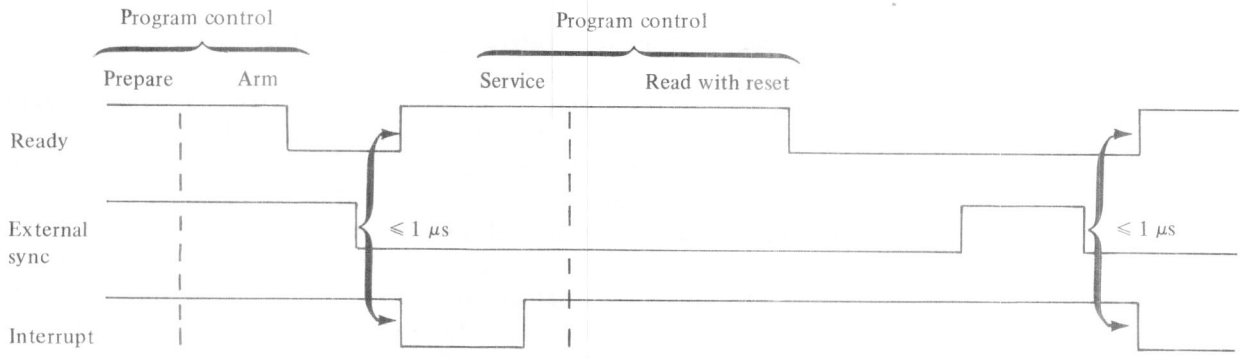


Figure 5-3. DI external sync timing diagram

Diagnostic Mode

The diagnostic mode is entered by performing either a Set Test Ones command or a Set Test Zeros command. When the appropriate command is executed: (1) the user's inputs are disabled, (2) either 1's or 0's are placed on the input receivers, and (3) the 'external sync' receiver is pulsed. When subsequent Read commands are issued, the DI group responds exactly as if the actual user inputs had been set, including the PI and external sync functions.

Integrated Digital I/O Electrical Characteristics

Digital Input (DI) Characteristics

Each digital input (or process interrupt) point is nonisolated and is designed to operate with TTL-compatible voltage levels. Voltage inputs up to ±24 volts may be used with this feature. Figure 5-4 shows a representative input point. For voltages above +5 volts, the input impedance is a function of the input voltage. Each DI point has an internal pull-up resistor, and unconnected inputs are held at the inactive state (up level).

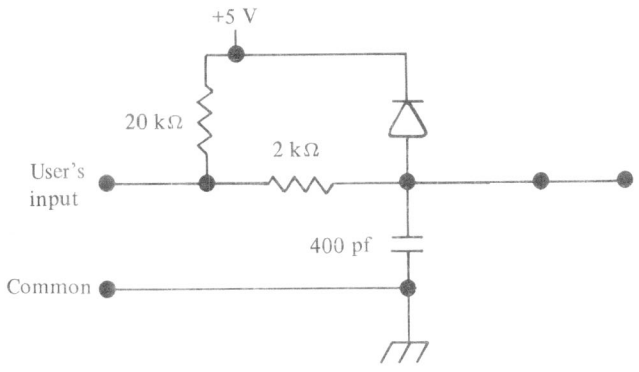


Figure 5-4. DI equivalent circuit

Digital and 'External Sync' Input Specifications

Each DI point and the 'external sync' input meet the following specifications:

Input impedance:	≥9.2 kilohms at less than +4.5 V; ≥2 kilohms at +24 V; ≥2 kilohms at −24 V
Input limits:	+24 Vdc, maximum; −24 Vdc, minimum
Logical 1:	≤1.0 volt
Logical 0:	≥2.5 volts

Response Time

Response time ($\leq$9 microseconds) is the time between the points at which the user's input meets and maintains the required voltage for the logical 1 level and the 50% point of the resulting interrupt request in the PI mode. This time includes an envelope of 5 microseconds in which the card could be performing a Read PI or Read PI With Reset command.

External Sync Deskew

The DI inputs must be stable for a minimum of 0.5 microsecond prior to and after the activation of 'external sync.' Changes during this time result in unpredictable data in the DI register.

Digital Output (DO) Characteristics

Each digital output point is a nonisolated, solid-state current-sink point, as represented by the equivalent circuit shown in Figure 5-5. When operated without a user-source voltage, each point generates TTL-compatible voltage levels. When operated with a user source higher than +5 volts, each point operates as an open collector, solid-state current sink. Each point is capable of sinking 100 mA in the "on" state. There is no restriction on the number of DO points sinking maximum current simultaneously.

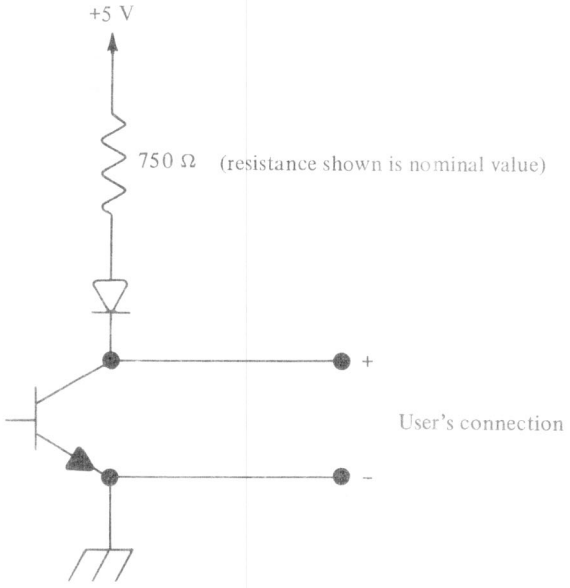


Figure 5-5. DO equivalent circuit

Digital and 'Ready' Output Specifications

Each DO point and the 'ready' output meet the following specifications into a resistive load:

Output Levels

Writing a logical 1 causes the output transistor to turn on. If a logical 0 is written, the output transistor turns off. When the transistor is on, the output is considered active.

Voltage output:

1. With user source:
   - Off state: +52.8 Vdc, maximum
   - On state: +0.8 Vdc, maximum
2. Without user source:
   - Off state: +5.5 Vdc at 0.0 mA source, maximum; +2.4 Vdc at 1.0 mA source, minimum
   - On state: +0.8 Vdc, maximum

Current input:

- On state: 100 mA, maximum, per point with user source
- Off state: 500 μa, maximum, per point at +52.8 Vdc user source

Response Time

Digital outputs meet and maintain specifications within 2 microseconds after the Write DO command is issued to the channel. 'Ready' output lags the digital outputs by a minimum of 500 nanoseconds and a maximum of 1 microsecond.

Integrated Digital I/O Physical Characteristics

Signal Pin Assignments

Figure 5-6 shows the location of the top-card connectors (TCCs) on the integrated digital I/O feature card and the pin-numbering scheme. Figures 5-7 through 5-9 list the pin assignments for each of the connectors.

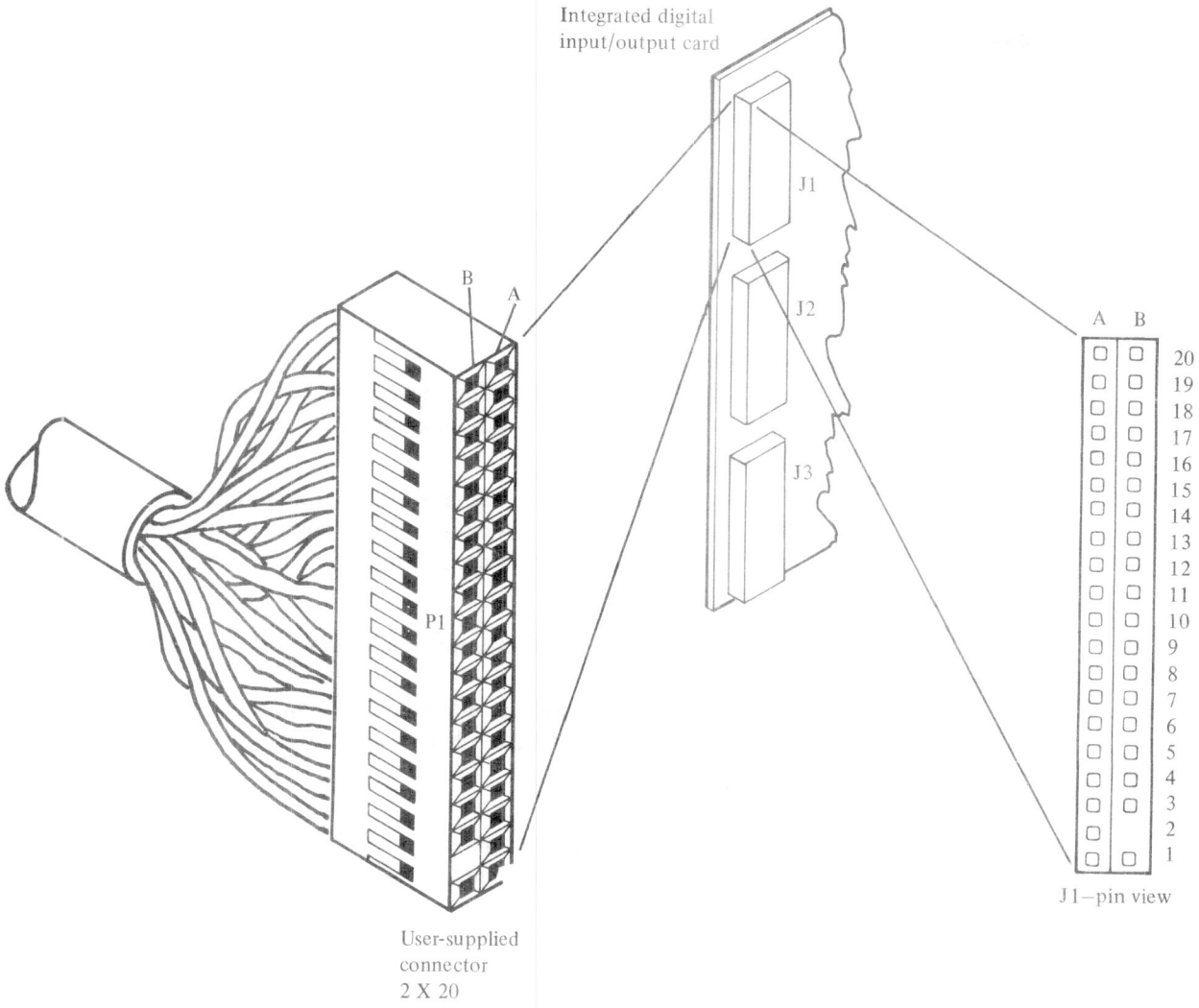


Figure 5-6. Integrated digital I/O feature card and cable connectors

Pin	J1—A-side	Group	J1—B-side	Group
20	DI 0	0	DI 1	0
19	DI 2	0	DI 3	0
18	DI 4	0	DI 5	0
17	Common		DI 6	0
16	Common		DI 7	0
15	Common		DI 8	0
14	Common		DI 9	0
13	Common		DI 10	0
12	Common		DI 11	0
11	Common		DI 12	0
10	Common		DI 13	0
9	Common		DI 14	0
8	Common		DI 15	0
7	Common		DI 0	1
6	Common		DI 1	1
5	Common		DI 2	1
4	Common		DI 3	1
3	DI 5	1	DI 4	1
2	DI 6	1	Polarizing pin	—
1	DI 8	1	DI 7	1

Figure 5-7. Integrated digital I/O pin assignments TCC connector J1 (top of card)

Pin	J2—A-side	Group	J2—B-side	Group
20	DI 9	1	DI 10	1
19	DI 11	1	DI 12	1
18	DI 13	1	DI 14	1
17	Common		DI 15	1
16	Common		Ext sync in	0
15	Common		Ext sync in	1
14	Common		Ext sync in	2
13	Common		Ext sync in	3
12	Common		Spare	2
11	Common		Spare	—
10	Common		Spare	—
9	Common		DO 0	2
8	Common		DO 1	2
7	Common		DO 2	2
6	Common		DO 3	2
5	Common		DO 4	2
4	Common		DO 5	2
3	DO 7	2	DO 6	2
2	DO 8	2	Polarizing pin	—
1	DO 10	2	DO 9	2

Figure 5-8. Integrated digital I/O pin assignments TCC connector J2 (middle of card)

Pin	J3—A-side	Group	J3—B-side	Group
20	DO 11	2	DO 12	2
19	DO 13	2	DO 14	2
18	DO 15	2	DO 0	3
17	Common		DO 1	3
16	Common		DO 2	3
15	Common		DO 3	3
14	Common		DO 4	3
13	Common		DO 5	3
12	Common		DO 6	3
11	Common		DO 7	3
10	Common		DO 8	3
9	Common		DO 9	3
8	Common		DO 10	3
7	Common		DO 11	3
6	Common		DO 12	3
5	Common		DO 13	3
4	Common		DO 14	3
3	Ready	0	DO 15	3
2	Ready	1	Polarizing pin	—
1	Ready	3	Ready	2

Figure 5-9. Integrated digital I/O pin assignments TCC connector J3 (bottom of card)

Integrated Digital I/O to Customer Access Panel Connections

Figure 5-10 shows the pin numbering scheme for the 160-pin contact block used for the customer access panel (CAP) feature. Figure 5-11 shows the relationship between the integrated digital I/O feature and the customer access panel feature. Figures 5-12 through 5-15 show the connections for both the top-card connectors (TCCs) and the CAP connector for each digital group.

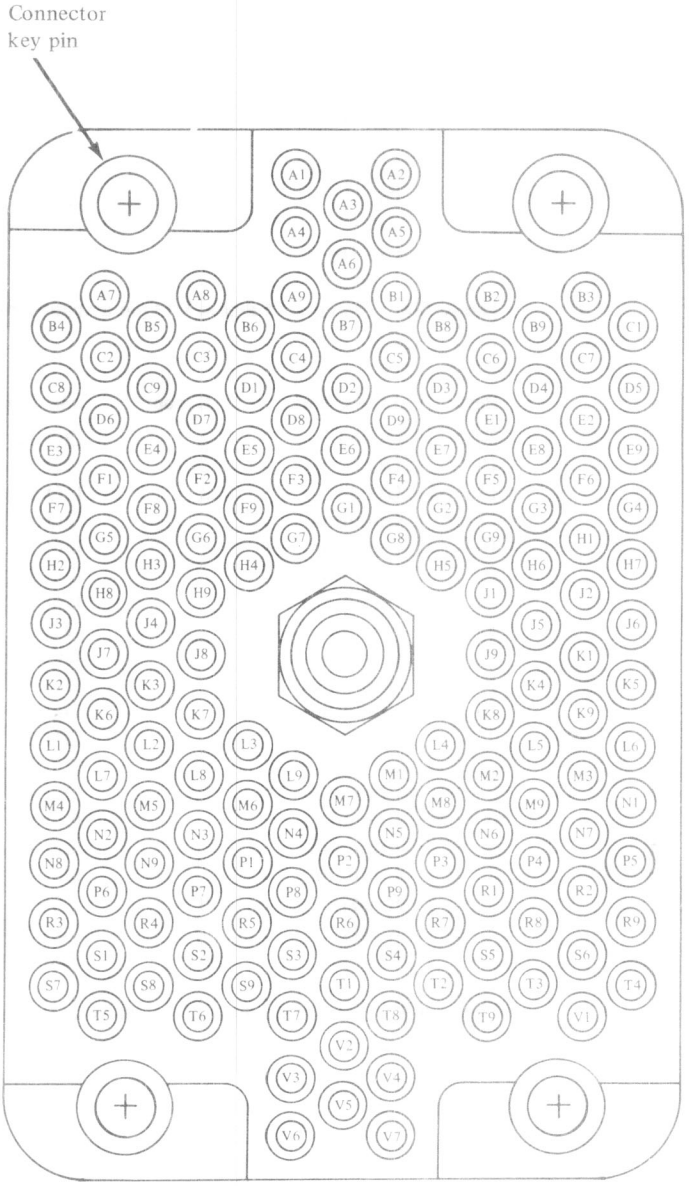


Figure 5-10. Customer access panel 160-pin connector

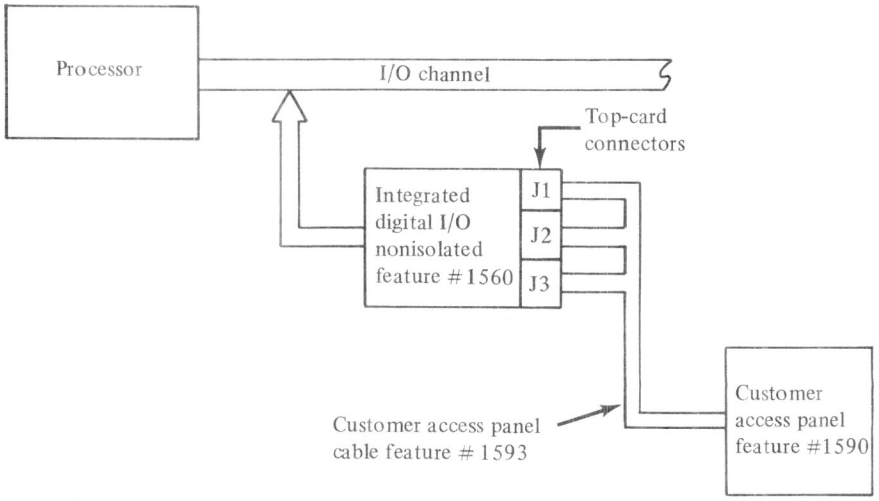


Figure 5-11. Relationship of integrated digital I/O feature to customer access panel feature

Name	TCC pin	CAP pin	Name	TCC pin	CAP pin
0+	J1A20	D3	8+	J1B15	F1
0–	Chassis	B2	8–	J1A12	C2
Shield	Frame		Shield	Frame	
1+	J1B20	F8	9+	J1B14	E9
1–	J1A17	C9	9–	J1A11	C1
Shield	Frame		Shield	Frame	
2+	J1A19	D2	10+	J1B13	E8
2–	Chassis	A6	10–	Chassis	C6
Shield	Frame		Shield	Frame	
3+	J1B19	F7	11+	J1B12	E7
3–	J1A16	C8	11–	Chassis	E1
Shield	Frame		Shield	Frame	
4+	J1A18	D1	12+	J1B11	E6
4–	J1A7	B6	12–	Chassis	G1
Shield	Frame		Shield	Frame	
5+	J1B18	F6	13+	J1B10	E5
5–	J1A15	C7	13–	Chassis	D7
Shield	Frame		Shield	Frame	
6+	J1B17	F4	14+	J1B9	E4
6–	Chassis	F5	14–	Chassis	C3
Shield	Frame		Shield	Frame	
7+	J1B16	F3	15+	J1B8	E3
7–	J1A13	C4	15–	J1A5	B4
Shield	Frame		Shield	Frame	
Ext sync +	J2B16	L7	Ready +	J3A3	M8
Ext sync –	J2A15	H8	Ready –	Chassis	N6
Shield	Frame		Shield	Frame	

Figure 5-12. TCC/CAP connections—digital input group 0

Name	TCC pin	CAP pin	Name	TCC pin	CAP pin
0+	J1B7	E2	8+	J1A1	A7
0–	J1A4	B3	8–	Chassis	A4
Shield	Frame		Shield	Frame	
1+	J1B6	D9	9+	J2A20	J6
1–	J1A14	C5	9–	J1A4	G4
Shield	Frame		Shield	Frame	
2+	J1B5	D8	10+	J2B20	M4
2–	J1A8	B7	10–	Chassis	L8
Shield	Frame		Shield	Frame	
3+	J1B4	D6	11+	J2A19	J5
3–	J1A6	B5	11–	Chassis	G9
Shield	Frame		Shield	Frame	
4+	J1B3	D5	12+	J2B19	M3
4–	Chassis	A2	12–	Chassis	M2
Shield	Frame		Shield	Frame	
5+	J1A3	B1	13+	J2A18	J4
5–	Chassis	A5	13–	Chassis	G6
Shield	Frame		Shield	Frame	
6+	J1A2	A9	14+	J2B18	M1
6–	Chassis	A8	14–	J2A7	G8
Shield	Frame		Shield	Frame	
7+	J1B1	D4	15+	J2B17	L9
7–	J1A10	B9	15–	Chassis	M7
Shield	Frame		Shield	Frame	
Ext sync +	J2B15	L6	Ready +	J3A2	M6
Ext sync –	Chassis	J9	Ready –	J3A12	P1
Shield	Frame		Shield	Frame	

Figure 5-13. TCC/CAP connections—digital input group 1

Name	TCC pin	CAP pin	Name	TCC pin	CAP pin
0+	J2B9	K9	8+	J2A2	G2
0–	J2A16	J2	8–	J2A11	H4
Shield	Frame		Shield	Frame	
1+	J2B8	K6	9+	J2B1	J7
1–	J2A5	G5	9–	J2A10	H3
Shield	Frame		Shield	Frame	
2+	J2B7	K5	10+	J2A1	F9
2–	J2A14	H7	10–	Chassis	F2
Shield	Frame		Shield	Frame	
3+	J2B6	K4	11+	J3A20	R2
3–	J2A13	H6	11–	J3A9	N7
Shield	Frame		Shield	Frame	
4+	J2B5	K3	12+	J3B20	T5
4–	Chassis	H9	12–	Chassis	T6
Shield	Frame		Shield	Frame	
5+	J2B4	K2	13+	J3A19	P9
5–	J2A9	H2	13–	J3A8	N5
Shield	Frame		Shield	Frame	
6+	J2B3	K1	14+	J3B19	T4
6–	J2A8	H1	14–	J3A16	P5
Shield	Frame		Shield	Frame	
7+	J2A3	G3	15+	J3A18	P8
7–	J2A6	G7	15–	J3A7	N4
Shield	Frame		Shield	Frame	
Ext sync +	J2B14	L5	Ready +	J3A1	R3
Ext sync –	Chassis	J1	Ready –	J3A6	N2
Shield	Frame		Shield	Frame	

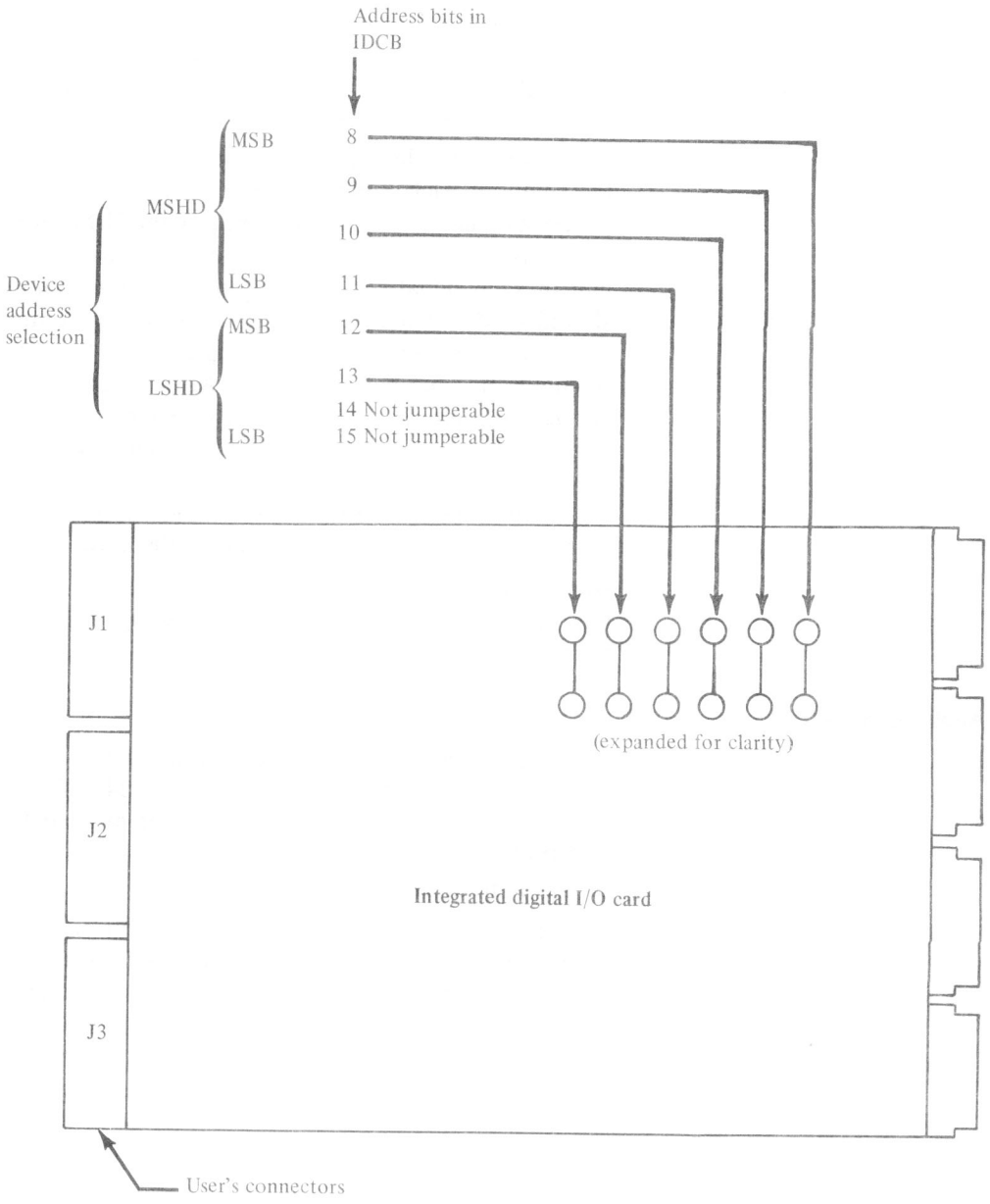
Figure 5-14. TCC/CAP connections—digital output group 2

Name	TCC pin	CAP pin	Name	TCC pin	CAP pin
0+	J3B18	T3	8+	J3B10	S3
0–	Chassis	T9	8–	Chassis	T7
Shield	Frame		Shield	Frame	
1+	J3B17	T2	9+	J3B9	S1
1–	Chassis	S5	9–	J3A17	P6
Shield	Frame		Shield	Frame	
2+	J3B16	T1	10+	J3B8	R9
2–	Chassis	V2	10–	J2A5	N1
Shield	Frame		Shield	Frame	
3+	J3B15	S9	11+	J3B7	R8
3–	Chassis	V3	11–	J3A15	P4
Shield	Frame		Shield	Frame	
4+	J3B14	S8	12+	J3B6	R7
4–	Chassis	S2	12–	J3A14	P3
Shield	Frame		Shield	Frame	
5+	J3B13	S7	13+	J3B5	R6
5–	J3A10	N8	13–	J3A13	P2
Shield	Frame		Shield	Frame	
6+	J3B12	S6	14+	J3B4	R5
6–	Chassis	V1	14–	Chassis	P7
Shield	Frame		Shield	Frame	
7+	J3B11	S4	15+	J3B3	R4
7–	Chassis	T8	15–	J3A11	N9
Shield	Frame		Shield	Frame	
Ext sync +	J2B13	L4	Ready +	J3B1	M5
Ext sync –	J2A12	H5	Ready –	Chassis	N3
Shield	Frame		Shield	Frame	

Figure 5-15. TCC/CAP connections—digital output group 3

Jumper Selections

Figure 5-16 shows the location of jumpers for the integrated digital I/O feature card.



Key:

MSB = most-significant bit
LSB = least-significant bit
MSHD = most-significant hexadecimal digit
LSHD = least-significant hexadecimal digit

Note: Jumpers plugged = logical 0
Jumpers removed = logical 1

Figure 5-16. Jumper selections

Integrated Digital I/O Design Considerations

All integrated digital I/O points are nonisolated. The ground reference for all these points is the top-card connector of the feature card. User-supplied cables that are appropriate to the environment should be used and, in most cases, should be shielded.

When attaching to the customer access panel, the shields of the input pairs should be attached to the frame at the 160-pin connector through a short, low-impedance stub. A screw terminal is provided for this purpose just below and to the right of the connectors.

When attaching directly to the top-card connectors with a customer cable, the shield of each cable should be attached to the frame as it enters the processor, the I/O expansion unit, or the IBM 4997 Rack Enclosure, whichever comes first. There are common pins provided for the reference half of each signal pair on the top-card connectors. The reference halves should be doubled-up and attached to these "common" pins. The reference lines must be doubled-up because there are not enough commons to supply one pin per signal pair. After all the reference halves are connected, there should be at least six empty common pins. The empty pins should be joined together and attached to the frame ground through as short a path as possible. Screw terminals for this purpose are located on top of the processor and I/O expansion units. The empty pins should be located in a group at the very top of the card.

Because the performance of this interface may be affected by noise, appropriate arc suppression, noise filtering, etc., may be necessary on the user's inputs.

Application Notes

The cables that plug into the top-card connector on the integrated digital I/O feature card should be made using #24 AWG wire and must use Berg part number 75598-003 pins (or equivalent) and Berg part number 65405-013 housing (or equivalent). Refer to Figure 5-6 for an illustration of the cable connector.

The cable to the customer access panel can be made using a 160-pin male connector block, Amp* part number 202799-2 (or equivalent): female contacts, Amp part number 66108-1 (or equivalent); and #26 AWG wire.

* Amp, Incorporated

Chapter 6. Customer Direct Program Control (DPC) Adapter Feature

Introduction

Figure 6-1 is a block diagram of the customer DPC adapter feature, which provides the end-user with a subset of the processor I/O channel. The interface adheres to the processor I/O channel architecture, with an additional throughput delay of approximately 2.5 microseconds.

The DPC adapter feature is designed to perform direct program control (DPC) functions only and can be configured to accommodate 4, 8, or 16 I/O device addresses; therefore, the feature allows interrupt vectoring for up to 16 interrupting sources. The actual number of devices connected, when configured as stated here, is limited by the termination scheme implemented by the customer. The termination scheme must provide data-buffering hardware and control-handshaking logic to expand the number of attached devices to the configured limits. The I/O device address configuration allows interrupt vectoring for up to 16 interrupting sources by individual device address. A DPC operation causes a parallel transfer of one 16-bit word of data or control information to or from an I/O device. An Operate I/O instruction must be executed for each data transfer. Data bus parity is checked. When parity is not generated by an I/O device on the input data bus, internal circuitry on the feature card generates odd parity.

All the devices attached to the DPC adapter share a common prepare field (interrupt level and I-bit). The adapter has 75 lines, including 18 data bus-out bits (with two parity bits), 18 data bus-in bits (with two parity bits), 16 interrupt request in lines (when configured for 16 I/O device addresses), three function bits, four modifier bits, four I/O device address bits, and 12 control and response lines. The data flow is always 16 bits without the parity option or 18 bits (including two parity bits) with the parity option.

Diagnostic capability is designed into the DPC adapter feature card. This capability allows the user to send data or control information from the processor and "wrap" the same information back to the processor from either the adapter card or from an external I/O device.

The DPC adapter feature uses TTL nonisolated cable drivers with a current capacity of 175 mA. This allows a wide range of customer termination schemes.

Relationship to Other Features

Jumper pins are provided on the circuit card to select the address domain of the adapter. The configuration must include assignment of a device address with a range of either 4, 8, or 16 contiguous addresses. A parity option is also selected to be compatible with attached devices. Interrupts can be masked off during external diagnostic mode by jumper selection.

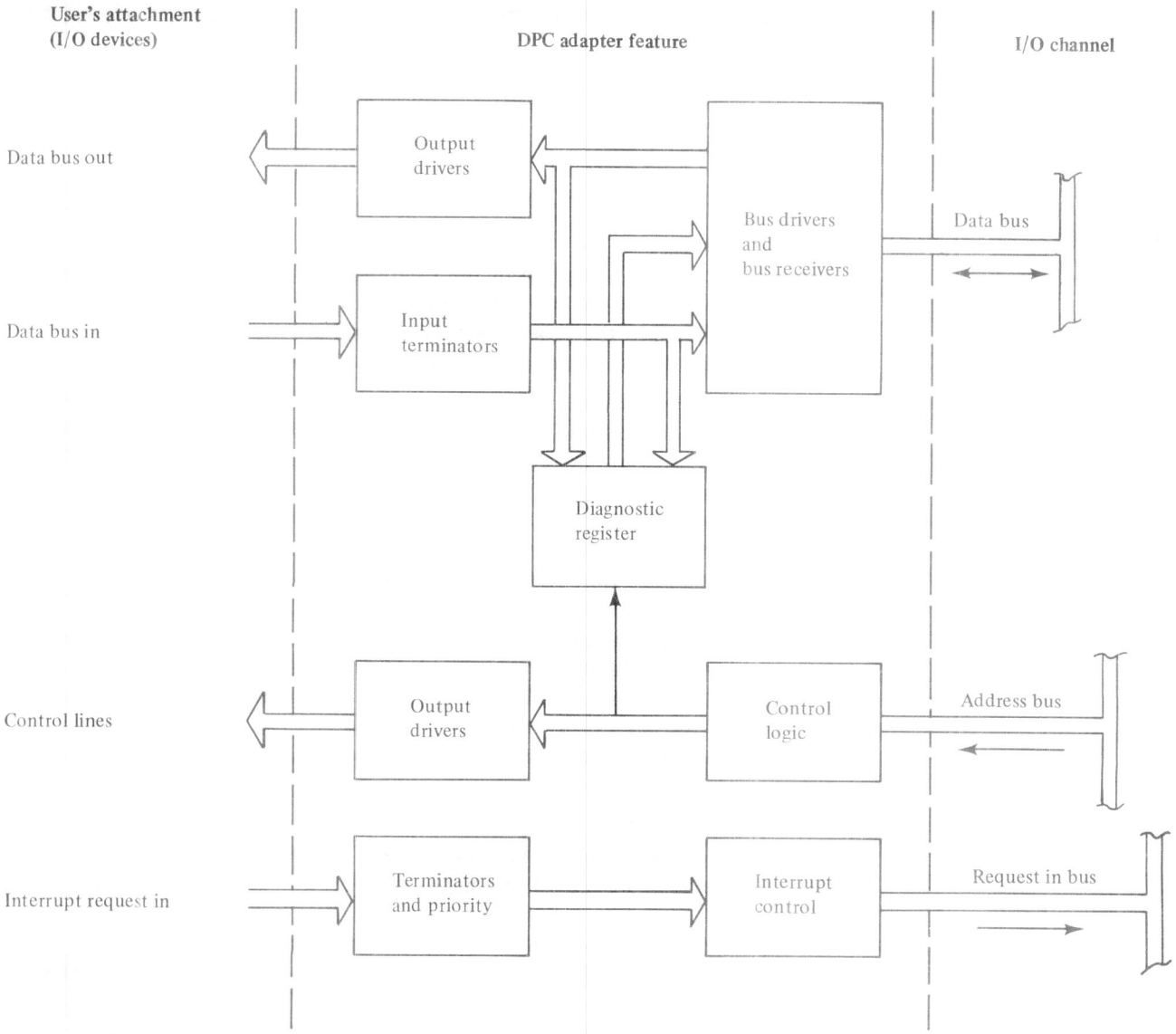


Figure 6-1. Block diagram of the customer direct program control adapter feature

Application Summary

The DPC adapter feature card provides a convenient means of attaching customer equipment to the processor I/O channel.

To facilitate attachment of various devices to the adapter interface, additional hardware is required. Like the processor I/O channel, the DPC adapter provides no functional capability in a stand-alone configuration. The DPC adapter can be used for attachment of: typical digital instruments, another computer, typical data processing I/O equipment (such as low-speed readers, punches, or plotters), or typical commercial data-acquisition systems.

Functional Description of the DPC Adapter Signal Lines

The DPC adapter has 75 lines that can have subsets, depending on the level of functions required by the I/O device. Bits 1–3 and bits 4–7 of the command field in the IDCB are mapped into DPC adapter function bits (three bits) and modifier bits (four bits), respectively. Bits 12, 13, 14, and 15 of the device address field in the IDCB are mapped into the DPC adapter device address bits. If the DPC adapter is configured for less than 16 I/O devices, bits 12 and 13 are truncated, as necessary, and replaced by 0's in the DPC adapter device address bits. Device addresses should start at the lowest-configured device address. Figure 6-2 shows all the I/O lines available between the DPC adapter and attached devices.

Signal name*	Direction (adapter/device)	Number of lines
I/O active	→	1
Function bits	→	3
Modifier bits	→	4
Device address	→	4
Data bus out	→	18 (16)**
Interrupt service active	→	1
Strobe	→	1
Data bus in	←	18 (16)**
Interrupt request	←	16
Condition code in	←	3
Select response	←	1
Halt or MCHK	→	1
System reset	→	1
Power-on reset	→	1
Diagnostic mode	→	1
Diagnostic mode modifier	→	1

*All signal lines are down-level active.

**When parity option is not selected.

Figure 6-2. DPC adapter signal lines

The DPC adapter signal lines are defined in the following sections.

I/O Active

'I/O active' is an outbound tag to signal to an I/O device that it may begin execution of the command specified by the function and modifier bits. This tag is necessary to execute all device-directed commands. It is active at least 200 nanoseconds after activation of the function, modifier, and device-address bits.

Function Bits

The 'function bits' are three outbound lines that specify the general type of I/O operation to be performed. They are defined as follows:

Function bits	Function
0 1 2	
0 0 0	Read data
0 0 1	Read data
0 1 0	Read status
0 1 1	Reserved*
1 0 0	Write data
1 0 1	Write data
1 1 0	Write control
1 1 1	Reserved*

*These are system-reserved functions for cycle-steal and should not be implemented by devices. Devices should return command reject to these functions, subject to Operate I/O instruction condition-code precedence, as defined in the appropriate processor description manual (see Preface).

Modifier Bits

The 'modifier bits' are four outbound lines that are used in conjunction with the function bits for further definition of the I/O operation to be performed. Certain modifier values, when used with read status or write control, have system functions and must be implemented by all attached devices. These commands are defined as follows:

Function	Modifier bits	Command
	0 1 2 3	
Read status	0 0 0 0	Read ID
Write control	1 1 1 1	Device Reset

The modifier bit values for device-directed commands are device-dependent, with the exception of the preceding formats, and are defined as follows:

Function bits	Modifier bits	Command
0 1 2	*0 1 2 3*	
0 0 X	X X X X	Read Data
0 1 0	X X X X	Read Status
1 0 X	X X X X	Write Data
1 1 0	X X X X	Write Control

Note: X=0 or 1.

Device Address

'Device address' is a set of four outbound lines. These lines contain four bits of encoded device address to select the device that is to respond to the current operation. 'Device address' is used during both an I/O active sequence or an interrupt-service active sequence. When the DPC adapter is configured to attach less than 16 I/O devices, the leading bit of each device-address is always 0.

Data Bus Out

'Data bus out' is an 18-bit outbound bus with 16 bits of data and two parity bits, odd parity by byte. This bus is used to transfer data and control information to the I/O devices and is active during write-data or write-control operations.

During the write-data or write-control operation, 'data bus out' is active from 200 nanoseconds before the rise of the 'I/O active' tag until the fall of the 'select response' tag, measured at the output of the DPC adapter card. During the inactive state, 'data bus out' is logically 0, including parity. When the parity option is not selected, the device uses only the 16 data lines.

Interrupt Service Active

'Interrupt service active' is an outbound tag line used to signal an I/O device that an interrupt-service sequence may now begin. The tag is active from 200 nanoseconds after 'device address' is activated and remains active until the fall of the 'select response' tag, measured at the output of the DPC adapter card.

Strobe

'Strobe' is an outbound line to the I/O device presently being selected (device address equivalent to the preassigned address of an I/O device) during an I/O active sequence or an interrupt-service active sequence.

During an I/O active sequence, the device should use 'strobe' to register data on the outbound data transfer or use it to reset data (for example, Read PI With Reset command) on the inbound data transfer. During an interrupt-service active sequence, the selected device uses 'strobe' to reset its interrupt request, interrupt information byte (IIB), or interrupt status byte (ISB).

If a parity error is detected by the processor I/O channel during a read-data or read-status operation, 'strobe' is inactive throughout the sequence.

If the DPC adapter card is configured without the parity option and a parity error is detected during a write-data or write-control operation, the 'strobe line' is inactive throughout the sequence, except during the system-defined Device Reset command.

Data Bus In

'Data bus in' is an 18-bit inbound bus with 16 bits of data and two parity bits, odd parity by byte. This bus is used to transfer data and status information from the devices to the processor, and is activated by selected devices during Read Data, Read Status, or an interrupt-service active sequence. When the parity option is not selected, the device generates only 16 bits of data.

Interrupt Request

There are 16 inbound 'interrupt request' lines from 16 devices (when configured for 16 device addresses). An external device signals an interrupt condition by raising its 'interrupt request' line. Once this line is raised, a device must keep its request active until (1) it is serviced (the interrupting device activates the 'select response' tag during an interrupt-service active sequence and receives 'strobe') or (2) the device receives Device Reset, 'halt or MCHK,' 'system reset,' or 'power-on reset.'

Condition Code In

'Condition code in' is a three-bit binary encoded bus used by an I/O device to pass status information to the processor during an I/O active sequence or an interrupt-service active sequence.

The 'condition code in' bus is activated with the rise of the 'select response' tag and is maintained active at least until 'strobe' goes active, as seen at the output of the I/O device. Once a value is activated on the 'condition code in' bus, it is not changed.

Select Response

'Select response' is an inbound tag sent by an I/O device to signal recognition of 'I/O active' or 'interrupt service active.' This tag also indicates to the DPC adapter feature that the required inbound data and/or control information for the transfer has been placed on the interface. Any data or information must be activated on the interface no later than the rise of 'select response,' as seen at the output of the I/O device. This tag may fall no sooner than the fall of 'I/O active' or 'interrupt service,' as seen at the output of the I/O device.

Halt or MCHK

'Halt or MCHK' is a tag from the processor I/O channel to all I/O devices. The tag means that a Halt I/O command has been issued by the program or that a machine-check class interrupt has occurred. When this tag is detected by an I/O device, the device must clear any status, states, requests, interface control logic, and registers, with the following exceptions:

- Output sensor points
- Timer values
- Those registers not addressable by the software

System Reset

'System reset' is a tag to all attached I/O devices, and is singular in nature and meaning. When 'system reset' is detected, an I/O device must reset and clear any status, states, requests, registers, and interface control logic.

Power-On Reset

'Power-on reset' is an outbound control line from the power supply to all system components. It is activated on all power on/off sequences. While 'power-on reset' is active, all system components are held in a system reset state. Residual addresses, output sensor points, and timer values are also reset. The receiver for this line is always enabled.

Diagnostic Mode and Diagnostic Mode Modifier

The 'diagnostic mode' line and the 'diagnostic mode modifier' line are device-dependent. These lines can be used as programmable control lines in conjunction with the Set Diagnostic Mode command (external diagnostic mode).

DPC Adapter Operational Characteristics

The DPC adapter performs three types of information or status transfers: output, input, and interrupt-service sequences.

There are no timing restrictions inherent in the interface architecture and, as such, the interface is called asynchronous. This means that the response from a given I/O device triggers the next sequential action rather than a specified timing condition. (Time-out indications for error detection are not excluded.)

Output Sequence

Figure 6-3 is a timing diagram for a typical output sequence.

An output sequence is executed as follows:

1. Function, modifier, device address bits, and data are placed on their appropriate lines.
2. The 'I/O active' tag is skewed (at least 200 nanoseconds) and activated on the interface.
3. Upon recognition of an address compare and 'I/O active,' the device raises the 'select response' tag. Once raised, this tag must be held active at least until the fall of the 'I/O active' tag. 'Condition code in' must be active until 'strobe' becomes active or until 'I/O active' becomes inactive for the duration of the 'select response' tag.
4. 'Strobe' is activated and dropped.

   Note: If the DPC adapter feature is configured without the parity option and a parity error is detected between the processor I/O channel and the feature, 'strobe' is not activated except during the Device Reset command.
5. The 'I/O active' tag is deactivated.
6. Upon recognition of the absence of the 'I/O active tag,' the device drops 'select response' and 'condition code in.'
7. The function, function modifier, device address, and data buses are deactivated.

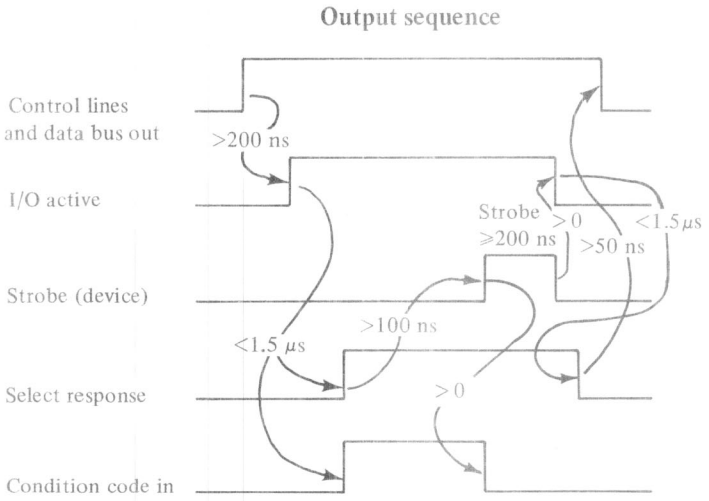


Figure 6-3. Output sequence timing diagram

Input Sequence

Figure 6-4 is a timing diagram for a typical input sequence.

An input sequence is executed as follows:

1. Function, modifier, and device address bits are placed on their appropriate lines.
2. The 'I/O active' tag is skewed (at least 200 nanoseconds) and activated on the interface.
3. Upon recognition of an address compare and 'I/O active,' the device raises the 'select response' tag. Once raised, this tag must be held active at least until the fall of the 'I/O active' tag. 'Data bus in' and 'condition code in' must be active until 'strobe' becomes active or until 'I/O active' becomes inactive for the duration of the 'select response' tag.
4. 'Strobe' is activated and dropped; however, if a parity error is detected by the processor, this tag is not activated.
5. The 'I/O active' tag is deactivated.
6. Upon recognition of the absence of the 'I/O active' tag, the device drops 'select response,' 'condition code in,' and 'data bus in.'

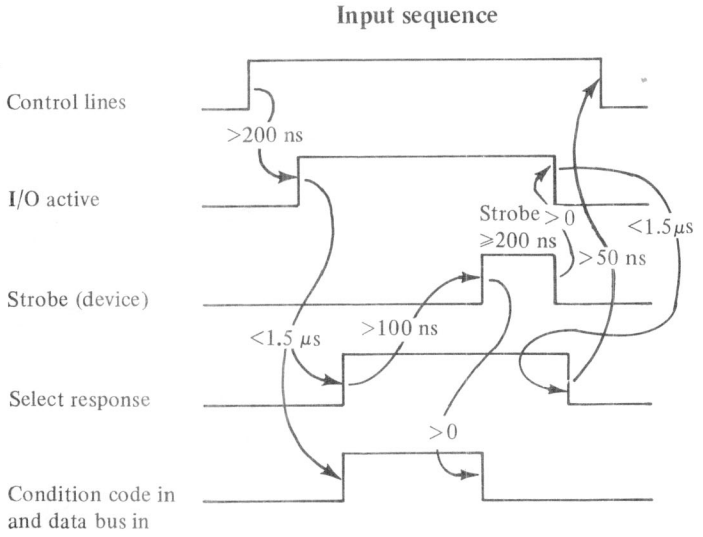


Figure 6-4. Input sequence timing diagram

Interrupt-Service Sequence

Figure 6-5 is a timing diagram for a typical interrupt-service sequence. This sequence is executed as follows:

1. The device address bits are placed on their appropriate lines.
2. The 'interrupt service active' tag is skewed (at least 200 nanoseconds) and activated on the interface.
3. Upon recognition of an address compare and 'interrupt service active,' the device raises the 'select response' tag. Once raised, this tag must be held active at least until the fall of the 'interrupt service active' tag. 'Condition code in' and 'data bus in' must be active for the duration of the 'select response' tag or at least remain active until 'strobe' becomes active.
4. 'Strobe' is activated and dropped. The I/O device must reset its interrupt request at the leading edge of 'strobe.'
5. The 'interrupt service active' tag is deactivated.
6. Upon recognition of the absence of the 'interrupt service active' tag, the device drops 'select response,' 'condition code in,' and 'data bus in.'
7. The device address bus is deactivated.

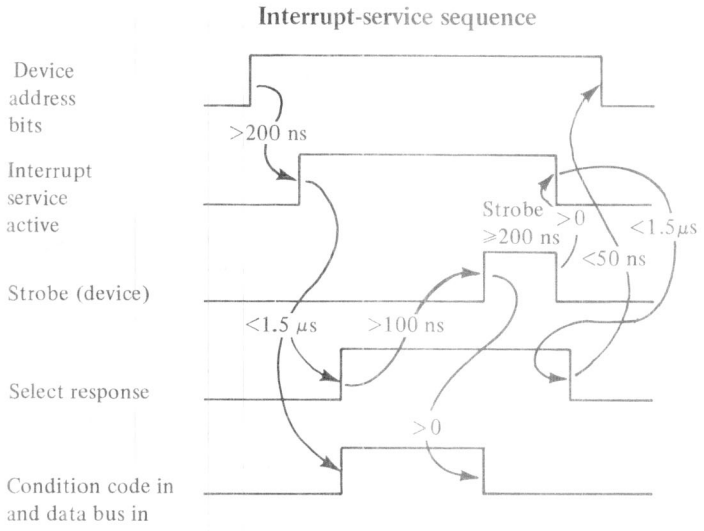


Figure 6-5. Interrupt-service sequence timing diagram

DPC Adapter Electrical Characteristics

The DPC adapter drivers and terminators are designed to interface with cables that have a characteristic impedance of approximately 100 ohms.

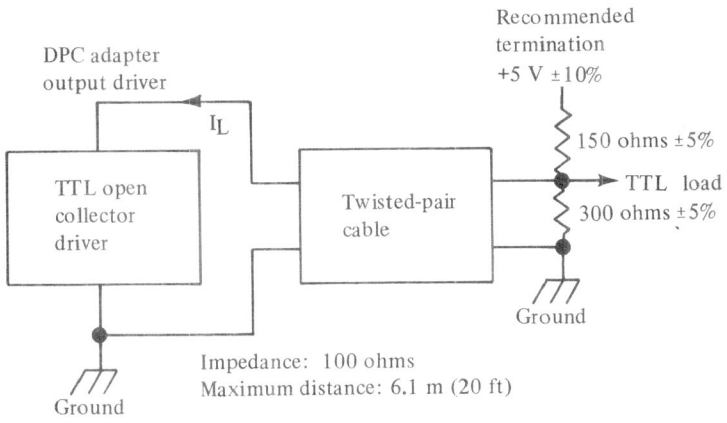
All DPC adapter interface lines are down-level active; the interface is nonisolated, TTL compatible.

Drivers

Figure 6-6 shows the output signal electrical circuit.

The output specifications are as follows:

Driver type:	TTL open collector	
Output voltage:	Up level:	+2.4 volts leakage current, minimum; I_L = 40 μa at 2.4 V, maximum
	Down level:	+0.7 volt at 175 mA, maximum
Input current:	Maximum current sinking capacity, 175 mA at +0.7 volt	



Up level:	+2.4 volts leakage current, minimum I_L = 40 μa at 2.4V, maximum
Down level:	+0.7 volt at 175 mA, maximum

Figure 6-6. Output signal electrical circuit

Receivers

Figure 6-7 shows the input signal electrical circuit.

The input specifications are as follows:

Input voltage:	Down level: +0.6 volt at 42 mA, maximum Up level: +2.4 volts, minimum
Input current:	≤ 42 mA at +0.6 volt
Input impedance:	100 ohms
Logical 1:	≤ +1.0 volt
Logical 0:	≥ +2.5 volts

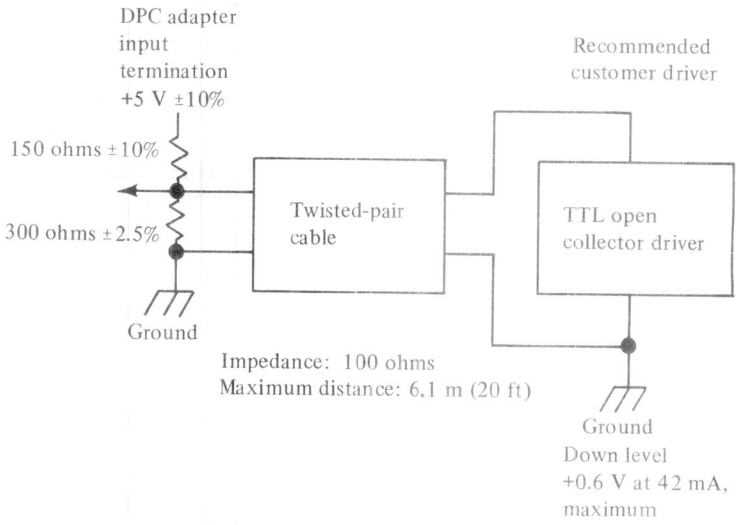


Figure 6-7. Input signal electrical circuit

DPC Adapter Physical Characteristics

Signal Pin Assignments

Figure 6-8 shows the top-card connectors (TCCs) for the DPC adapter. Figures 6-9 through 6-11 list the pin assignments for each of the connectors.

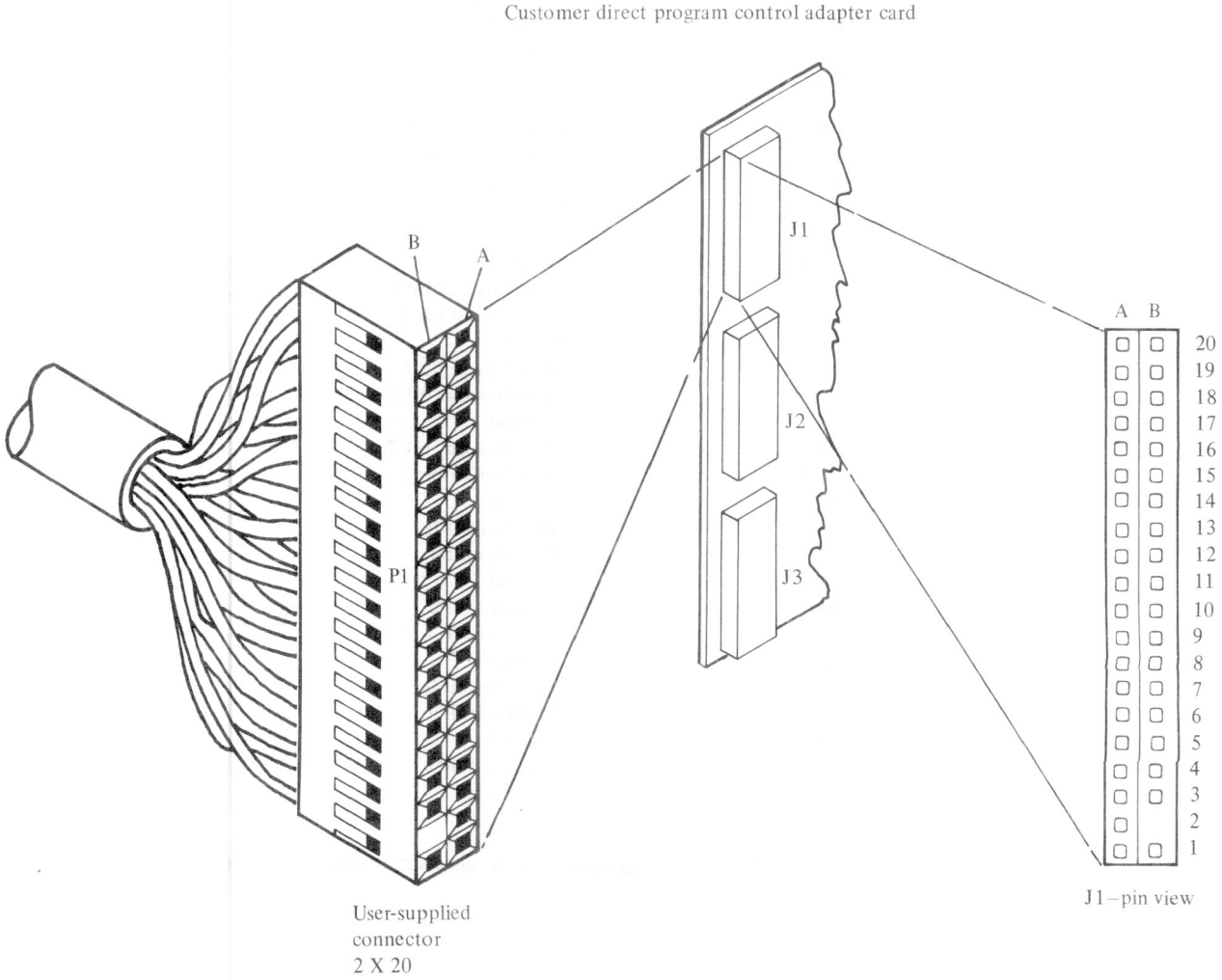


Figure 6-8. Customer DPC adapter card and cable connector

Pin assignment	Signal
A01	Data bus in parity 0–7
B01	Data bus out parity 0–7
A02	Ground
B02	Plugged - key
A03	Data bus in bit 0
B03	Data bus out bit 0
A04	Ground
B04	Data bus out bit 1
A05	Data bus in bit 1
B05	Ground
A06	Data bus in bit 2
B06	Data bus out bit 2
A07	Ground
B07	Data bus out bit 3
A08	Data bus in bit 3
B08	Ground
A09	Data bus in bit 4
B09	Data bus out bit 4
A10	Ground
B10	Data bus out bit 5
A11	Data bus in bit 5
B11	Ground
A12	Data bus in bit 6
B12	Data bus out bit 6
A13	Ground
B13	Data bus out bit 7
A14	Data bus in bit 7
B14	Ground
A15	Modifier bit 0
B15	Modifier bit 1
A16	Ground
B16	Modifier bit 2
A17	Modifier bit 3
B17	Ground
A18	Function bit 0
B18	Function bit 1
A19	Ground
B19	Function bit 2
A20	Not used
B20	Ground

Figure 6-9. DPC adapter pin assignments—TCC connector J1 (top of card)

Pin assignment	Signal
A01	Data bus in parity 8–15
B01	Data bus out parity 8–15
A02	Ground
B02	Plugged - key
A03	Data bus in bit 8
B03	Data bus out bit 8
A04	Ground
B04	Data bus out bit 9
A05	Data bus in bit 9
B05	Ground
A06	Data bus in bit 10
B06	Data bus out bit 10
A07	Ground
B07	Data bus out bit 11
A08	Data bus in bit 11
B08	Ground
A09	Data bus in bit 12
B09	Data bus out bit 12
A10	Ground
B10	Data bus out bit 13
A11	Data bus in bit 13
B11	Ground
A12	Data bus in bit 14
B12	Data bus out bit 14
A13	Ground
B13	Data bus out bit 15
A14	Data bus in bit 15
B14	Ground
A15	Select response
B15	Diagnostic mode
A16	Ground
B16	Diagnostic mode modifier
A17	Condition code in bit 0
B17	Ground
A18	Condition code in bit 1
B18	Condition code in bit 2
A19	Ground
B19	Not used
A20	Not used
B20	Ground

Figure 6-10. DPC adapter pin assignments—TCC connector J2 (middle of card)

Pin assignment	Signal
A01	Interrupt request 0
B01	Interrupt request 1
A02	Ground
B02	Plugged - key
A03	Interrupt request 2
B03	Interrupt request 3
A04	Ground
B04	Interrupt request 4
A05	Interrupt request 5
B05	Ground
A06	Interrupt request 6
B06	Interrupt request 7
A07	Ground
B07	Interrupt request 8
A08	Interrupt request 9
B08	Ground
A09	Interrupt request 10
B09	Interrupt request 11
A10	Ground
B10	Interrupt request 12
A11	Interrupt request 13
B11	Ground
A12	Interrupt request 14
B12	Interrupt request 15
A13	Ground
B13	Device address bit 0
A14	Device address bit 1
B14	Ground
A15	Device address bit 2
B15	Device address bit 3
A16	Ground
B16	Interrupt service active
A17	I/O active
B17	Ground
A18	Strobe
B18	Halt or MCHK
A19	Ground
B19	System reset
A20	Power on reset
B20	Ground

Figure 6-11. DPC adapter pin assignments—TCC connector J3 (bottom of card)

DPC Adapter to Customer Access Panel Connections

Figure 6-12 shows the connection from the DPC adapter top-card connectors (TCCs) to the customer access panel (CAP) connector (feature #1590). For an illustration of the CAP connector, refer to Figure 5-10.

Signal name		TCC pin	CAP connector
Data bus in bit	+	J1A3	A7
	–	Chassis	A8
Data bus in bit 1	+	J1A5	B4
	–	J1A4	B5
Data bus in bit 2	+	J1A6	C2
	–	Chassis	C3
Data bus in bit 3	+	J1A8	C8
	–	J1A7	C9
Data bus in bit 4	+	J1A9	D6
	–	Chassis	D7
Data bus in bit 5	+	J1A11	E3
	–	J1A10	E4
Data bus in bit 6	+	J1A12	F1
	–	Chassis	F2
Data bus in bit 7	+	J1A14	F7
	–	J1A13	F8
Data bus in bit 8	+	J2A3	G5
	–	Chassis	G6
Data bus in bit 9	+	J2A5	H2
	–	J2A7	H3
Data bus in bit 10	+	J2A6	H8
	–	Chassis	H9
Data bus in bit 11	+	J2A8	J3
	–	J2A10	J4
Data bus in bit 12	+	J2A9	J7
	–	Chassis	J8
Data bus in bit 13	+	J2A11	K2
	–	J2A13	K3
Data bus in bit 14	+	J2A12	K6
	–	Chassis	K7
Data bus in bit 15	+	J2A14	L1
	–	J2A16	L2
Data bus in parity 0–7	+	J1A1	L7
	–	Chassis	L8
Data bus in parity 8–15	+	J2A1	M4
	–	J2A2	M5

Figure 6-12 (Part 1 of 4). DPC adapter to customer access panel

Signal name		TCC pin	CAP connector
Data bus out bit 0	+	J1B3	B3
	–	Chassis	B2
Data bus out bit 1	+	J1B4	C1
	–	J1A2	B9
Data bus out bit 2	+	J1B6	C7
	–	Chassis	C6
Data bus out bit 3	+	J1B7	D5
	–	J1B5	D4
Data bus out bit 4	+	J1B9	E2
	–	Chassis	E1
Data bus out bit 5	+	J1B10	E9
	–	J1B8	E8
Data bus out bit 6	+	J1B12	F6
	–	Chassis	F5
Data bus out bit 7	+	J1B13	G4
	–	J1B11	G3
Data bus out bit 8	+	J2B3	H1
	–	Chassis	G9
Data bus out bit 9	+	J2B4	H7
	–	J2B5	H6
Data bus out bit 10	+	J2B6	J2
	–	Chassis	J1
Data bus out bit 11	+	J2B7	J6
	–	J2B8	J5
Data bus out bit 12	+	J2B9	K1
	–	Chassis	J9
Data bus out bit 13	+	J2B10	K5
	–	J2B11	K4
Data bus out bit 14	+	J2B12	K9
	–	Chassis	K8
Data bus out bit 15	+	J2B13	L6
	–	J2B14	L5
Data bus out parity 0–7	+	J1B1	M3
	–	Chassis	M2
Data bus out parity 8–15	+	J2B1	N1
	–	J2A4	M9

Figure 6-12 (Part 2 of 4). DPA adapter to customer access panel

Signal name		TCC pin	CAP connector
Modifier bit 0	+	J1A15	N2
	–	Chassis	N3
Modifier bit 1	+	J1B15	N8
	–	J1B14	N9
Modifier bit 2	+	J1B16	P6
	–	Chassis	P7
Modifier bit 3	+	J1A17	R3
	–	J1A16	R4
Device address bit 0	+	J3B13	N7
	–	Chassis	N6
Device address bit 1	+	J3A14	P5
	–	J3A13	P4
Device address bit 2	+	J3A15	R2
	–	Chassis	R1
Device address bit 3	+	J3B15	R9
	–	J3B14	R8
Function bit 0	+	J1A8	S1
	–	Chassis	S2
Function bit 1	+	J1B18	S7
	–	J1B17	S8
Function bit 2	+	J1B19	T5
	–	Chassis	T6
Condition code 0	+	J2A17	S6
	–	Chassis	S5
Condition code 1	+	J2A18	T4
	–	J2A19	T3
Condition code 2	+	J2B18	V1
	–	Chassis	T9
Select response	+	J2A15	M6
	–	J2B17	N4
Diagnostic mode	+	J2B15	P2
	–	Chassis	M7
Diagnostic mode modifier	+	J2B16	L4
	–	Chassis	M1
Interrupt service active	+	J3B16	M8
	–	J3B17	N5
I/O active	+	J3A17	P1
	–	Chassis	P8
Strobe	+	J3A18	P3
	–	Chassis	P9

Figure 6-12 (Part 3 of 4). DPC adapter to customer access panel

Signal name		TCC pin	CAP connector
Interrupt request 0	+	J3A1	A1
	–	J3A2	A4
Interrupt request 1	+	J3B1	A3
	–	Chassis	A6
Interrupt request 2	+	J3A3	A2
	–	Chassis	A5
Interrupt request 3	+	J3B3	B6
	–	Chassis	A9
Interrupt request 4	+	J3B4	B8
	–	Chassis	B1
Interrupt request 5	+	J3A5	D1
	–	J3A4	C4
Interrupt request 6	+	J3A6	D3
	–	J3A7	C5
Interrupt request 7	+	J3B6	D2
	–	J3B5	B7
Interrupt request 8	+	J3B7	E5
	–	Chassis	D8
Interrupt request 9	+	J3A8	E7
	–	Chassis	D9
Interrupt request 10	+	J3A9	F9
	–	J3A10	F3
Interrupt request 11	+	J3B9	G2
	–	J3B8	F4
Interrupt request 12	+	J3B10	G1
	–	J3B11	E6
Interrupt request 13	+	J3A11	H4
	–	Chassis	G7
Interrupt request 14	+	J3A12	H5
	–	Chassis	G8
Interrupt request 15	+	J3B12	L3
	–	Chassis	L9
Halt or MCHK	+	J3B18	R5
	–	J3A16	S3
System reset	+	J3B19	R6
	–	J3A19	T1
Power on reset	+	J3A20	R7
	–	J3B20	S4

Figure 6-12 (Part 4 of 4). DPC adapter to customer access panel

Jumper Selections

Figure 6-13 shows the location of jumpers for the DPC adapter feature card.

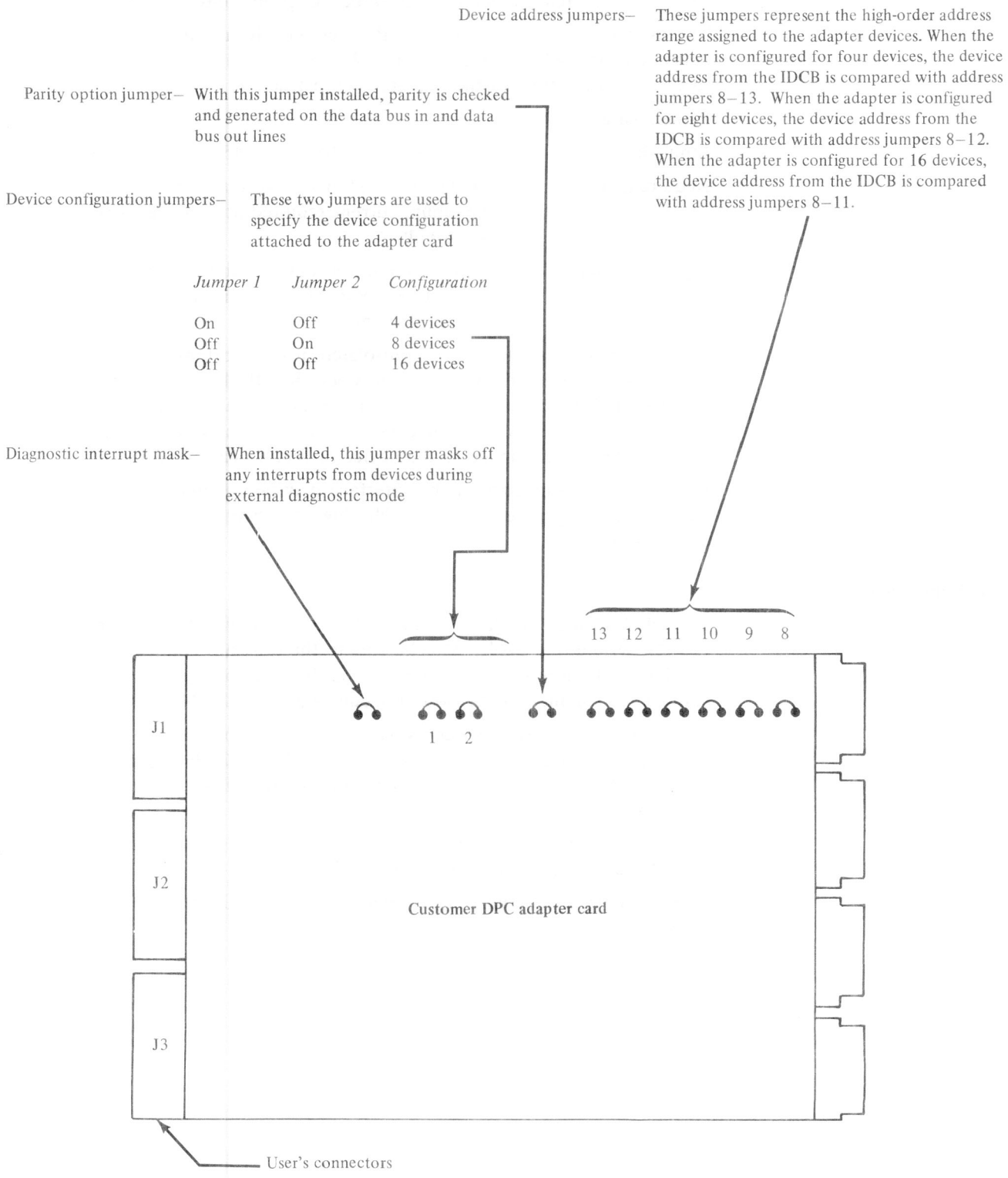


Figure 6-13. Jumper selections

DPC Adapter Design Considerations

The DPC adapter feature is used in applications that require access to the processor I/O channel; it does not provide cycle-steal capability. Therefore, the feature is limited to direct program control applications.

The overhead attributable to the DPC adapter, given that all user-device delays on the DPC interface are 0, is 2.5 microseconds (maximum) added to the execution time of the operate I/O instruction.

Recommended:

Input driver:	TTL open collector (SN75451 or equivalent)
Requirement:	Down level: +0.6 volt at 42mA, maximum; minimum current required at down level, 42 mA at +0.6 volt
Input terminators:	150-ohm and 300-ohm divider network to +5 Vdc ±10%; effective termination impedance equals 100 ohms

Note: Because this interface is nonisolated, it is important to ensure that there is a good ground connection between the OEM device being attached and the card file that contains the DPC adapter feature card. If there is not a good ground connection, a large common-mode voltage may be developed, and damage to the device or feature card could result.

Because the performance of this interface may be affected by noise, appropriate arc suppression, noise filtering, etc., may be necessary on the user's inputs.

Application Notes

The DPC adapter should be connected to a device with a maximum 6.1-m (20-ft) twisted-pair cable. Attachments to the top-card connector must use a polarized Berg housing, part number 65405-013 (or equivalent); Berg contact, part number 75598-003 (or equivalent); and #24 AWG wire.

The cable to the customer access panel feature can be made by using a 160-pin male connector block, Amp part number 202799-2 (or equivalent); female contact, Amp part number 66108-1 (or equivalent); and #24 AWG wire.

The DPC adapter card connector pin assignment for ground points should be followed at the device end of the cable.

Diagnostic wrap capability is provided at all the DPC adapter feature connection points for devices.

Appendix A. General Purpose Interface Bus Adapter (RPQ D02118)

Introduction

The term "General Purpose Interface Bus (GPIB)" is commonly used to identify the Institute of Electrical and Electronics Engineers (IEEE) Standard 488, as approved in 1975 and updated in 1978 (IEEE Standard 488-1975, IEEE Standard 488-1978). This interface standard was established to facilitate the interconnection of programmable instrumentation and other system components.

The IBM Series/1 General Purpose Interface Bus Adapter Feature, RPQ D02118, is designed to provide a cycle-stealing interconnection path between the OEM devices that adhere to the IEEE Standard 488 and the Series/1 processor I/O channel.

Adapter Functional Description

The GPIB adapter uses a bidirectional 16-signal interface for information and data exchange. This signal interface may be grouped functionally into three component buses (Figure A-1): (1) the management group (five lines), which provides overall bus control; (2) the transfer group (three lines), which provides an asynchronous three-wire "handshake" for information exchange; and (3) the data group (eight lines), which transfers all addressing, programming, and data information on the interface.

A normal GPIB implementation on the Series/1 consists of the GPIB adapter, which acts as the bus controller, and up to 14 additional noncontroller units. The controller first seizes the interface; it then configures the network by designating a single device to transmit data (talker) and a number of devices to receive data (listeners). The controller may configure itself as a talker or a listener, and multiple listeners may be active during any data or information transfer.

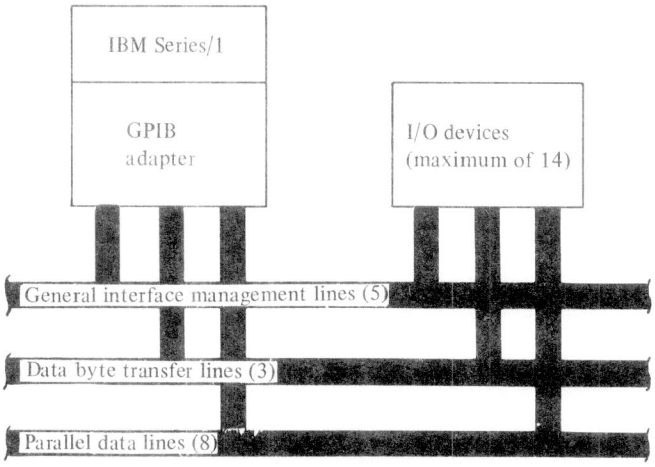


Figure A-1. Interface structure

The rate of transfer is determined by the speed with which the sending device places each byte on the bus and the effective data rate at which the slowest of all receivers accepts the data byte, up to a maximum instantaneous data rate of 65K bytes per second. Data rate is largely dependent upon the block size of the data transfered.

Adapter Hardware Description

The GPIB adapter is a single Series/1 I/O card, which provides cycle-stealing controller capabilities for an instrumentation network. The adapter may be plugged into any I/O position on a Series/1 processor card file or the 4959 I/O expansion unit card file. Multiple GPIB adapters may be installed on a Series/1 system, with each feature controlling a different GPIB network of OEM devices.

Interconnection between the GPIB adapter and the first OEM device on the interface is accomplished via a 4-meter (13.1-ft) cable (RPQ D02119), which provides an IEEE Standard 488 24-pin stackable connector as the user interface. Additional OEM devices are interconnected with 1-, 2-, and 4-meter (3.3-, 6.5-, and 13.1-ft) IEEE 488 cables, which are available throughout the industry.

Adapter Command Functions

The GPIB adapter utilizes the cycle-stealing architecture of the Series/1 to provide a high-speed controller for a GPIB network. The feature accepts commands from the Series/1 processor I/O channel and provides all required interface protocol for those operations. There are four groups of GPIB adapter commands:

- Bus-initialization commands
- Information-exchange commands
- Universal GPIB commands
- Polling and status commands

Figure A-2 shows the command groups, with a description for each operation. All command acronyms used by the GPIB adapter relate to the specific operation, as described in the IEEE standard.

Bus initialization

Command	Description
Write Interface Clear (IFC)	Causes the bus to go into a quiescent state.
Write Remote Enable (REN)	Places addresses on the bus. These addresses allow the specified devices to respond to further operations.

Information exchange

Command	Description
Write Configure	Used to transfer configuration information and/or device programming information (if less than 50 bytes) on the bus.
Write Data	Places device programming information or data on the bus for those devices addressed as listeners.
Read Data	Allows data to be transferred from a device on the bus into Series/1 main storage.
Read Monitor	Allows data to be transferred/monitored between devices on the bus.

Universal

Command	Description
Write Selected Device (SDC)	Causes those devices whose addresses are contained in the data area to be reset.
Write Device Clear (DCL)	Causes all devices to be reset.
Write Group Execute Trigger (GET)	Causes those devices whose listen addresses are contained in the data area to have their predefined basic operation initiated.
Write Go To Local (GTL)	Causes those devices whose listen addresses are contained in the data area to respond to both the interface messages and panel controls.
Write Local Lock Out (LLO)	Causes the devices to respond only to interface control messages (not panel controls).

Figure A-2 (Part 1 of 2). GPIB adapter command groups

Polling and Status

Command	Description
Write Parallel Poll Enable (PPE)	Puts those devices whose listen addresses are contained in the data area into a response mode.
Write Parallel Poll Disable (PPD)	Used to selectively disable those devices whose listen addresses appear in the data area from participating in a parallel poll sequence.
Write Parallel Poll Unconfigure (PPU)	Causes all devices that are currently able to respond to a parallel poll to be forced into a parallel poll idle state.
Write Parallel Poll (PPL)	Conducts a parallel poll for those devices configured during the Write Parallel Poll Enable (PPE) command.
Write Serial Poll Enable (SPE)	Allows the devices whose talk addresses are contained in the data area to present status.
Write Serial Poll Disable (DPS)	Disables the serial poll status reporting ability of the devices.
Read Serial Poll Results (SPL)	Reads the result of the latest serial poll into Series/1 main storage (one byte per device).
Read Parallel Poll Results (PPL)	Reads the result of the latest parallel poll into Series/1 main storage (one byte).

Figure A-2 (Part 2 of 2). GPIB adapter command groups

Application Summary

The GPIB adapter can interface with different types of devices, such as: printers, keyboards plotters, card readers, tape drives, graphic displays, and testing instrumentation (such as digital voltmeters, oscilloscopes, signal generators, and frequency analyzers).

Because of the asynchronous transfer architecture of IEEE Standard 488, there are no transmission limitations on intercommunication between unrelated devices; the slowest device governs the data rate. This technique provides a solution to the common problems of data overrun, baud-rate compatibilities, and synchronous communication.

Implementation of IEEE Standard 488

The Series/1 GPIB adapter implements the following interface function standards of IEEE Standard 488:

C1 GPIB adapter is the only allowed system controller, and it provides the control for the generation of the interface clear (IFC) and the remote enable (REN) interface messages.

C2 This interface function allows the GPIB adapter to generate the interface clear (IFC) message.

C3 This interface function allows the GPIB adapter to generate the remote enable (REN) message.

C4 This interface function allows the GPIB adapter to respond to service requests (SRQs) generated by the devices attached to the interface bus. The GPIB adapter responds synchronously to an active service request (SRQ) and generates an attention interrupt to the processor, if the adapter is not busy.

C25 This interface function allows the GPIB adapter to send interface messages, conduct parallel polls, conduct serial polls, and take control synchronously. As the controller in charge, it cannot receive control from, or pass control to, another device or itself.

Interface functions are implemented as follows:

SH1 Source handshake interface function, in combination with AH1, is used to control the initiation, transmission, and termination of multiline messages.

AH1 Acceptor handshake interface function, in combination with SH1, is used to control the initiation, reception, and termination of multiline messages. With the SH1 function, the AH1 function guarantees an asynchronous transfer of each message byte between a single sending device and one or more receiving devices.

T8 Talker interface function is capable of sending configuration and programming information to devices on the interface. This function restricts the GPIB adapter from responding to a serial poll or being configured in the talk-only mode.

L4 Listener interface function is capable of receiving device-dependent data, such as multiline messages from other devices. The GPIB adapter inhibits configuration in the listen-only mode.

SRQ Service request interface function inhibits the GPIB adapter from generating a service request interface message.

RLO Remote local interface function inhibits the GPIB adapter from responding to the remote enable (REN), go to local (GTL), or local lock out (LLO) interface messages; the GPIB adapter is the only permitted active controller.

PPO Parallel poll (PPO) interface function inhibits the GPIB adapter from responding to a parallel poll sequence; the GPIB adapter is the only permitted active controller.

DCO Device clear (DCO) interface function inhibits the GPIB adapter from responding to a device clear message; the GPIB adapter is the only permitted active controller.

DTO Device trigger (DTO) interface function inhibits the GPIB adapter from responding to a group execute trigger (GET) message; the GPIB adapter is the only permitted active controller.

For further information concerning these functions or the general purpose interface bus, refer to the *IEEE Standard Digital Interface for Programmable Instrumentation*, published by the Institute of Electrical and Electronics Engineers, Inc., 345 East 47th Street, New York, New York 10017. Refer also to the *IBM Series/1 General Purpose Interface Bus (GPIB) Adapter—RPQ D02118 Custom Feature*, GA34-1556.

Index

READER'S COMMENT FORM

GA34-0033-3

IBM Series/1 User's
Attachment Manual

Your comments assist us in improving the usefulness of our publications; they are an important part of the input used in preparing updates to the publications. IBM may use and distribute any of the information you supply in any way it believes appropriate without incurring any obligation whatever. You may, of course, continue to use the information you supply.

Please do not use this form for technical questions about the system or for requests for additional publications; this only delays the response. Instead, direct your inquiries or requests to your IBM representative or the IBM branch office serving your locality.

Corrections or clarifications needed:

Page Comment

Cut or Fold Along Line

Please indicate your name and address in the space below if you wish a reply.

Thank you for your cooperation. No postage stamp necessary if mailed in the U.S.A. (Elsewhere, an IBM office or representative will be happy to forward your comments.)

Reader's Comment Form

Cut Along Line

Fold and tape | Please Do Not Staple | Fold and tape

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 40 ARMONK, NEW YORK

POSTAGE WILL BE PAID BY ADDRESSEE

IBM Corporation
Systems Publications, Dept 27T
P.O. Box 1328
Boca Raton, Florida 33432

Fold and tape | Please Do Not Staple | Fold and tape

IBM

International Business Machines Corporation
General Systems Division
4111 Northside Parkway N.W.
P.O. Box 2150, Atlanta, Georgia 30301
(U.S.A. only)

General Business Group/International
44 South Broadway
White Plains, New York 10601
(International)

GA34-0033-3
Printed in U.S.A.

READER'S COMMENT FORM

GA34-0033-3

IBM Series/1 User's
Attachment Manual

Your comments assist us in improving the usefulness of our publications; they are an important part of the input used in preparing updates to the publications. IBM may use and distribute any of the information you supply in any way it believes appropriate without incurring any obligation whatever. You may, of course, continue to use the information you supply.

Please do not use this form for technical questions about the system or for requests for additional publications; this only delays the response. Instead, direct your inquiries or requests to your IBM representative or the IBM branch office serving your locality.

Corrections or clarifications needed:

Page Comment

Cut or Fold Along Line

Please indicate your name and address in the space below if you wish a reply.

Thank you for your cooperation. No postage stamp necessary if mailed in the U.S.A. (Elsewhere, an IBM office or representative will be happy to forward your comments.)

Reader's Comment Form

Cut Along Line

Fold and tape | Please Do Not Staple | Fold and tape

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 40 ARMONK, NEW YORK

POSTAGE WILL BE PAID BY ADDRESSEE

IBM Corporation
Systems Publications, Dept 27T
P.O. Box 1328
Boca Raton, Florida 33432

Fold and tape | Please Do Not Staple | Fold and tape

IBM

International Business Machines Corporation
General Systems Division
4111 Northside Parkway N.W.
P.O. Box 2150, Atlanta, Georgia 30301
(U.S.A. only)

General Business Group/International
44 South Broadway
White Plains, New York 10601
(International)

GA34-0033-3
Printed in U.S.A.